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Why an MC68300 or MC68HC16 Microcontroller May Fail to Release Reset

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Introduction

The most common reasons that a device from either of the MC68300 or MC68HC16 Families fails to come out of reset are:

- The pullup resistor on the RESET pin is too large. This pullup resistor should be no larger than 1 k.
- A capacitor is connected from the RESET pin to ground.

In no case should a capacitor be connected to the RESET pin.

NOTE: *Poor oscillator design and implementation can also cause the device to fail to release reset.*

General Information

This is what happens to the RESET pin during a power-on condition:

- When power is applied to the device, the RESET pin is driven low.
- The voltage-controlled oscillator (VCO) achieves phase-lock, and sets the SLOCK bit in the synthesizer control register (SYNCR).

- Tthe RESET line is driven low for 512 clock periods. At the end of the 512-clocks, the line is released and allowed to be pulled up by an external device. After 10 or 14 cycles have elapsed, the RESET line is again sampled. It the RESET pin is at a logic 0, the internal circuitry pulls it low for an additional 512 cycles, releases it for 10 or 14 cycles, and then samples it again. If the RESET pin is read as a logic 1 at the end of the 10- or 14-cycle period, the internal RESET signal is released on the intermodule bus and the device begins operation by fetching the initial stack pointer and program counter values. Once again, if the RESET signal fails to reach a logic 1 level in the prescribed time, check the value of the pullup resistor and be certain that no capacitors are connected to the RESET pin.

Considerations When Not Using the VCO

When the voltage-controlled oscillator (VCO) is not being used, it is important to hold the RESET line in its asserted (low) condition until both the power supply and the clock are stable.

As soon as the RESET line is released, the device will start counting the 512-clock period. If the clock is unstable or has entered a meta-stable mode, the clock frequency could be considerably outside the operating range of the device. If the clock is still unstable at the end of the 512-clock period, problems are sure to arise. Usually, the device will not operate if this is the case.

Low-Voltage Inhibit for Reset Release

Putting a low-voltage inhibit (LVI) device on the RESET pin will prevent the release of RESET before the power supply has reached its final value. More importantly, the LVI will prevent the device from entering an unknown state, if the power supply dips below specified minimum operating voltage and then rises back to proper operating level. If this

situation (commonly called a brown-out) occurs, the device may no longer function correctly and may not respond to a RESET signal.

To ensure that a brown-out condition will not cause the device to malfunction, an LVI chip can place the device in RESET while the device is still in a known operating condition. Then, if a brown-out does occur, the device will be held in a known condition while the power is below the operating range of the part.

When power is restored, RESET will be released by the LVI chip and the device will operate normally.

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