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Autovector Generation Using Chip Select Logic on MC68300 and MC68HC16 Devices

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Introduction

An AVEC signal can be used to respond to an interrupt acknowledge cycle for one of the external interrupts (IRQ [7:1]) and automatically choose a particular interrupt vector.

IRQ [7:1] use vector numbers 11–17 on the CPU16 and vector numbers 25–31 on the CPU32. It is possible to respond to the interrupt acknowledge cycle with a DSACK signal which requires an external device to supply its own interrupt vector.

General Information

Once an external interrupt is recognized and the end of the current instruction is reached, an internal arbitration cycle occurs to determine the source of the interrupt. Only external interrupts can use AVEC. The following explanation will be offered to show how to use the internal chip select logic to generate the AVEC signal.

Each chip select pin has an associated base address register (CSBAR) and option register (CSOR) that define certain characteristics regarding

when a chip select line will be asserted. There are also two chip select pin assignment registers. There are two bits in the chip select pin assignment registers associated with each chip select line whereby a line can be configured as a 16-bit chip select, an 8-bit chip select, a general-purpose output, or an alternate function, such as bus request or function code 2. Whether or not a chip select line is configured as a chip select line or other function, the associated CSOR and CSBAR register comparators will be active.

This means, for instance, that even if the FC0/CS3 line is configured as function code 0, a general-purpose output, an 8-bit chip select or a 16-bit chip select, the DSACK and AVEC generation circuitry is always active and can be used to internally generate either AVEC or DSACK signals.

To internally generate an AVEC signal, the CSOR and CSBAR registers can be programmed in the following manner. It is important to note that during the interrupt acknowledge cycle, function code pins [2:0] are driven to logic ones. Address bus bits ADDR [23:4] are driven to logic ones. If a particular line is configured as a chip select and programmed to respond during an IACK cycle, the chip select will assert. If the line is configured as an output or alternate function, the line will not assert during the IACK cycle. However, the AVEC or PSACK signal will still be generated.

The respective fields of CSBAR should be programmed to the value $FFF8.

Here is the breakdown for these bits:

- Bits [15:3] — Program all of these bits to logic 1s. Remember, the address bus will be driven to address%1111111111111111xxx.
- BLKSZ — Program this field to%000, for example, a block size of 2 Kbytes.

For autovectoring, the respective fields of CSOR should be programmed according to the information in **Table 1**.

Table 1. Autovectoring CSOR Program

Mode	ASYNC
Byte	Both will always work.
R/W	READ or READ/WRITE; the IACK cycle is always a READ cycle
STRB	AS
DSACK	Don’t care
Space	CPU space; IACK cycles always occur in CPU space only
IPL	Program this field either to the individual interrupt for which autovectoring is desired or to %000, which causes autovectoring to occur for all external interrupts.
AVEC	ON

Summary

The IACK cycle is always a read cycle occurring in CPU space at address $FFFFFX.

A chip select line can be programmed to any of its functions, and the internal base address and option register functions will still be active.

If the chip select line is programmed to a chip select function via the CSPAR register, the external chip select pin will assert during the IACK cycle if there is an address match. An internally generated AVEC always causes the IACK cycle to be a fast termination cycle.

AVEC, whether generated internally or supplied externally, can only be used to terminate the IACK cycle of an external interrupt, IRQ [7:1].

Unless all external interrupts are to use autovectors (IPL = %000), an individual set of base address/option registers must be used for each level of interrupt.

An AVEC cannot be used to terminate the IACK cycle of an internally generated interrupt from any module, including the periodic interrupt timer (PIT) of the system integration module (SIM).

When responding to SIM interrupts, which include the external interrupts IRQ [7:1], the IARB field of the SIM configuration register must be set to a non-zero value. A value of %0000 in this field will cause all SIM interrupts to be treated as spurious interrupts if the IACK cycle is terminated with BERR.

NOTE: *The IACK cycle of both internal and external interrupts can be terminated with an external DSACK. Only an external interrupt's IACK cycle can be terminated with AVEC.*

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