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DSACK Generation on the System Integration and Single-Chip Integration

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General Information

The system integration module (SIM) and single-chip integration module (SCIM) provide programmable chip-select logic to help the designer interface a modular microcontroller to external peripherals.

Chip select assertion can be synchronized with the bus control timing to provide correct timing signals for external devices.

The chip select logic also generates DSACK and AVEC signals internally.

Question

A question that often arises is: What happens if a chip select is programmed as either discrete output or alternate function in the chip-select pin assignment register (CSPARx), but the chip-select base address (CSBARx) and chip-select option registers (CSORx) are also programmed?




Intent

The intent is to use the pin for discrete output or its alternate function and also use the internal chip select logic to generate a DSACK signal.

This assumes that the external address pins are being used to generate one or more chip-enable signals discretely and also that the external pins DSACK0 and DSACK1 are not used as bus control signals.

Although the user's manual states that doing this is allowed, it fails to state whether the DSACK is for an 8- or 16-bit port. In this case, if CSPARx is programmed for alternate function, the DSACK will be for a 16-bit port. But if CSPARx is programmed as discrete output, then the DSACK will be for an 8-bit port.

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