

# Motorola Semiconductor Engineering Bulletin

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### Disabling All Interrupts on Power-On for MC683xx and MC68HC16 Devices Using the Single-Chip Integration Module or System Integration Module

By Charles Melear  
Austin, Texas

#### General Information

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From a power-up condition with either the MC683xx or the MC68HC16 Families of MCUs, IRQ7 will be active immediately. If the IRQ7 line is driven to an active low condition, program runaway is possible.

If the IARB field in the system integration module (SIM) or single-chip integration module (SCIM) configuration register is 0 out of reset, the interrupt is treated as a spurious interrupt. If the spurious interrupt vector points to a valid address and that address contains a valid spurious interrupt exception routine, the exception is recoverable. Otherwise, the program runs away.


Only the early mask sets of the MC68332 came out of reset with the IARB bits set to 0; however, in modern versions of the SCIM and SIM, the IARB field is set to \$F. However, if no interrupt handler is present for IRQ7, the program will still run away.

To prevent the occurrence of all interrupts from the release of reset, the port containing the IRQ pins can be configured via the data bus to be I/O (input/output) pins instead of interrupts.



On the MC68332, the IRQ pins are on port F. If data bus pin 9 (DATA9) is held high at the release of reset, the port F pins will be IRQ lines and IRQ7 will immediately be active. If DATA9 is held low at the release of reset, port F will be I/O lines and interrupts will not be possible.

If IRQs are desired at a later time, the pin assignment register for port F can be modified to make any or all of the port F pins act as IRQ lines.

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