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Unexplained Three-Stating of the Address Bus on M68300 and M68HC16 Devices

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Introduction

Some users of the devices in the M68300 and M68HC16 Families have observed that the devices appear to halt operation and go into a three-stated condition. This condition appears to occur either randomly or occur in a certain block of code, but not at a certain instruction in that block of code.

General Information

This problem is often caused by improperly configuring the data bus at the release of RESET.

In particular, chip select line 0 (CS0) can assume one of three different functions. This line can be configured as:

- A 16-bit chip select
- An 8-bit chip select
- A bus request (BR)

However, at the release of reset, this line can only assume the function of a 16-bit chip select or bus request.

Many designers rely on the internal pullup devices on the data bus to hold the respective data bus pins high during reset. This, in general, is not a good practice. Sometimes the pullup device fails to maintain a data bus pin at a logic 1 during the time RESET is asserted.

Obviously, when RESET is released, the data bus pin may be interpreted as a logic 0 instead of a logic 1. The implication for the data bus 1 pin is that it will cause the CS0 pin to be configured as BR instead of a 16-bit chip select.

Even if this scenario occurs, the BR pin may float to a logic 1 condition where it will have no effect. Because of capacitive coupling and noise, the BR pin may be driven to a logic 0. At this time, the MCU will halt, three-state its address/data bus structure, and wait until the BR pin is driven (or floats) back to a logic 1 condition.

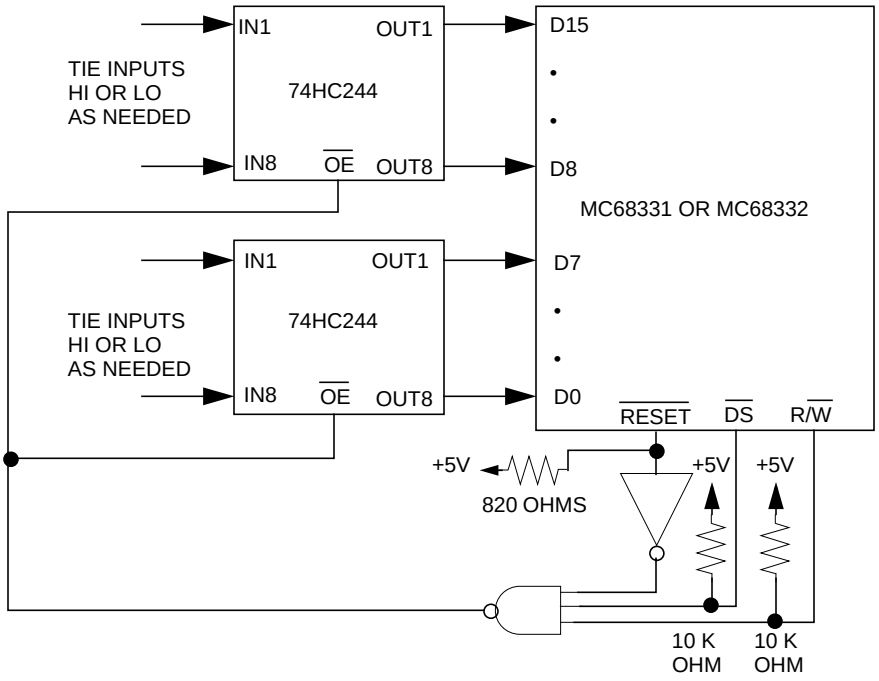
The problem can be alleviated by simply pulling up the data bus 1 pin with a 10-K resistor.

NOTE: *For all the specification purists, putting a resistor on a data bus pin degrades performance at higher frequencies. However, many designers use resistive pullups without significant, practical effects.*

Another method for solving the problem of the CS0 line inadvertently being configured as BR is to put a pullup resistor on the CS0 line and then have software explicitly write to the chip-select pin assignment register to configure CS0 as BR. If the CS0 line is accidentally configured as BR at the release of RESET, the pullup resistor will keep the BR line from floating to a logic 0, thus three-stating the data bus.

The preferred method for asserting data bus pins during reset involves driving the data bus with an active driver. A circuit to perform this function is shown in **Figure 1**.

While this method does require external circuitry, it is certainly recommended when high levels of noise may be encountered or when high reliability of operation is an overriding concern. There is a hold time requirement of 5 ns after the release of reset for a data bus pin to be recognized reliably at a particular logic level.



NOTE: THIS CIRCUIT PROTECTS MEMORY ACCESSES THAT ARE CURRENTLY IN PROGRESS. THAT IS, IF THE RESET PIN IS ASSERTED DURING AN EXTERNAL MEMORY ACCESS, THE OUTPUTS OF THE 74HC244'S CANNOT BE TURNED ON UNTIL THE EXTERNAL MEMORY IS COMPLETED, THUS PREVENTING THE CORRUPTION OF DATA BEING WRITTEN TO THE EXTERNAL MEMORY DEVICE. IF THIS IS NOT A CONCERN TO THE SYSTEM, THEN THE RESET PIN CAN SIMPLY BE TIED DIRECTLY TO THE OE PINS OF THE 74HC244.

Figure 1. Circuitry to Drive Data Bus Pins during $\overline{\text{RESET}}$ Assertion

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