Order this document
by EB268/D

Motorola Semiconductor Engineering Bulletin

EB268

Starting and Stopping the Time Processor Unit Clock Using the Background Debug Mode

By Sharon Darley
Austin, Texas

Introduction

Developers of time processor unit (TPU) microcode may want to halt microcode execution when debugging.

One way to do this is to enter the background debug mode (BDM), a special operating mode in which normal instruction execution is suspended.

Once BDM is entered, the TPU can halt execution after the current microcycle or at the end of the current state. Once halted, the TPU resumes execution when the CPU exits from BDM.

For more information on microcode development support, see the *M68300 Family TPU Time Processor Unit Reference Manual*, Motorola document number TPURM/AD. This is the original version of the TPU reference manual. This information does not appear in revision 1, the *Modular Microcontroller Family TPU Time Processor Unit Reference Manual*.

General Information

A debugger called TPUBUG that can stop the TPU and single step through microcode is available on the Freeware Data System. Using this debugger is the easiest way to stop the TPU and debug microcode. However, the TPU can be halted without using the debugger.

To Halt the TPU

First, the MCU must be put in special test mode so that the development support control register (DSCR) can be modified. This register resides in supervisor space and can be written only when the MCU is in test mode. Otherwise, it reads as $0000. This register determines the TPU microengine's response to the FREEZE signal, which the CPU asserts when it enters BDM.

These four steps explain how to enter special test mode and enable the background mode so that it can be entered upon the occurrence of certain conditions.

1. Enable BDM by holding BKPT low at the rising edge of RESET. It must be held low for at least two clock cycles prior to negation of RESET.
2. If using the MC68332, MC68HC16Z1, or MC68HC16Z2, enable the test mode by pulling the TSTME pin low. If using the MC68F333 or the MC68HC16Y1, make sure that the TSC pin is always low to prevent all of the output drivers from going into an inactive, high-impedance state.
3. Enter test mode by setting the ETM (enter test mode) bit. The ETM is bit 0 in the test submodule control register (CREG) at address $YFFA38. This bit can be written only once, so it must be set on the first attempt to write it.
4. Set the IMB FREEZE response bits (FRZ0/FRZ1) in the DSCR ($YFFE04). These two bits (bits 7 and 8) determine the TPU microengine response to a FREEZE signal.
    a. For the TPU to halt at the end of the current microcycle upon the assertion of FREEZE, set bit 8. Clear bit 7. For the TPU to halt at the next time-slot boundary, set both bits.

Now that BDM has been enabled, enter BDM by:

- Holding the BKPT signal low
- By causing a double bus fault, or
- By executing the BGND instruction.

All of these methods cause the CPU to assert the FREEZE signal, thus stopping the TPU until FREEZE is negated.

How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution, P.O. Box 5405, Denver, Colorado 80217, 1-800-441-2447 or 1-303-675-2140. Customer Focus Center, 1-800-521-6274

JAPAN: Nippon Motorola Ltd.: SPD, Strategic Planning Office, 141, 4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan. 03-5487-8488

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd., 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

Mfax™, Motorola Fax Back System: RMFAX0@email.sps.mot.com; http://sps.motorola.com/mfax/; TOUCHTONE, 1-602-244-6609; US and Canada ONLY, 1-800-774-1848

HOME PAGE: http://motorola.com/sps/

MOTOROLA