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Problems with the PPWA Function on Revision P MC68332 Devices

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Introduction

The period/pulse width accumulation (PPWA) function on the time processor unit (TPU) is an accurate way to accumulate and measure pulse periods and pulse high times. The PPWA function can accumulate either 16- or 24-bit periods or pulse widths.

However, users sometimes experience problems when using the 24-bit mode.

General Information

The microcode for the PPWA function was altered for the revision P of the MC68332 in an effort to achieve greater performance.

Unfortunately, the alterations caused a problem in the 24-bit mode. Although most updates of ACCUM and PPWA_UB will be accurate, once in awhile, a particular sequence of events will cause PPWA_UB to be updated erroneously.

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There are three ways a match or transition service request can be generated for PPWA. All three requests cause the PPWA function to enter state ACCUM_LOW_PIN.

The first type of request is generated when a falling transition is reached. The second type of request is generated if updating ACCUM causes an overflow, and PPWA_UB needs to be updated. The third type of request is generated if it is time to update ACCUM due to an ACCUM_RATE match.

The problem occurs if this sequence of service requests occurs:

1. A falling transition is detected. The TPU enters state ACCUM_LOW_PIN. ACCUM is updated, and an overflow is detected. A flag is set so that the channel will request service to re-enter state ACCUM_LOW_PIN to process the overflow by incrementing PPWA_UB. State ACCUM_LOW_PIN is exited, and the channel then requests service to re-enter the same state so that it can process the overflow.

2. In the same cycle that the service request to process the overflow is generated, a match service request is generated to update ACCUM as indicated by the parameter ACCUM_RATE. This request also causes the TPU to enter state ACCUM_LOW_PIN; however, it overrides the request due to overflow. As a result, the TPU still enters state ACCUM_LOW_PIN, but it ignores the service request due to the overflow, and PPWA_UB is not incremented, even though it should be.

This problem causes the accumulation to be slightly lower than it should be. Depending upon the value in ACCUM_RATE, the frequency of overflows, and the value in MAX_COUNT, the error of the accumulated period or pulse width can be minimal. Only the 24-bit mode on revision P processors (4D87M or 2D87M) are affected. The 16-bit mode is not affected, and future MC68332 devices will have this problem corrected.

Users who experience this problem have a few workaround options:

1. Replace the processors with a different mask revision. Older revisions of the chip, as well as future revisions, will not have this problem.

2. Use the programmable time accumulator function (PTA) that will be available on the MC68332G mask instead of PPWA. PTA is similar to the PPWA function, except that it does not generate links. It produces a 32-bit accumulation, and it can measure pulse low times as well as pulse high times.

3. Set ACCUM_RATE to $FF, which is the slowest setting possible. This may help alleviate the problem, depending on the individual application. Or experiment with the ACCUM_RATE setting, since the frequency of an update due to ACCUM_RATE and a falling transition occurring simultaneously can be estimated using probability.

4. Use the 16-bit mode if possible.

5. Download the corrected PPWA function (or the PTA function) into RAM and run the TPU out of emulation mode. See *Using the TPU Function Library and TPU Emulation Mode,* Motorola document order number TPUN00/D for more information on running the TPU in emulation mode. A debugger that allows the TPU to run in emulation mode is also available from Motorola. Standard functions are available on the Motorola website, http://www.mcu.motsps.com. Select FTP file server.

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