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Low Power Write Enable Generation for M68300 Family Microprocessors

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Dynamic bus sizing support circuitry is normally implemented using PALs. However for battery-powered applications, these devices can draw unacceptable amounts of power. The circuit presented here implements byte write enable functions for a 16-bit processor/memory combination, using just two[1] low power 74HCTTL devices.

16-bit Dynamic bus sizing makes use of 5 processor signals[2] that implement a protocol for exchanging information about the external port size, base address, and bytes remaining to be transferred.

SIZ1 and SIZ0 indicate the number of bytes remaining for transfer. DSACK1 and DSACK0 indicate port width to CPU (Fixed, 16-bit memory). A0 indicates the base address for transfer.

SIZ1	SIZ0	A0	Transfer Type	Y	UWE	LWE
0	0	0	long word, aligned	0	0	0
0	0	1	long word, misaligned	X	1	1
0	1	0	byte, aligned	2	0	1
0	1	1	byte, misaligned	3	1	0
1	0	0	word, aligned	4	0	0
1	0	1	word, misaligned	X	1	1
1	1	0	3 bytes, aligned	X	0	0
1	1	1	3 bytes, misaligned	X	1	1

Table 1. Dynamic Bus Sizing Signals and Circuit Outputs
(X represents the "don't care" state)

The left three columns in the above table show CPU outputs that indicate size and base address of the transfer taking place. In the dynamic bus sizing circuit, these three signals are fed to the address inputs of a 74HC138 decoder, resulting in a uniquely decoded signal representing each state (shown in the 'Y' column). After generating the Y outputs, it is simply a matter of using combinatorial logic to generate the required upper and lower byte write enables. R/$\overline{W}$ (inverted, which may require an additional device if one is not present in the circuit), $\overline{CSx}$, to ensure operation only when memory is being addressed, and $\overline{DS}$ to ensure correct memory write timings.

1. Three devices may be required, as the circuit uses an inverted version of the R/$\overline{W}$ signal. It is assumed that an inverter or inverted version of R/$\overline{W}$ will be available elsewhere in the design.
2. Refer to the relevant processor data books for a full description of dynamic bus sizing and the signals involved.

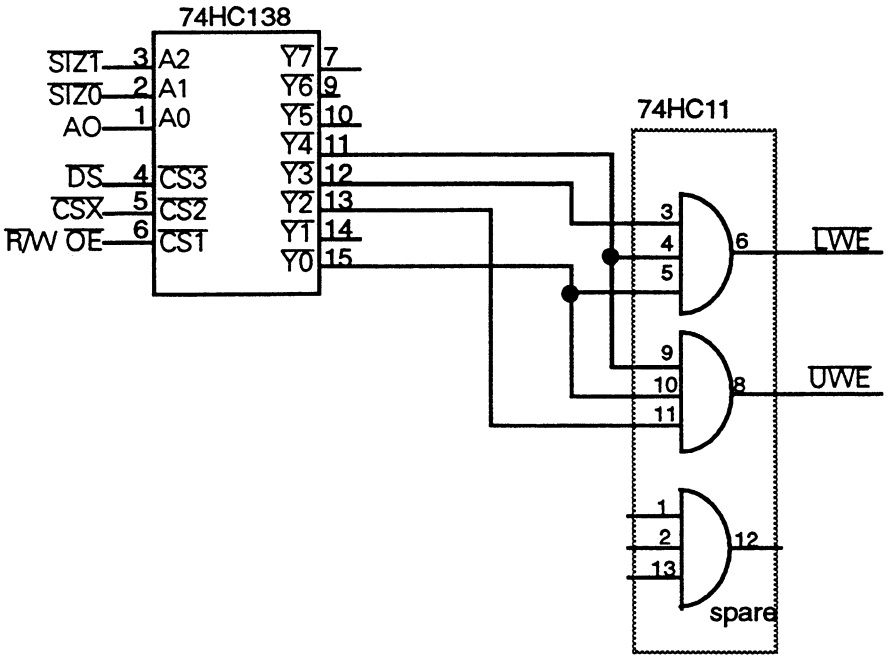

Figure 1. Dynamic Bus Sizer Circuit Diagram

The output signals are conditioned with Data Strobe, a Chip Select, and Read/Write, to ensure that the decoder is only enabled when the cycle is a write[3], Chip Select is asserted, and Data Strobe[4] is asserted.

The circuit in Figure 1 has been built and tested in a MC68340-based computer.

If the above circuit is to be implemented, please ensure that memory timing requirements are adhered to. Should they be violated, the circuit may still function, but with reduced reliability. The critical timing path through the above circuit is tP(74HC138) + tP(74HC11), approximately 50ns worst case. Should the delays prove unacceptable, 74AC logic would reduce the overall delay to approximately 18ns max.

For SRAM-based designs, the processor Chip Select signals can be programmed to generate internal DSACK signals. For such circuits, the above design can be used 'as-is'. For DRAM designs which require external DSACK generation, this circuit would have to be incorporated into the DRAM controller design.

3. Dynamic Bus Sizing is only required for write cycles
4. Data Srobe is not required if Chip Select is programmed to follow Data Strobe timings.

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