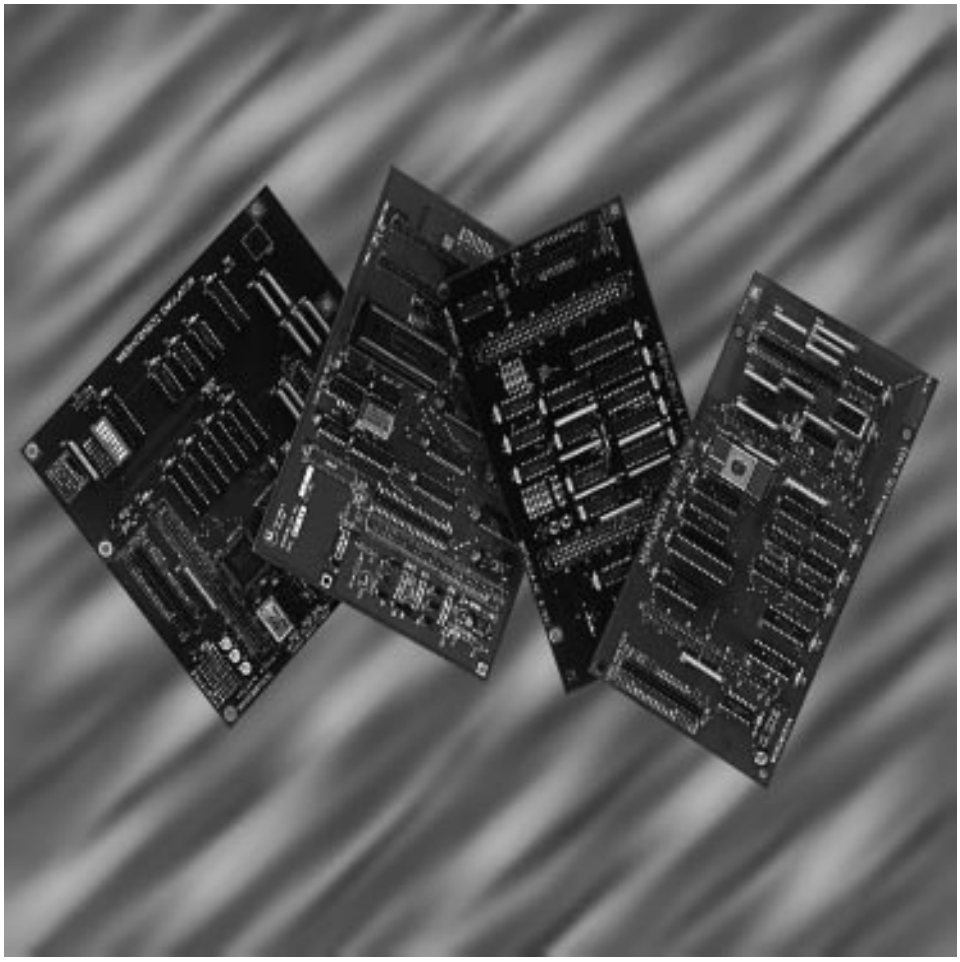
M68EM05JP7UM/D

M68EM05JP7

EMULATION MODULE
USER'S MANUAL



MOTOROLA

M68EM05JP7

Emulation Module
User's Manual

MOTOROLA

Motorola reserves the right to make changes without further notice to any products herein to improve reliability, function, or design. Motorola does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part.

Motorola and the Motorola logo are registered trademarks of Motorola, Inc.

Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

Revision History

The following table summarizes differences between this revision and the previous revision of this emulation module user's manual.

Previous Revision	NONE
Current Revision	1.0
Date	06/96
Changes	N/A
Location	N/A

Revision History

Table of Contents

Table of Contents

General Description

Contents

Introduction

Your M68EM05JP7 gives your Motorola development tool the ability to emulate target systems based on MC68HC705JP7, MC68HC705JJ7, and MC68HC05JJ6 microcontroller units (MCUs). The M68EM05JP7 is designed to be a low-voltage emulator, operating in the 3.0 Vdc to 5.0 Vdc range at maximum rated frequencies per the general release specification.

By substituting a different emulation module (EM), you can enable your Motorola development tool to emulate other MCUs. Refer to *Motorola's Development Tool Selector Guide*, order number SG173/D, for a complete list of available EMs.

This hardware user's manual explains connection, configuration, and operation information specific to the M68EM05JP7 emulation module. The module can be installed in two Motorola development systems. To configure your M68EM05JP7 for either an MMDS or an MMEVS, follow the instructions given in **MMDS/MMEVS Configuration and Operation** on page 19.

Emulation Components

Motorola's complete emulation system consists of the emulation module described in this manual as well as other separately purchased options described in the following paragraphs.

These items are included with the M68EM05JP7 emulation module:

- **An M68EM05JP7 emulation module (EM)** — The printed circuit board that enables system functionality for MC68HC705JP7 MCUs. The female connectors, on the bottom of the module, mate with male connectors on a development system platform board. The EM also has a connector for the target cable assembly.
- **Configuration software** — 3 1/2-inch diskette containing personality files for this module.

Separately purchased Motorola modular development tool options include:

- **An MMEVS platform board (M68MMPFB0508)** — The MMEVS is an economical development tool that provides real-time in-circuit emulation. The unit's integrated design environment includes an editor, an assembler, a user interface, and a source-level debugging program.
- **An MMDS0508 modular development system (M68MMDS0508)** — The MMDS is a high-performance development tool that has all the capabilities of the MMEVS. In addition, it also has a power supply, a bus state analyzer, and real-time memory windows.
- **Flex cable target assembly** — Refer to **Target Cable Assemblies** on page 12 for more information.

User supplied components include:

- **Host computer** — See the appropriate development tool user's manual for minimum requirements.
- **Power supply** — +5 Vdc is required for the MMEVS.

Emulation Module Layout

Figure 1 shows the layout of the M68EM05JP7. Jumper header W1 controls the low-power oscillator (LPO) source. Jumper header W2 lets you select the external pin oscillator (EPO) source. Jumper header W3 selects the software pulldown inhibit mask option for port A. Jumper header W4 controls the voltage applied to the $\overline{IRQ}/V_{PP}$ pin. Jumper header W5 determines the source voltage for the $\overline{IRQ}/V_{PP}$ pin.

Target connector J2 is the interface to a target system; this connector uses a separately purchased target cable assembly. When you install the M68EM05JP7 on the MMDS, the target cable passes through the slit in the station module enclosure. Connector J1 connects to a logic analyzer.

Variable resistor VR1 controls the MCU operating voltage between 3.0 V and 5.0 V. Test point header TP1 is the monitor point for MCU operating voltage adjustment. The MC68HC705JP7 MCU is at location XU22.

DIN connectors P1 and P2 connect the EM and a development system platform board. Lever terminal connector P3 is for inputting the personality EPROM (PEPROM) programming voltage.

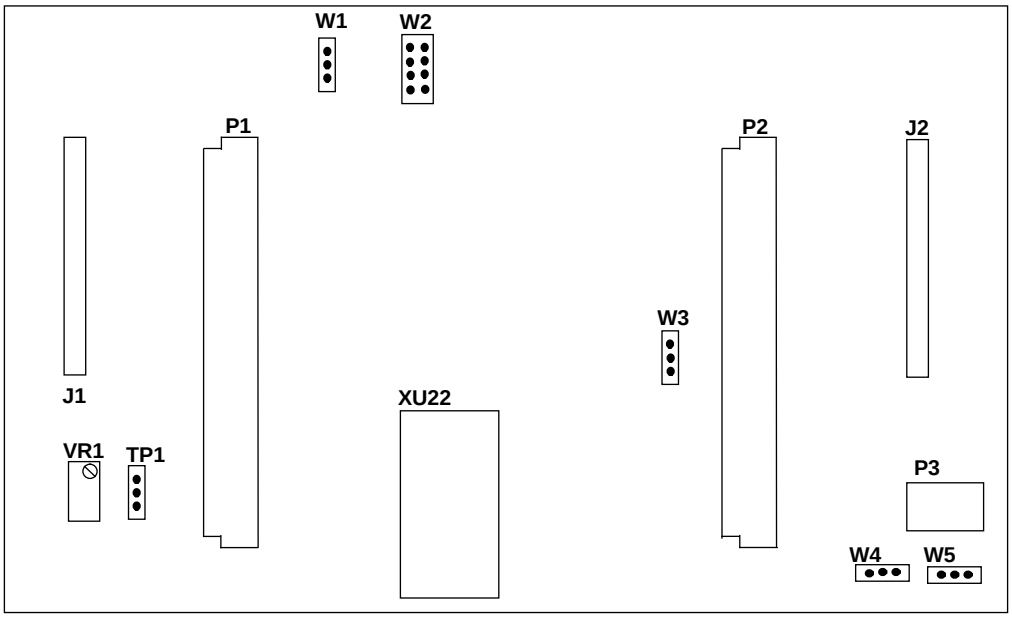


Figure 1. M68EM05JP7 Emulation Module

Target Cable Assemblies

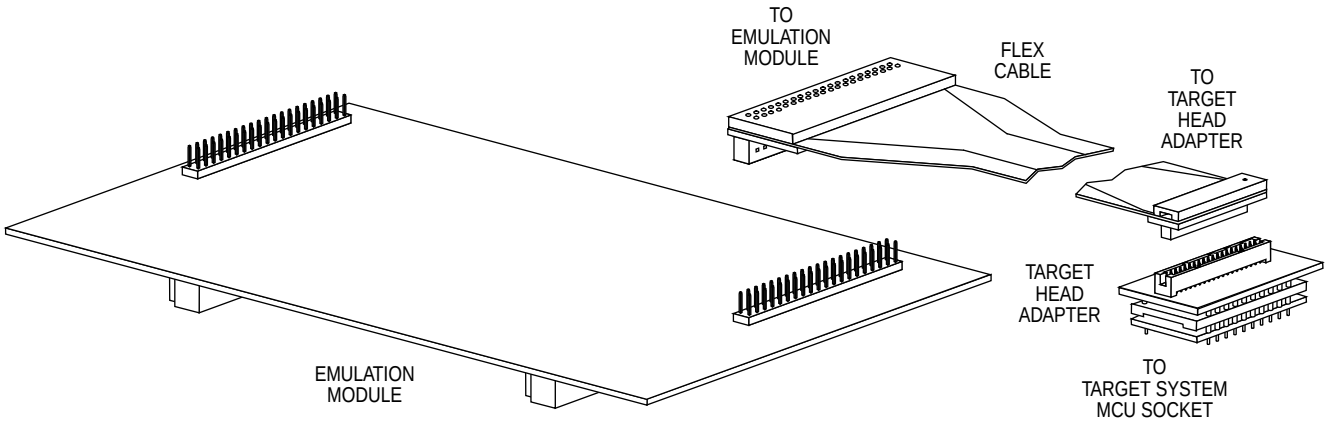
To connect your M68EM05JP7 to a target system, you need a separately purchased target cable assembly. Cable assemblies are available for four MCU packages: 20- and 28-pin DIP and 20- and 28-pin SOIC packages.

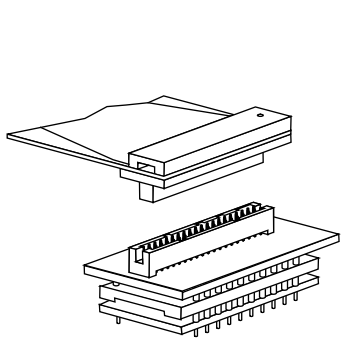
The target cable connects to the emulator via connector J2 on the M68EM05JP7 emulation module. Pin assignments and signal descriptions for connector J2 can be found in **Target Cable Connector Pin Assignments** on page 14.

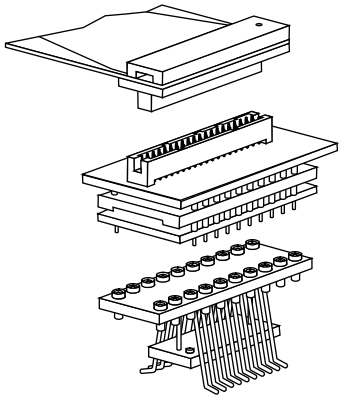
Figure 2 represents a target cable assembly. An assembly for DIP packages consists of a flex cable and a target head adapter. The assembly for SOIC packages requires an additional SOIC adapter. One end of the flex cable plugs onto M68EM05JP7 connector J2 with orientation shown in **Figure 2**. The other end of the flex cable plugs into the target head adapter. The target head adapter then inserts into either a DIP footprint in a target system or into the SOIC adapter.

The MCU package in your target system determines the target cable assembly components required:

- For a 20-pin DIP package (MC68HC(7)05JJx MCUs), use flex cable M68CBL05A and target head adapter M68TA05JJ7P20.
- For a 28-pin DIP package (MC68HC(7)05JPx MCUs), use flex cable M68CBL05A and target head adapter M68TA05JP7P28.
- For a 20-pin SOIC package (MC68HC(7)05JJx MCUs), use the flex cable assembly for the 20-pin DIP in conjunction with SOIC adapter M68DIP20SOIC.
- For a 28-pin SOIC package (MC68HC(7)05JPx MCUs), use the flex cable assembly for the 28-pin DIP in conjunction with SOIC adapter M68DIP28SOIC.







20-PIN DIP

FLEX CABLE:
M68CBL05A
TARGET HEAD ADAPTER:
M68TA05JJ7P20

28-PIN DIP

FLEX CABLE:
M68CBL05A
TARGET HEAD ADAPTER:
M68TA05JP7P28

20-PIN SOIC

FLEX CABLE:
M68CBL05A
TARGET HEAD ADAPTER:
M68TA05JJ7P20
DIP TO SOIC ADAPTER:
M68DIP20SOIC

28-PIN SOIC

FLEX CABLE:
M68CBL05A
TARGET HEAD ADAPTER:
M68TA05JP7P28
DIP TO SOIC ADAPTER:
M68DIP28SOIC

Figure 2. Target Cable Assembly

Connector Information

The connectors on the M68EM05JP7 module provide access to the user mode emulation signals (J2) as well as select internal signals (J1). Connector J2 is used for a cable interface to a user's target system, while connector J1 is used to connect a logic analyzer.

Target Cable Connector Pin Assignments

Figure 3 shows the pin assignments for connector J2. **Table 1** lists signal descriptions for connector J2.

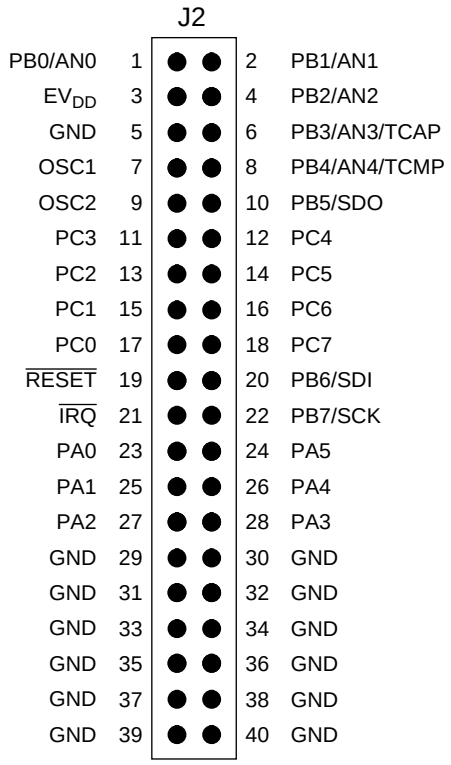


Figure 3. Target Connector Pin Assignments

Table 1. Connector J2 Signal Descriptions

Pin	Mnemonic	Signal
1, 2, 4, 6, 8	PB0/AN0 PB1/AN1 PB2/AN2 PB3/AN3/TCAP PB4/AN4/TCMP	PORT B (bits 0, 1, 2, 3, 4) — General-purpose I/O lines are controlled by software via data direction and data registers. Pins become the AN0, AN1, AN2, AN3, and AN4 lines respectively when the analog subsystem is enabled. PB3 and PB4 become the TCAP and TCMP pins respectively when the programmable timer subsystem is enabled.
3	EV_{DD}	EXTERNAL VOLTAGE DETECT — Connected to target V_{CC}; used to sense target power applied for target status in MMDS05 status window
5, 29-40	GND	GROUND
7	OSC1	TARGET OSCILLATOR 1 — A possible external clock source input for the M68EM05JP7 board; system bus frequency is OSC1 ÷ 2; use of this signal is controlled by jumper header W2.
9	OSC2	OSCILLATOR 2 — Output clock signal. Inversion of the OSC1 clock.
10, 20, 22	PB5/SDO PB6/SDI PB7/SCK	PORT B (bits 5, 6, 7) — General-purpose I/O lines are controlled by software via data direction and data registers. Pins become the SDO, SDI, and SCK lines respectively when the simple serial interface subsystem is enabled.
11, 12, 13, 14, 15, 16, 17, 18	PC3, PC4, PC2, PC5, PC1, PC6, PC0, PC7	PORT C (bits 0–7) — General-purpose I/O lines controlled by software via data direction and data registers. ***NOTE:*** *Port C is bonded out only on the MC68HC705JP7 MCU.*
21	$\overline{IRQ}$	TARGET INTERRUPT REQUEST — Active-low input signal from the target that asynchronously applies an MCU interrupt ***NOTE:*** *The V_{PP} programming voltage should not be applied to this pin. Doing so will damage the development system. Connector P3 is available for programming voltage input.*
19	$\overline{RESET}$	Active-low bidirectional signal to/from the target system is driven low to pull the MCU into reset.
23, 24, 25, 26, 27, 28	PA0, PA5, PA1, PA4, PA2, PA3	PORT A (bits 0, 5, 1, 4, 2, 3) — General-purpose I/O lines are controlled by software via data direction and data registers. Port A has high-current sink capability on all pins and external interrupt capability on bits 0–3.

Logic Analyzer Connector Pin Assignments

Figure 4 shows the pin assignments for logic analyzer connector J1. This connector provides easy access to many of the signals used internally. **Table 2** lists signal descriptions for this connector.

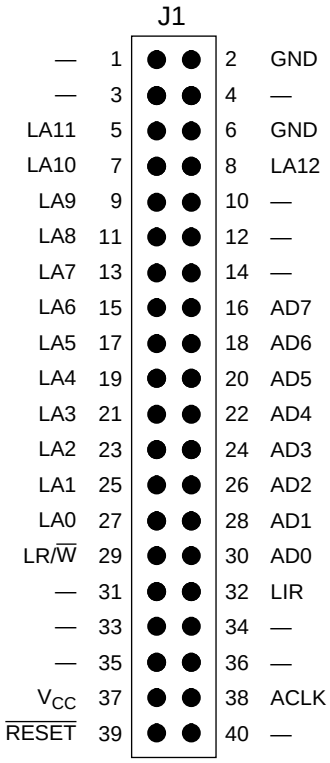


Figure 4. Connector J1 Pin Assignments

Table 2. Logic Analyzer Connector J1 Signal Descriptions

Pin	Mnemonic	Signal
1, 3, 4, 10, 12, 14, 31, 33, 34, 35, 36, 40	NC	No connection
2, 6	GND	GROUND
8	LA12	LATCHED ADDRESS (bit 12) — MCU latched output address bus
5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27	LA11–LA0	LATCHED ADDRESSES (bits 11–0) — MCU latched output address bus
16, 18, 20, 22, 24, 26, 28, 30	AD7–AD0	DATA BUS (bits 7–0) — MCU multiplexed I/O bus
29	LR/$\overline{W}$	LATCHED READ/WRITE — The MCU's write signal is latched and used on the emulator to control emulator memory accesses.
32	$\overline{LIR}$	LOAD INSTRUCTION REGISTER — Active low signal indicating an opcode fetch cycle is in process.
37	V_{CC}	+5 Vdc POWER — Connection to the system voltage V_{CC}
38	ACLK	ANALYZER CLOCK — The latched addresses are valid on the latched address bus at the rising edge of ACLK. Also, data is valid on the AD BUS at ACLK's rising edge.
39	$\overline{RESET}$	RESET — Active-low signal; will be asserted during internally or externally caused resets

MMDS/MMEVS Configuration and Operation

Contents

Introduction

The following paragraphs explain how to configure and use your M68EM05JP7 as part of an MMDS or MMEVS system. For other parts of system installation and configuration, see either the *MMDS0508 Operations Manual* (MMDS0508OM/D) or *MMEVS05/MMEVS08 Operations Manual* (MMEVS0508OM/D).

The topics covered in this chapter are:

- **Setting M68EM05JP7 Jumper Headers** on page 21 explains how to set the M68EM05JP7 jumper headers.
- **Remaining System Installation** on page 25 covers the final steps to system installation.
- **Setting Emulation Voltage** on page 26 explains how to adjust the MC68HC705JP7 MCU operating voltage.
- **Personality Files Usage** on page 27 discusses the personality file used on the M68EM05JP7 board.
- **Personality EPROM Programming** on page 27 covers programming procedures for the 64-bit personality EPROM.
- **Emulation Specifics** on page 29 explains special considerations for emulating with this module.

NOTE: *You can configure an M68EM05JP7 already installed in the system platform board. To do so, remove system power and then follow the guidance of this chapter.*

CAUTION: *Be sure to switch off power before you reconfigure an installed EM. Reconfigure EM jumper headers with the power on can damage emulation circuits.*

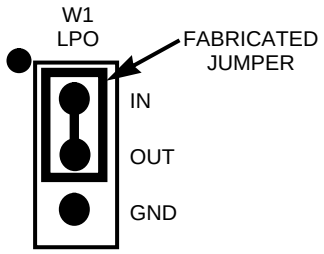
Setting M68EM05JP7 Jumper Headers

Your M68EM05JP7 has five jumper headers — W1 through W5. The following explains how to configure these components.

Internal Clock Control Header, W1

The internal clock control header provides access to the emulated internal low-power oscillator (LPO) frequency generated by the Y1 crystal circuit. The LPO on the M68EM05JP7 module operates at 500 kHz, the nominal LPO frequency. The LPO frequency passes through jumper header W1 and gives the user the ability to supply an alternate LPO frequency. To use an alternate internal clock source, remove the fabricated jumper from W1 and connect the source to the OUT pin of header W1. A digital ground connection is available at the GND pin.

NOTE: *The user-supplied LPO source should be a CMOS level square wave.*



External Clock Source Select Header, W2

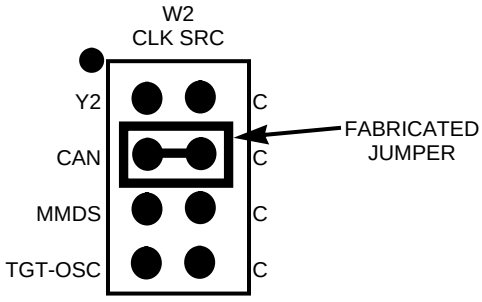
Jumper header W2 determines the source of the external clock signal. The diagram here illustrates the jumper header where the pins marked C indicate common pins. The default configuration selects the 4-MHz canned oscillator clock source (at board location XY3).

There are three other possible sources for the external clock. One source, from the platform board, requires repositioning the W2 jumper between pins MMDS and C and then using the system's OSC command to select a frequency.

For a user-supplied clock source, coming through a target cable connected to J2, reposition the W2 jumper between pins TGT_OSC and C.

NOTE: *The user-supplied source through the target cable should be a CMOS level square wave.*

The fourth possible external clock source is a user-supplied crystal oscillator circuit. The M68EM05JP7 has been designed with an unpopulated crystal circuit. For this source, reposition the W2 jumper between pins Y2 and C and supply the components for the Y2 crystal circuit. The IC device at location U1 is an 74HCU04 inverter and provides the inverter for a standard single inverter oscillator. The user supplies the appropriate crystal, resistors, and capacitors for operating the external clock at a particular frequency. See **M68EM05JP7 Schematics (Sheet 4 of 7)** on page 39 for schematic details of the crystal circuit.

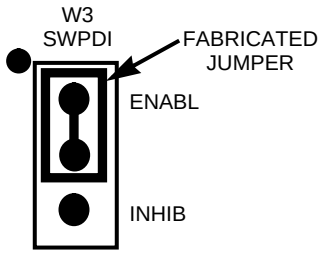


NOTE: *To use any of the external clock sources, the external pin oscillator must be selected as the MCU clock source through manipulation of the OM2:OM1 bits in the IRQ status and control register (ISCR)*

SWPDI Mask Option Control Header, W3

Jumper header W3 controls the software pulldown inhibit mask option for port A. With the jumper in the ENABL position, the mask option bit is clear and the port A pulldowns can be controlled via software. With the jumper in the INHIB position, the mask option is set and the port A pulldowns are inhibited.

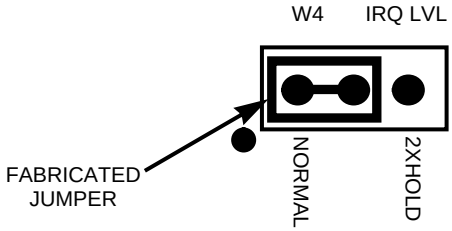
NOTE: *The port B pulldowns are not controlled by this jumper. They are controlled by what is programmed in the SWPDI bit of the mask option register in the resident MC68HC705JP7 MCU.*



$\overline{IRQ}/V_{PP}$ Level Control Header, W4

When the resident MC68HC705JP7 is in reset, the $\overline{IRQ}/V_{PP}$ voltage level is at the voltage determined by $\overline{IRQ}/V_{PP}$ source control header W5. The $\overline{IRQ}/V_{PP}$ level control header W4 controls the voltage level the $\overline{IRQ}/V_{PP}$ pin will be at during routine operation when the external $\overline{IRQ}$ is not asserted and the part is not in reset. If jumper header W4 is in the NORMAL position, the $\overline{IRQ}/V_{PP}$ level will drop to the MCU operating voltage once the part comes out of reset. If jumper header is in the 2XHOLD position, the $\overline{IRQ}/V_{PP}$ level will be held at the voltage determined by $\overline{IRQ}/V_{PP}$ source control header W5.

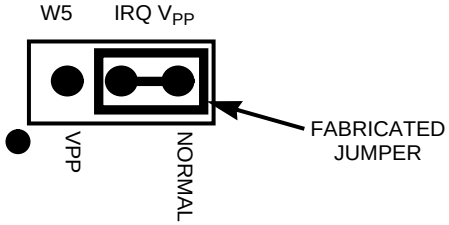
NOTE: *The W4 jumper header should be in the 2XHOLD position for personality EPROM programming only.*



$\overline{IRQ}/V_{PP}$ Source Control Header, W5

Jumper header W5 determines the source for high voltage applied to the $\overline{IRQ}/V_{PP}$ pin. In the NORMAL position, the voltage is supplied from the development systems charge pump (~12 V). In the V_{PP} position, the voltage is supplied from the user through lever terminal connector P3.

NOTE: *The W5 jumper header should be in the V_{PP} position for personality EPROM programming only.*



Remaining System Installation

When you have configured headers W1–W5, M68EM05JP7 configuration is completed. At that time, make sure of these points:

- Ensure that the power to the development tool is off.
- Remove the panel from the station module top, if installing the M68EM05JP7 in an MMDS station module.
- Fit together EM connectors P1 and P2 on the bottom of the board and platform board DIN connectors. Snap the corners of the EM onto the plastic standoffs.
- Connect the target cable, if appropriate.
- Replace the panel, if installing in an MMDS.

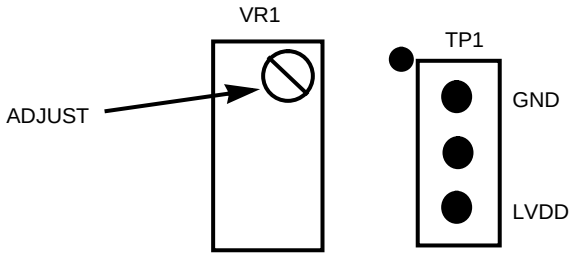
At this point, you are ready to make remaining cable connections, as necessary, and restore power.

For instructions, consult either the *MMEVS05/MMEVS08 Operations Manual* (MMEVS0508OM/D) or *MMDS0508 Operations Manual* (MMDS0508OM/D).

Setting Emulation Voltage

The M68EM05JP7 module has an on-board voltage regulator that can be adjusted to provide low-voltage emulation in the 3.0 V to 5.0 V range. The adjustment for that variable voltage is variable resistor VR1. Test point TP1 is used for connection to a voltmeter during voltage adjustment.

To adjust the MCU operating voltage, first ensure that no target cable is connected to target cable connector J2. Then connect a voltmeter across the GND and LVDD pins of test point header TP1 and adjust variable resistor VR1 to the desired voltage level. Make sure that the target system's operating voltage is at the newly adjusted level before connecting target signals through the J2 connector.



Personality Files Usage

The development system uses a specific personality file to emulate MC68HC(7)05JJx and MC68HC(7)05JPx MCU devices: file 0002BVxx.MEM. The debugger software loads this personality file upon power up. The file is on an individual disk shipped with the M68EM05JP7.

NOTE: *Note that personality file names follow the pattern 00ZZZVxx.MEM, where ZZZ is the EM identifier or MCU name and xx is the version of the file.*

Personality EPROM Programming

The MC68HC705JP7 and MC68HC705JJ7 MCUs have a 64-bit personality EPROM (PEPROM) that is controlled through MCU registers and the $\overline{IRQ}/V_{PP}$ voltage. To program this array on the resident MCU, the user must write or obtain code that will modify the array correctly.

NOTE: *The MC68HC05JJ6 MCU does not have the personality EPROM. When emulating the MC68HC05JJ6 MCU, user code should not manipulate the PEPROM status and control register (PEBSR) or the PEPROM bit select register (PEBSR).*

Refer to the general release specification for proper programming sequence. The required programming voltage must be supplied by the user through lever terminal connector P3. Proper configuration of jumper headers W4 and W5 is also required.

The following sequence shows how to program the PEPROM:

1. Ensure that power to the development system is off.
2. On the M68EM05JP7 emulation module, set jumper header W4 to the 2XHOLD position and the W5 jumper header to the VPP position.
3. On the M68EM05JP7 emulation module, make connections to P3 to supply the required programming voltage. Do not turn the V_{PP} supply voltage on.
4. Turn on power to the development system.
5. Turn on the V_{PP} supply voltage. At this point, the proper programming voltage is applied to the resident MCU.
6. Start running debugger software.
7. Load and execute the necessary code to program the PEPROM.
8. Once the PEPROM programming is complete, exit the debugger software.
9. Remove V_{PP} source voltage from connector P3.
10. Turn off development system power.
11. Reposition jumper headers W4 and W5 to the normal position.

NOTE: *To program the PEPROM, V_{DD} must be greater than 4.5 Vdc.*

CAUTION: *To avoid damaging emulator circuits, the development system voltage must be turned on before you supply the V_{PP} source voltage through the P3 connector. Also, the source voltage should be removed from P3 before turning off the development system voltage.*

Emulation Specifics

The following paragraphs detail differences between the performance of MC68HC(7)05JPx and MC68HC(7)05JJx MCUs run in single-chip operation and how certain features will perform during emulation.

$\overline{IRQ}/V_{PP}$ Input Pin

In single-chip mode operation:

The $\overline{IRQ}/V_{PP}$ pin drives the asynchronous IRQ interrupt function of the CPU. The pin is also used for programming voltage when programming the personality EPROM, the user EPROM, or the MOR.

In emulation:

The $\overline{IRQ}/V_{PP}$ signal supplied to connector J2 through a target cable drives only the asynchronous IRQ interrupt function.

A V_{PP} voltage should not be supplied to the $\overline{IRQ}/V_{PP}$ pin in a target application while the emulator is connected. Connector P3 is available for V_{PP} programming voltage input.

Pullup on $\overline{IRQ}$

In single-chip mode operation:

There is no pullup on the $\overline{IRQ}$ pin. Your application must pull the $\overline{IRQ}$ pin to V_{DD} level to prevent interrupts.

In emulation:

The $\overline{IRQ}$ pin is pulled up on the module. Be aware that an application without the $\overline{IRQ}$ pin pulled high will emulate correctly but will fail in the application because of a floating IRQ line. The $\overline{IRQ}$ pin pulled high on the module causes these results.

Personality EPROM

In single-chip mode operation:

The MC68HC05JJ6 does not have a personality EPROM and accesses to the PEPROM registers are undefined.

In emulation:

The MC68HC05JJ6 device is emulated with a MC68HC705JP7 device resident on the M68EM05JP7 module. For accurate emulation, the PEPROM registers should not be accessed when emulating the MC68HC05JJ6 MCU.

Mask Option Register (MOR) Control

In single-chip mode operation:

The MCU mask options will be determined by which options have been programmed in the MOR EPROM location of the resident MC68HC705JP7 MCU. This register must be programmed using a dedicated programmer.

In emulation:

Like single-chip, the mask option register should be programmed to the desired value using a dedicated programmer prior to insertion in the M68EM05JP7 module. The exception is the SWPDI mask option, which is detailed in **SWPDI Mask Option Bit**.

SWPDI Mask Option Bit

In single-chip mode operation:

The software programmable pulldown inhibit option is determined by what has been programmed in the mask option register (MOR). If the bit is set, all I/O pulldowns are inhibited.

In emulation:

The programmed software programmable pulldown inhibit option only controls the pulldowns for port B. The port A and port C pulldown inhibit option is emulated with jumper header W3.

NOTE: *Port C is bonded out only on the MC68HC705JP7 MCU.*

Schematics

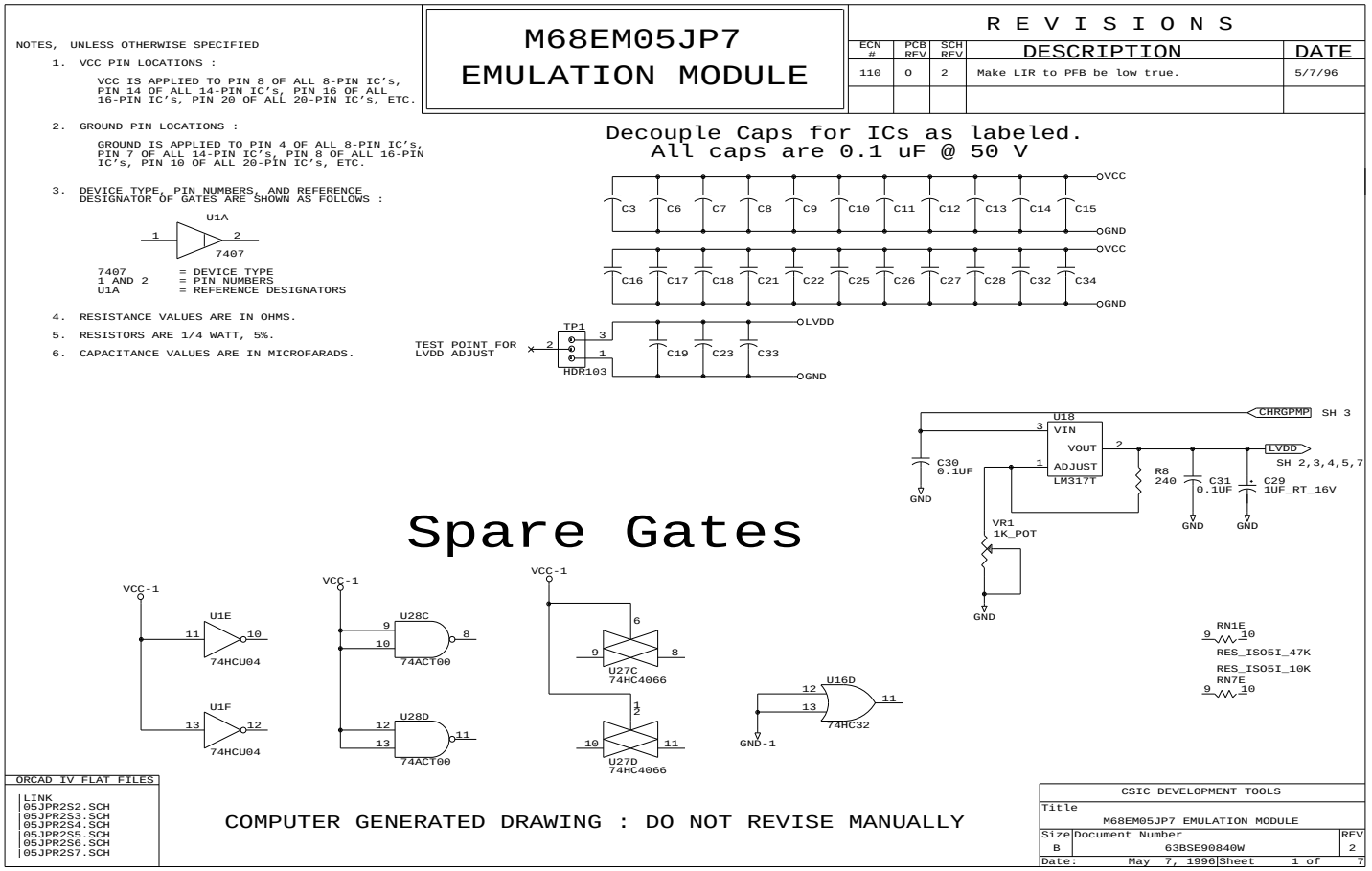
Contents

M68EM05JP7 Schematics

Refer to the following pages for the seven sheets of schematics for the M68EM05JP7 emulation module.

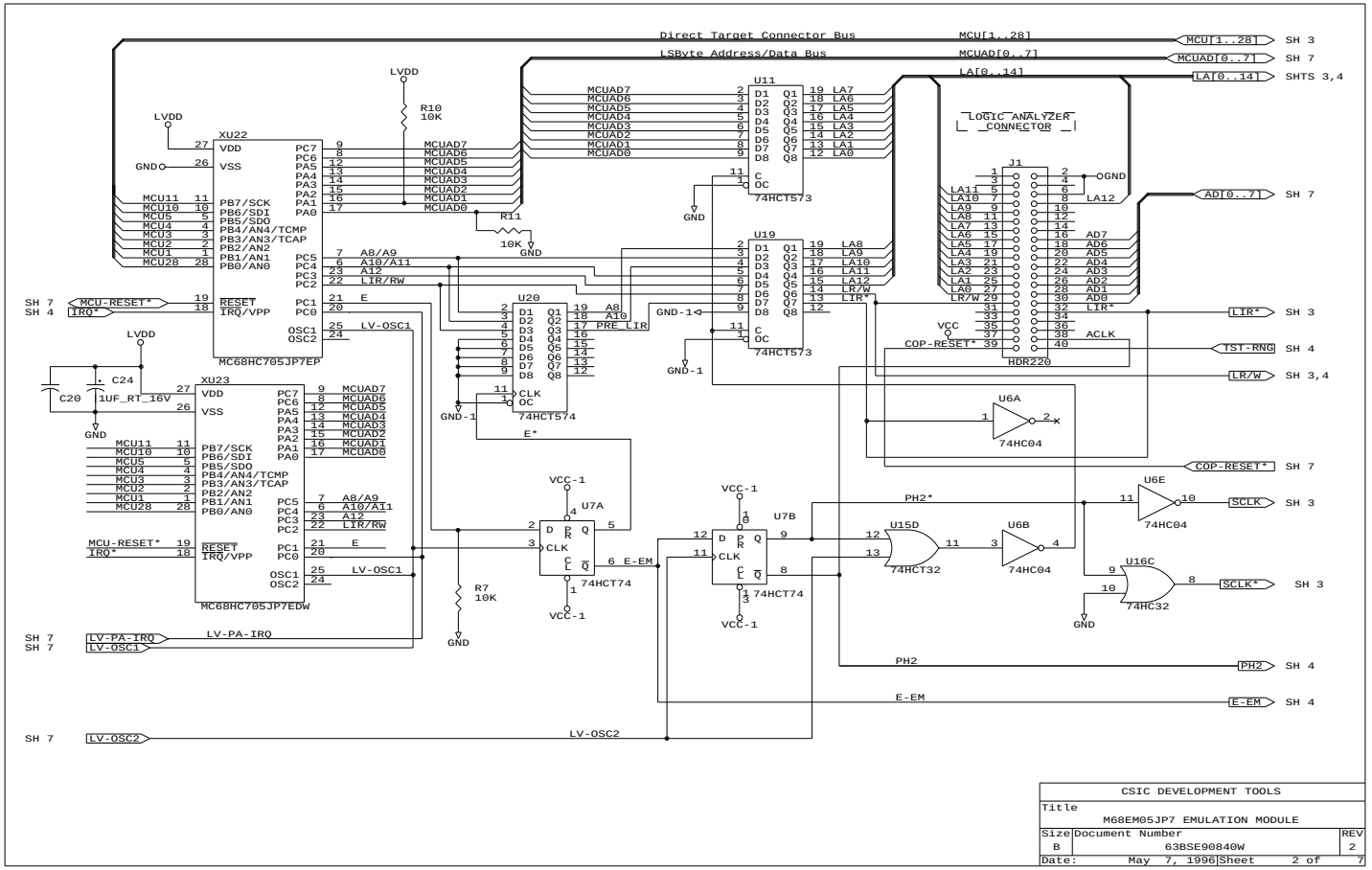
Schematics

M68EM05JP7 Schematics (Sheet 1 of 7)



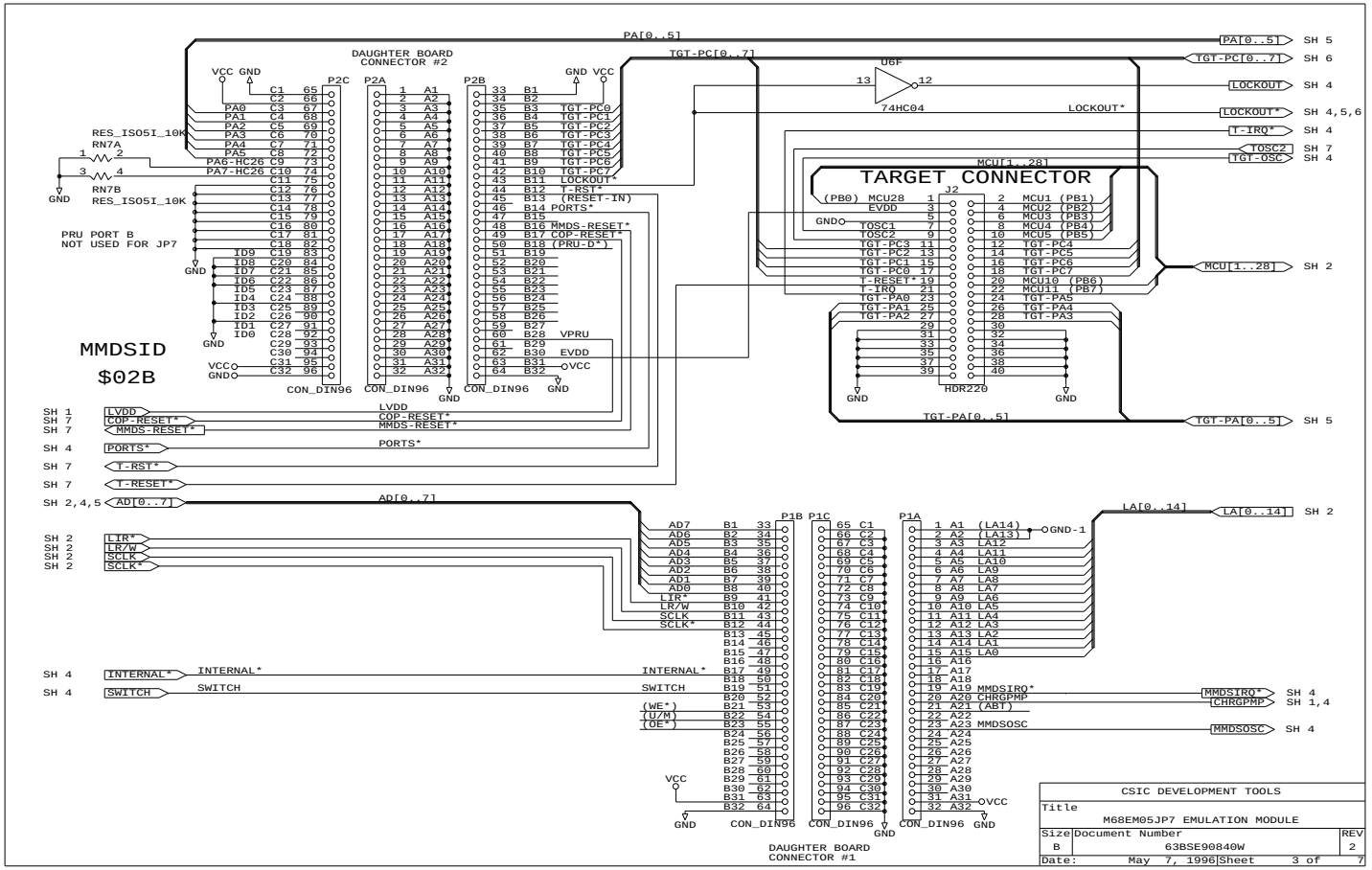
Schematics

M68EM05JP7 Schematics (Sheet 2 of 7)



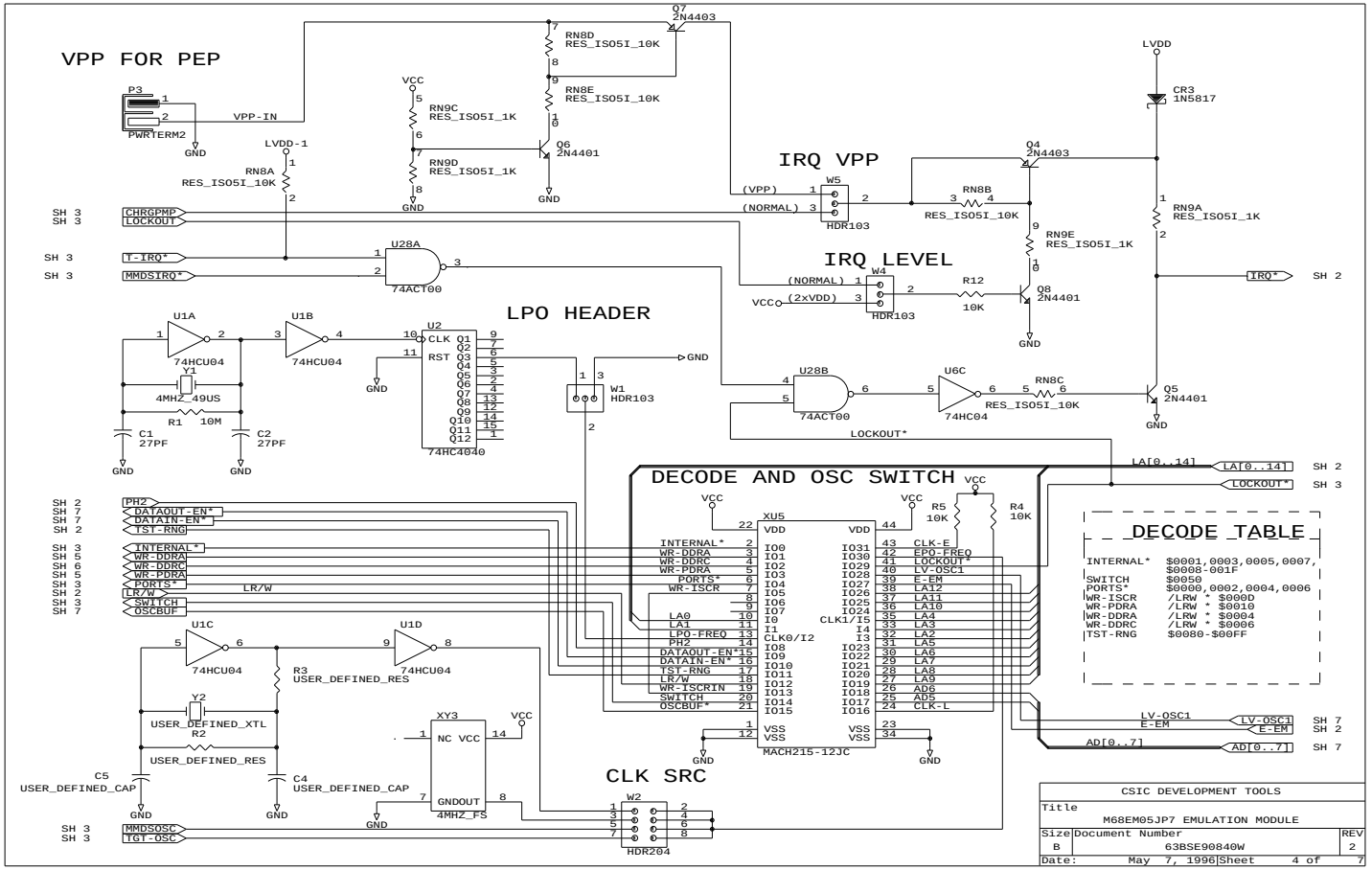
Schematics

M68EM05JP7 Schematics (Sheet 3 of 7)



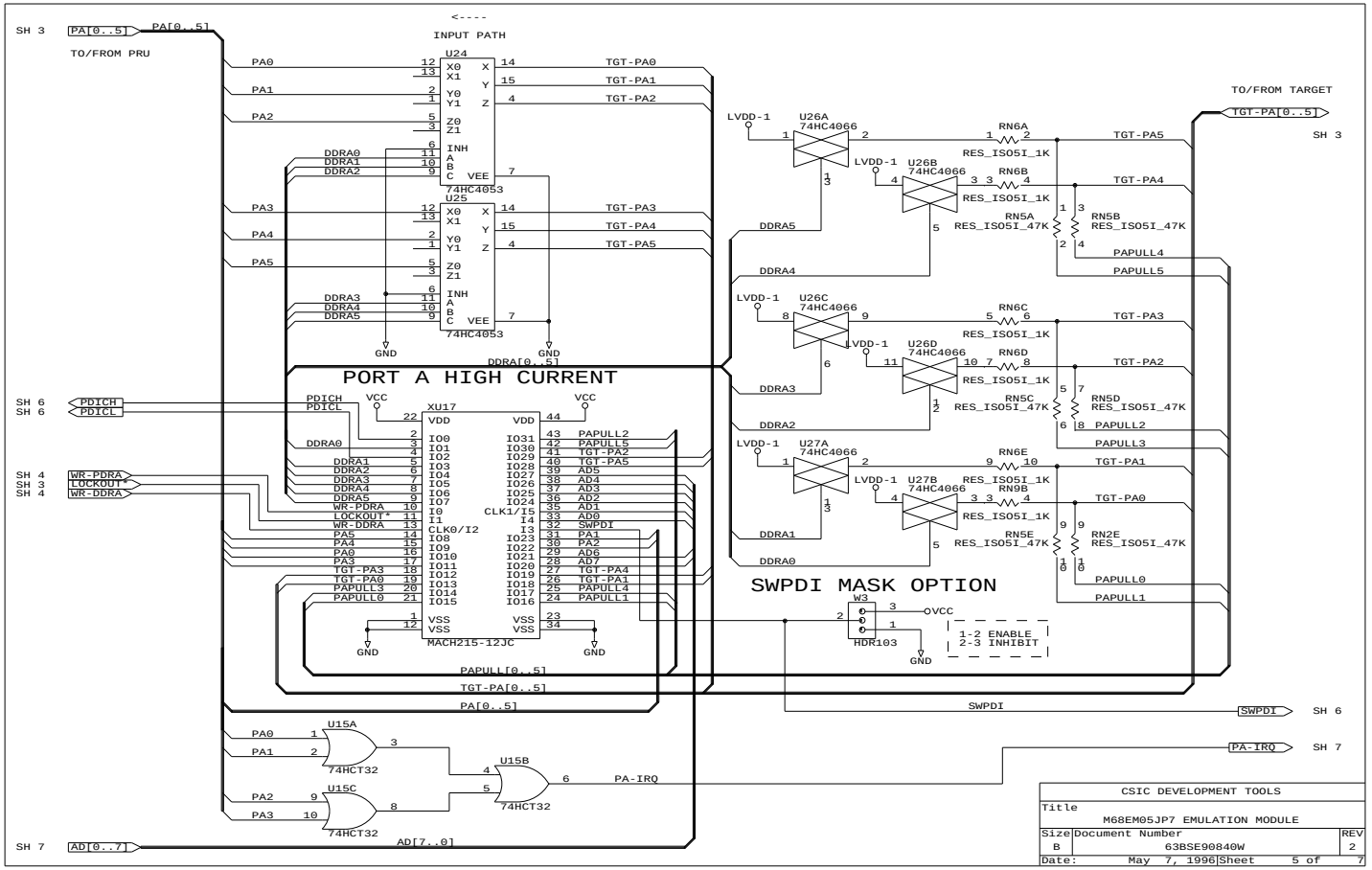
Schematics

M68EM05JP7 Schematics (Sheet 4 of 7)



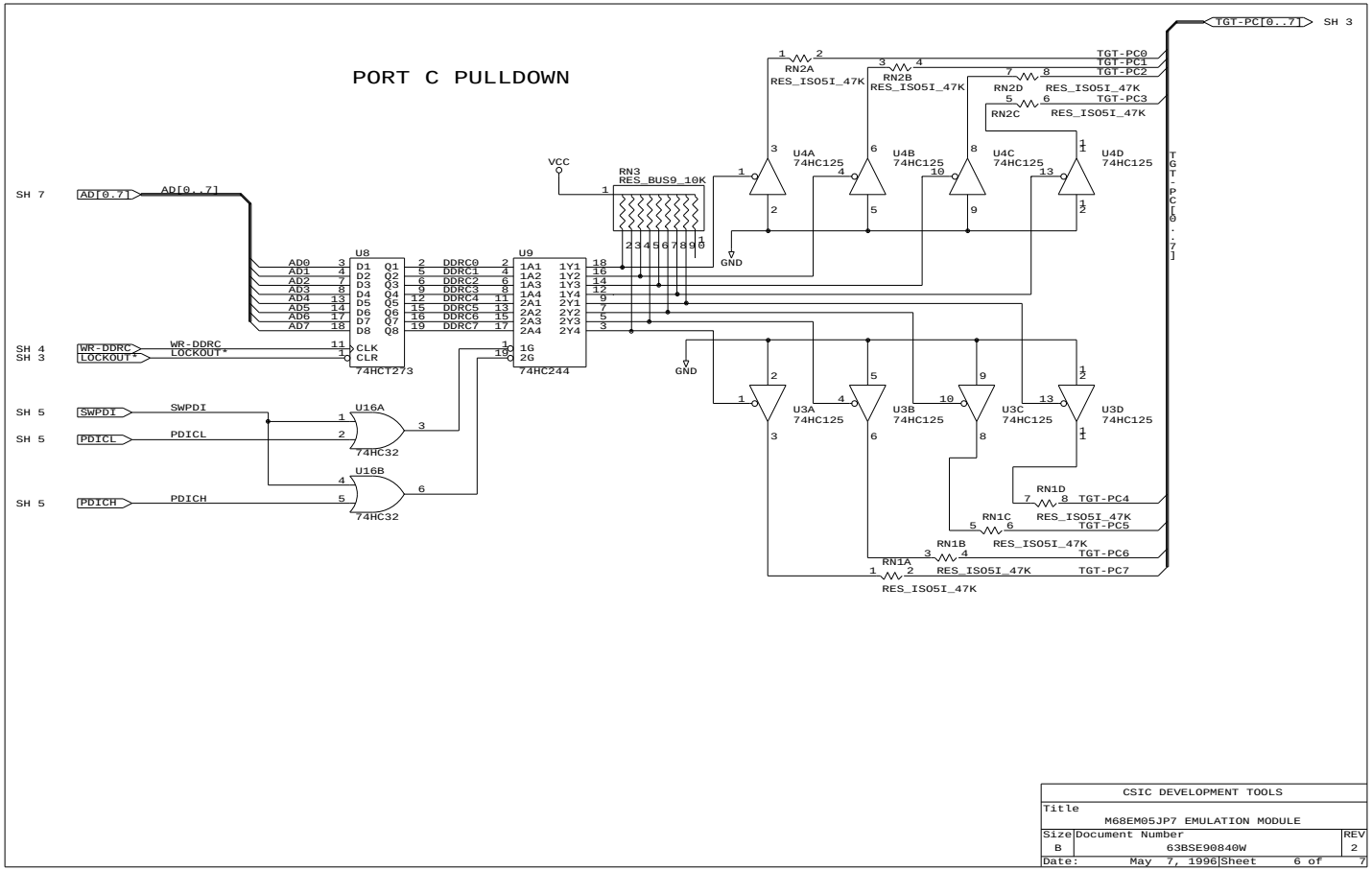
Schematics

M68EM05JP7 Schematics (Sheet 5 of 7)



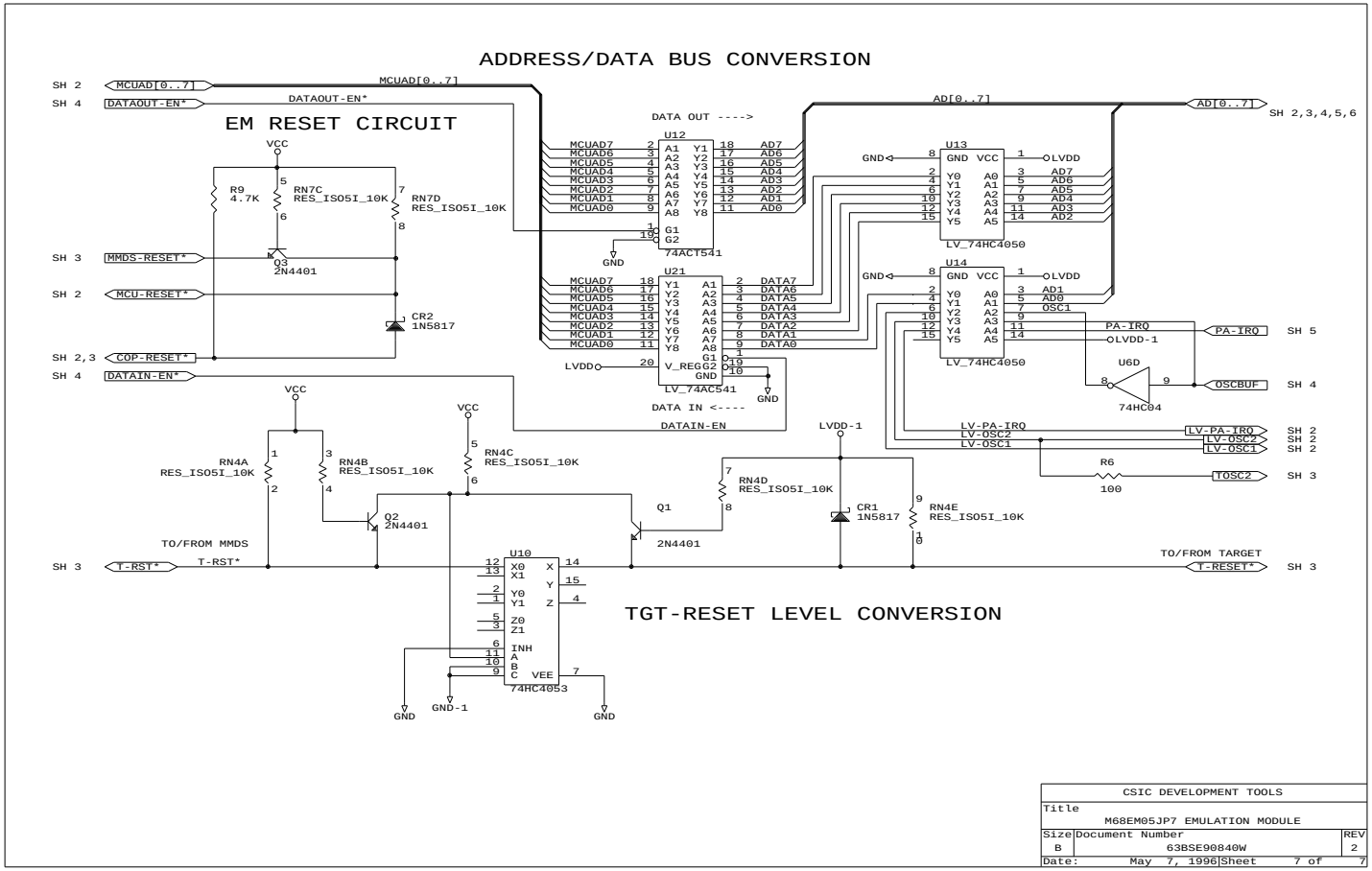
Schematics

M68EM05JP7 Schematics (Sheet 6 of 7)



Schematics

M68EM05JP7 Schematics (Sheet 7 of 7)



Schematics

How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.1-800-441-2447 or 602-303-5454

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE 602-244-6609

INTERNET: http://Design-NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-81-3521-8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298