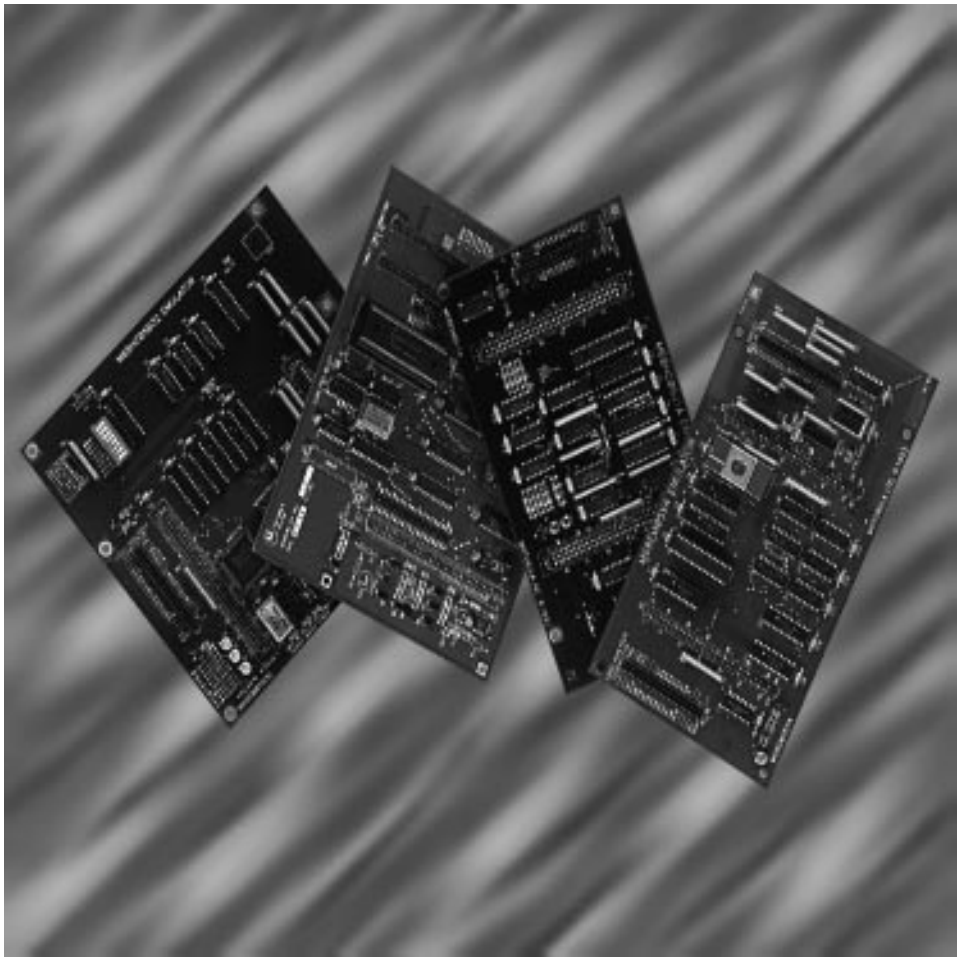
M68EM05P18UM/D

M68EM05P18

EMULATION MODULE
USER'S MANUAL



MOTOROLA

M68EM05P18

Emulation Module
User's Manual

Revision History

This table summarizes differences between this revision and the previous revision of this emulation module user's manual.

Previous Revision	None
Current Revision	Original release
Date	06/96

Revision History

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Introduction

Your M68EM05P18 gives your Motorola development tool the ability to emulate target systems based on the MC68HC805P18 and MC68HC05P18 microcontroller units (MCUs). By substituting a different emulation module (EM), you can enable your Motorola development tool to emulate other MCUs. Refer to *Motorola's Development Tool Selector Guide*, order number SG173/D, for a complete list of available EMs.

This hardware user's manual explains connection, configuration, and operation information specific to the M68EM05P18 emulation module. The module can be installed in any of three Motorola development systems. To configure your M68EM05P18 for use as part of an MMDS05 or an MMEVS05/MMEVS08, follow the instructions given in **MMDS/MMEVS Configuration and Operation** on page 19. To configure your M68EM05P18 for use as part of an HC05EVS, follow instructions given in **HC05EVS Configuration and Operation** on page 31.

Emulation Components

Motorola's complete emulation system consists of the emulation module described in this manual as well as other separately purchased options described in the following paragraphs.

These items are included with the M68EM05P18 emulation module:

- **An M68EM05P18 emulation module (EM)** — the printed circuit board that enables system functionality for MC68HC805P18 and MC68HC05P18 MCUs. The female connectors, on the bottom of the module, mate with male connectors on a development system platform board. The EM also has a connector for the target cable assembly.
- **Configuration software** — 3 1/2-inch diskette containing personality files for this module.

Separately purchased Motorola modular development tool options include:

- **An MMEVS platform board (M68MMPFB0508)** — The MMEVS is an economical development tool that provides real-time in-circuit emulation. The unit's integrated design environment includes an editor, an assembler, a user interface, and a source-level debugging program.
- **An MMDS05 modular development system (MMDS05)** — The MMDS is a high-performance development tool that has all the capabilities of the MMEVS. In addition, it also has a bus state analyzer and real-time memory windows.
- **An HC05EVS platform board (M68HC05EVS) evaluation system** — An M68HC05EVS is a tool for designing and evaluating target systems. This system is being replaced by the more advanced MMEVS.
- Flex cable target assembly — Refer to **Target Cable Assemblies** on page 13 for more information.

User supplied components include:

- **Host computer** — See the appropriate development tool user’s manual for minimum requirements.
- **Power supply** — +5 Vdc required for the MMEVS and the EVS

Emulation Module Layout

Figure 1 shows the layout of the M68EM05P18. W1 selects the clock-signal source. Jumper header W2 controls the path of a target reset.

Target connector J2 is the interface to a target system and uses a separately purchased target cable assembly. When you install the M68EM05P18 on the MMDS05, the target cable passes through the slit in the station module enclosure. Connector J1 is used as a connection to a logic analyzer. DIN connectors P1 and P2 connect the EM and a development system platform board.

Location XU5 is the resident MCU. Switch SW1 enables or disables port A mask options. A wirewrap area is at the lower right corner of the M68EM05P18 board.

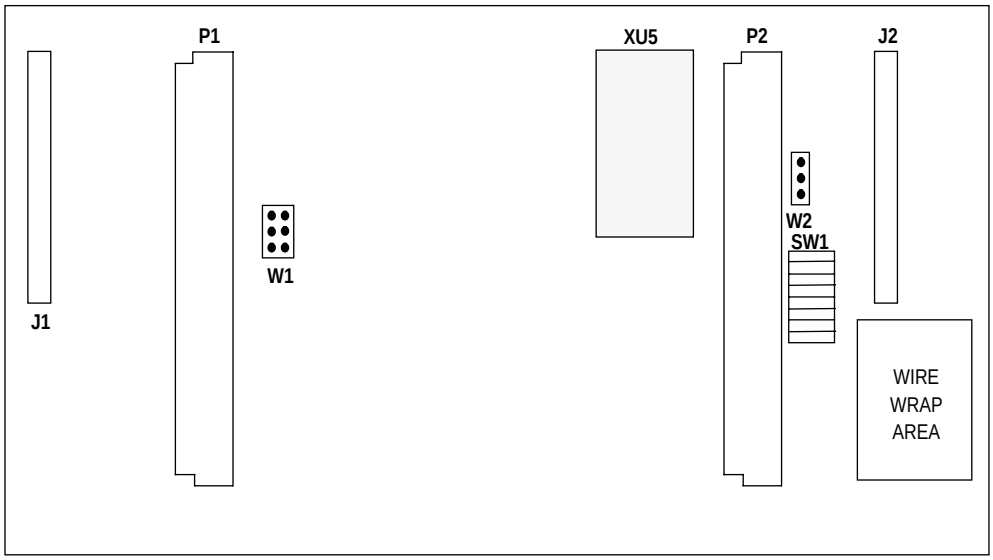


Figure 1. M68EM05P18 Emulation Module

Target Cable Assemblies

To connect your M68EM05P18 to a target system, you need a separately purchased target cable assembly. Cable assemblies support both MC68HC805P18 and MC68HC05P18 emulation and are available for two MCU packages: dual in-line plastic (DIP) and small outline integrated circuit (SOIC).

The target cable connects to the emulator via connector J2 on the M68EM05P18 emulation module. Pin assignments and signal descriptions for connector J2 can be found in **Target Cable Connector Pin Assignments** on page 15.

The drawings in **Figure 2** represent a target cable assembly. An assembly for 28-pin DIP packages consists of a flex cable and a target head adapter. The assembly for 28-pin SOIC packages requires an additional SOIC adapter. One end of the flex cable plugs onto M68EM05P18 connector J2 with orientation shown in **Figure 2**. The other end of the flex cable plugs into the target head adapter. The target head adapter then inserts into either a DIP footprint in a target system or into the SOIC adapter.

The MCU package in your target system determines the target cable assembly components required:

- For a 28-pin DIP package, use flex cable M68CBL05A and target head adapter M68TA05P9P28.
- For a 28-pin SOIC package, use the flex cable assembly for the 28-pin DIP in conjunction with SOIC adapter M68DIP28SOIC.

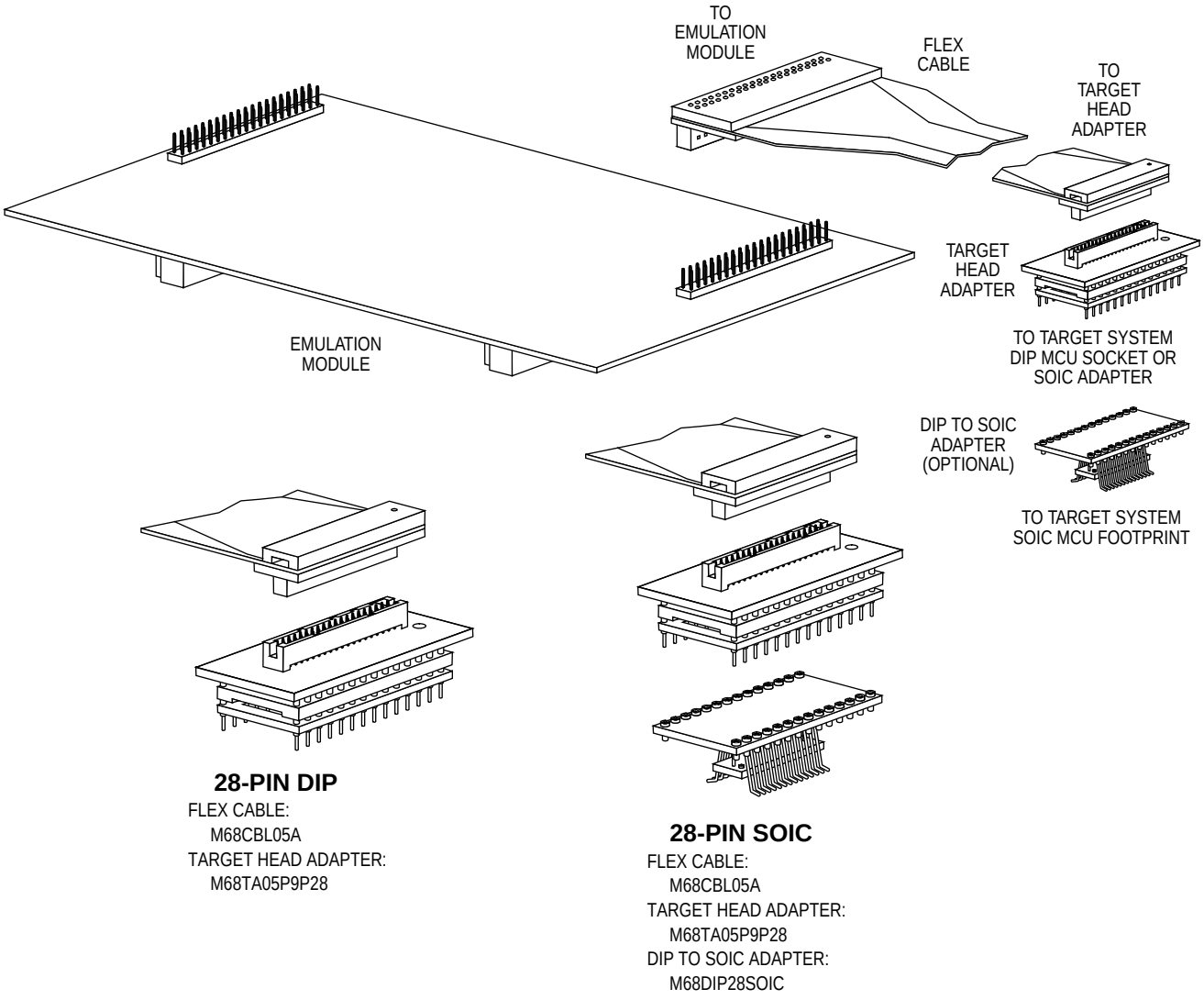


Figure 2. Target Cable Assembly

Connector Information

The connectors on the M68EM05P18 module provide access to the user mode emulation signals (J2) as well as select internal signals (J1). Connector J2 is used for a cable interface to a user's target system, while connector J1 is used to connect a logic analyzer.

Target Cable Connector Pin Assignments

Figure 3 shows the pin assignments for connector J2. **Table 1** lists signal descriptions for connector J2.

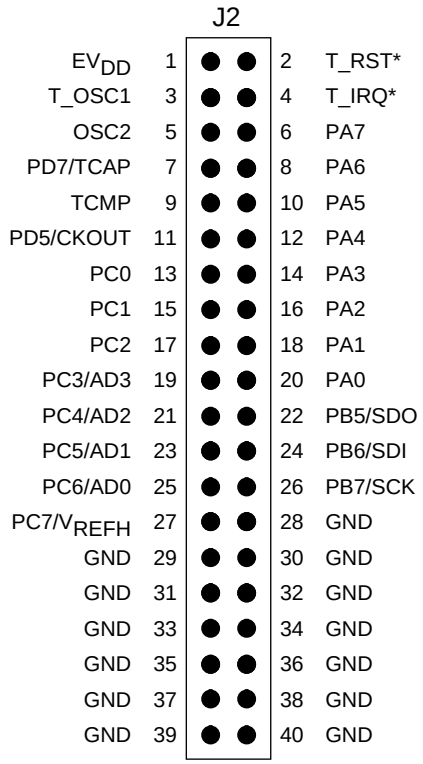


Figure 3. Target Connector Pin Assignment

Table 1. Connector J2 Signal Descriptions

Pin	Mnemonic	Signal
1	EV_{DD}	EXTERNAL VOLTAGE DETECT — V_{DD} input signal from the target used by the emulator to detect target system voltage
2	T_RST*	TARGET RESET — Active-low input signal that starts a system reset
3	T_OSC1	TARGET OSCILLATOR 1 — A possible clock source input for the M68EM05P18 board. System bus frequency is OSC1 ÷ 2. Use of this signal is controlled by jumper header W1.
4	T_IRQ*	TARGET INTERRUPT REQUEST — Active-low input signal from the target that asynchronously applies an MCU interrupt
5	OSC2	OSCILLATOR 2 — Output clock signal at two times the internal bus frequency
6, 8, 10, 12, 14, 16, 18, 20	PA7–PA0	PORT A (bits 7–0) — General-purpose I/O lines controlled by software via data direction and data registers
7	PD7/TCAP	PORT D (bit 7) — General-purpose input-only line TIMER CAPTURE — Input signal used by the input capture feature of the MCU programmable timer system
9	TCMP	TIMER COMPARE — Output signal used by the output compare feature of the MCU programmable timer system
11	PD5/CKOUT	PORT D (bit 5) — General-purpose I/O line controlled by software via data direction and data registers CLOCK OUTPUT — If the clock output mask option is enabled, this pin will become the buffered OSC2 clock.
13, 15, 17	PC0–PC2	PORT C (bits 0–2) — General-purpose I/O lines controlled by software via data direction and data registers
22, 24, 26	PB5–PB7 / SDO, SDI, SCK	PORT B (bits 5–7) — General-purpose I/O lines controlled by software via data direction and data registers. SIOP SIGNALS — If the serial I/O port (SIOP) is enabled, these pins are the serial communications pins. Pin 22 is the serial data output (SDO), pin 24 is the serial data input (SDI), and pin 26 is the serial clock (SCK).
19, 21, 23, 25, 27	PC3–PC7 / AD3–AD0, V_{REFH}	PORT C (bits 3–7) — General-purpose I/O lines controlled by software via data direction and data registers A/D INPUTS — If the analog-to-digital (A/D) subsystem is enabled, then the pins become A/D inputs. Pins 19, 21, 23, and 25 become A/D channels 3, 2, 1, and 0, respectively. Pin 27 is voltage reference high (V_{REFH}).
28–40	GND	GROUND

Logic Analyzer Connector Pin Assignments

Figure 4 shows the pin assignments for logic analyzer connector J1. This connector provides easy access to many of the signals used internally. **Table 2** lists signal descriptions for this connector.

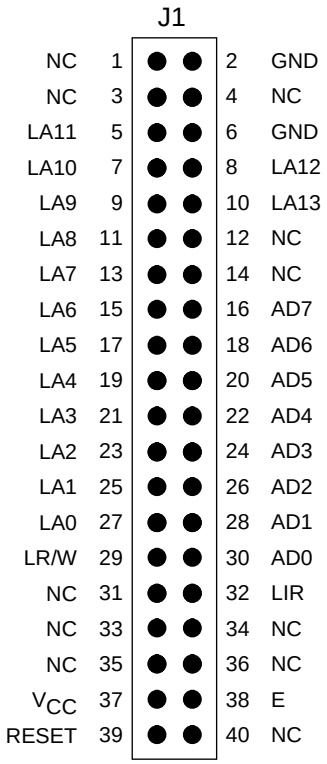


Figure 4. Connector J1 Pin Assignments

Table 2. Logic Analyzer Connector J1 Signal Descriptions

Pin	Mnemonic	Signal
1, 3, 4, 12, 14, 31, 33, 34, 35, 36, 40	NC	No connection
2, 6	GND	GROUND
5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27	LA11–LA0	LATCHED ADDRESSES (bits 11–0) — MCU latched output address bus
10, 8	LA13, LA12	LATCHED ADDRESSES (bits 13–12) — MCU latched output address bus
16, 18, 20, 22, 24, 26, 28, 30	AD7–AD0	ADDRESS/DATA BUS (bits 7–0) — MCU multiplexed address/data bus
29	LR/W	LATCHED READ/WRITE — The MCU's write signal is latched and used on the platform board to control emulator memory accesses.
32	LIR	LOAD INSTRUCTION REGISTER — Active-low signal indicating an opcode fetch cycle is in process
37	V_{CC}	+5 Vdc POWER — Connection to the system voltage V_{CC}
38	E	E CLOCK — Internally generated clock signal used as a timing reference. The frequency of E is 1/2 the frequency of input clock OSC1.
39	RESET	RESET — Active-low signal will be asserted during internally or externally caused resets.

MMDS/MMEVS Configuration and Operation

Contents

Introduction

The following paragraphs explain how to configure and use your M68EM05P18 as part of an MMDS or MMEVS system. For other parts of system installation and configuration, see either the *MMDS05 Operations Manual* (MMDS05OM/D) or *MMEVS05/MMEVS08 Operations Manual* (MMEVS0508OM/D). If you use your M68EM05P18 as part of an HC05EVS, refer to **HC05EVS Configuration and Operation** on page 31 for corresponding information.

The topics covered in this chapter are:

- **Setting M68EM05P18 Jumper Headers and Switches** on page 21 explains how to set the M68EM05P18 jumper headers.
- **Remaining System Installation** on page 25 covers the final steps to system installation.
- **Personality File Usage** on page 26 discusses how the personality file is used on the M68EM05P18 board.
- **MC68HC(8)05P18 Emulation** on page 26 explains considerations pertaining to the MCU you emulate.

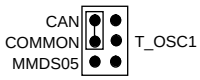
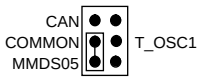
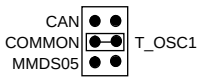
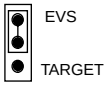
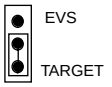
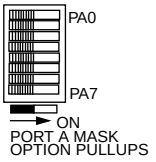
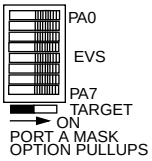
NOTE: *You can configure an M68EM05P18 already installed in the system platform board. To do so, remove system power and then follow the guidance of this chapter.*

CAUTION: *Be sure to switch off power before you reconfigure an installed EM. Reconfiguring EM jumper headers with the power on can damage emulation circuits.*

Setting M68EM05P18 Jumper Headers and Switches

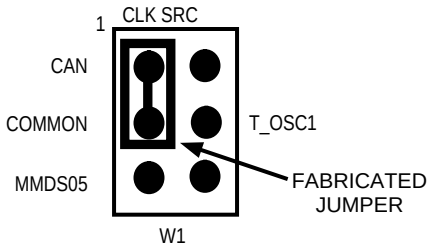
Your M68EM05P18 has two jumper headers — W1 and W2 — and an 8-position DIP switch, SW1, for the port A pullup/interrupt mask options. **Table 3** provides a quick reference for configuration options. Refer to the paragraphs that follow for a more detailed explanation.

Table 3. Jumper Header and Switch Positions for MMDS/MMEVS

Jumper/ Switch	Position	Description	Factory Setting
Clock Source Select, W1		Select the 4-MHz canned oscillator located on the EM board at XY1.	X
		Select the clock originating from the development system platform board. The frequency is controlled by the OSC command and is 2 MHz on power up.	
		Selects a user supplied clock source. The clock is input to connector J2 through a target cable assembly.	
Reset Select, W2		Always in this position for MMDS or MMEVS operation. Enables software to control bidirectional reset.	X
		Not applicable on MMDS or MMEVS	
Port A Interrupt Mask Option Control, SW1		Each port A bit is individually configurable. In the left position, the option is **not** selected.	X
		In the right position, the option **is** selected.	

Clock Source Select Header, W1

Jumper header W1 determines the clock-signal source. This diagram illustrates the jumper header where the pin marked COMMON is always connected to one of the three clock source pins via the fabricated jumper. The default configuration, between CAN and COMMON, selects the 4-MHz canned oscillator clock source (at board location XY1).



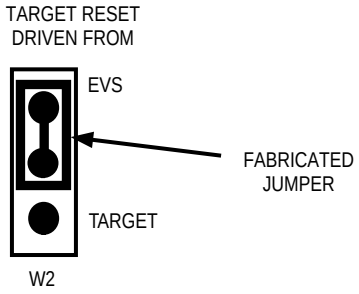
There are two other possible clock sources. To use the one originating from the development system platform, reposition the W1 jumper header between the MMDS05 and COMMON pins. Then use the system's OSC command to select a frequency.

For a user supplied clock source coming through the target cable connected to J2, reposition the W1 jumper header between the T_OSC1 and COMMON pins.

NOTE: *The user supplied source through the target cable should be a CMOS level square wave.*

Reset Select Header, W2

Jumper header W2 controls the path of a target reset. The diagram here shows the factory configuration: The fabricated jumper in the EVS position enables the emulation software to control the direction of resets. This is the only correct W2 configuration for an M68EM05P18 that is part of an MMDS or MMEVS.

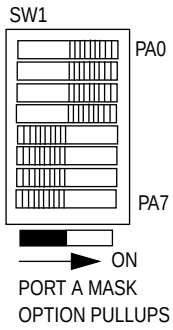


NOTE: *The TARGET configuration is not correct for an M68EM05P18 that is part of an MMDS or MMEVS. Such a configuration would interfere with correct operation of the RESETIN and RESETOUT commands.*

Port A Interrupt Mask Option Control Switch, SW1

The eight positions of switch SW1 enable or disable the port A interrupt mask options. Each position controls one port A line. A switch in the left position, OFF, disables the option; a switch in the right position, ON, enables the option.

If a mask option is enabled (switched ON) and the corresponding bit of the port A data direction register is configured as an input, a low on the port A pin generates an interrupt. The diagram here shows a possible setting: Interrupt masks are disabled for port A lines 0 through 3 and are enabled for port A lines 4 through 7.



The default setting for all eight positions of SW1 is OFF.

Remaining System Installation

When you have configured headers W1 and W2 and set switch SW1, M68EM05P18 configuration is complete:

- Ensure that the power to the development tool is off.
- If installing the M68EM05P18 in an MMDS05 station module, remove the panel from the station module top.
- Fit together EM connectors P1 and P2 (on the bottom of the board) and platform board DIN connectors. Snap the corners of the EM onto the plastic standoffs.
- Connect the target cable, if appropriate.
- If installing in an MMDS05, replace the panel.

At this point, you are ready to make remaining cable connections, as necessary, and restore power.

For instructions, consult either the *MMEVS05/MMEVS08 Operations Manual* (MMEVS0508OM/D) or the *MMDS05 Operations Manual* (MMDS05OM/D).

Personality File Usage

Your development system uses a specific personality file for the MCU type being emulated. For example, to emulate an MC68HC(8)05P18 MCU, the system uses the personality file 00022Vxx.MEM. Debugger software loads this personality file upon power up.

NOTE: *Note that personality file names follow the pattern 00ZZZVxx.MEM, where ZZZ is the EM identifier or MCU name and xx is the version of the file.*

MC68HC(8)05P18 Emulation

NOTE: *Be aware that if the computer operating properly (COP) mask option has been selected as enabled, your code must clear the COP watchdog timer counter to avoid a COP reset. The counter is cleared by writing a logical 0 to bit 0 at location $3FF0. This should be the first check when code is not operating as expected.*

The MC68HC(8)05P18 MCU is emulated on the M68EM05P18 emulation module. The resident MCU (socket XU5) should be an EEPROM device (an MC68HC805P18).

The following paragraphs detail known differences between the performance of an MC68HC805P18 MCU run in single-chip operation versus the way certain features will perform during emulation.

Mask Option Control

In single-chip mode operation:

For an MC68HC805P18 MCU, the mask options will be determined by which options have been programmed in the MOR EEPROM locations ($3F00–$3F01). These registers must be programmed using a dedicated programmer.

In emulation:

The first byte of mask options (MOR1–$3F00) is controlled initially by what has been programmed in the MOR1 EEPROM location (MOR1–$3F00). Alternatively, the mask options can be controlled via software and allow mask option changes during a debug session. Option changes can be accomplished by command entry (for instance, the MM command) or by execution of user code (for instance, STA instruction).

The procedure for changing MOR1 options during an emulation session requires manipulation of the reserved register at location $0011 and the MOR1 location. First, set bit 6 of register $0011 (write a $40 to location $0011). If you use the memory modify (MM) command, a "Write did not verify" message should be ignored. The mask options can then be set by writing the desired mask option register byte value to the MOR1 location ($3F00). To continue using the modified mask options, you must leave register $0011 bit 6 set to 1.

The selected mask options will return to the default options programmed in the MOR EEPROM location MOR1 if the MCU takes any reset or bit 6 of register $0011 is cleared (you write a $00 to $0011).

The second byte of mask options (MOR2–$3F01) is always controlled through the eight positions of DIP switch SW1. The top position controls the port A0 pin pullup/interrupt option and the bottom position controls the port A7 pin pullup/interrupt option. Each option will be enabled if its respective position is ON.

Port A Pullups/ Interrupts

In single-chip mode operation:

The simple port A input/output (I/O) feature and the associated interrupt/pullup options are implemented through the port A pins of the MC68HC(8)05P18 MCU. With this implementation, an interrupt service routine could poll the external $\overline{IRQ}$ pin using BIL and BIH statements and determine if the source of an interrupt was the external $\overline{IRQ}$ pin or one of the enabled port A interrupts.

In emulation:

The port A I/O function is rebuilt off-chip and the enabled interrupt/pullup options will generate interrupts through the external $\overline{IRQ}$ pin. An interrupt service routine using BIL and BIH instructions could not determine if an interrupt was generated via an external $\overline{IRQ}$ pin or one of the enabled port A interrupts. The proper way to differentiate between a port interrupt and external interrupt is to have the interrupt service routine poll possible port A interrupts and, if none are low, then the interrupt was driven by an external IRQ.

Port C Bit 7 Sharing with the A/D Subsystem

In single-chip mode operation:

The port C bit 7 pin is shared with the A/D subsystem. When the A/D is enabled, the pin becomes the V_{REFH} input. External port C bit 7 is not available to the CPU. Port C bit 7 data (PC7) and data direction (DDRC7) bits are still accessible from the CPU, though they have no effect on the external PC7/V_{REFH} pin. If the A/D subsystem is disabled, port C bit 7 functionality will be restored to the external pin, and the last conditions stored in PC7 and DDRC7 bits will determine data and direction for the simple I/O.

In emulation:

Port C is rebuilt external to the MCU while the V_{REFH} input for the A/D continues to be at the MCU pin. To prevent the port C bit 7 source from affecting the V_{REFH} function, port C bit 7 should be made an input (by clearing the DDRC7 bit) before enabling the A/D.

Programming the 128-Byte EEPROM Array

In single-chip mode operation:

The 128-byte EEPROM array can be programmed during normal operation of the part. User code modifies the array on single byte basis by manipulation of the programming register located at address $001C.

In emulation:

Like single-chip, the 128-byte EEPROM array can be programmed during normal operation of the part. User code modifies the array on single byte basis by manipulation of the programming register located at address $001C.

Alternately, the array can be modified using memory altering commands of the debugger. The commands that will modify the array are assemble (ASM), block fill (BF), load S19 file (LOAD), and memory modify (MM).

HC05EVS Configuration and Operation

Contents

Introduction

The following paragraphs explain how to configure and use your M68EM05P18 as part of an HC05EVS. For other parts of system installation or configuration, see the *HC05EVS Operations Manual* (HC05EVSOM/D). If you use your M68EM05P18 as part of an MMEVS05 or MMDS05, refer to **MMDS/MMEVS Configuration and Operation** on page 19 for corresponding information.

The topics covered in this chapter are:

- **Setting M68EM05P18 Jumper Headers and Switches** on page 33 explains how to set the M68EM05P18 jumper headers.
- **Remaining System Installation** on page 37 covers the final steps to system installation.
- **MC68HC(8)05P18 Emulation** on page 38 explains considerations pertaining to the MCU you emulate.
- **HC05EVS Limitations** on page 41 explains limitations on using the M68EM05P18 in an HC05EVS.

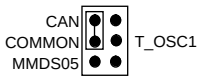
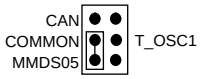
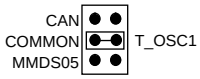
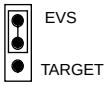
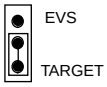
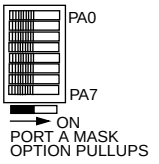
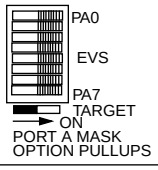
NOTE: *Note that you can configure an M68EM05P18 already installed in the HC05EVS platform board. To do so, disconnect platform board power, then follow the guidance of this chapter.*

CAUTION: *Be sure to switch off power before you reconfigure an installed EM. Reconfiguring EM jumper headers with power left on can damage HC05EVS circuits.*

Setting M68EM05P18 Jumper Headers and Switches

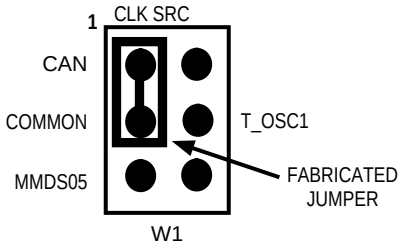
Your M68EM05P18 has two jumper headers — W1 and W2 — and an 8-position DIP switch, SW1, for the port A pullup/interrupt mask options. **Table 4** provides a quick reference for configuration options. Refer to the paragraphs that follow for a more detailed explanation.

Table 4. Jumper Header and Switch Positions for HC05EVS

Jumper/ Switch	Position	Description	Factory Setting
Clock Source Select, W1		Select the 4-MHz canned oscillator located on the EM board at XY1.	X
		Not applicable	
		Selects a user supplied clock source. The clock is input to connector J2 through a target cable assembly.	
Reset Select, W2		HC05EVS will drive resets out.	X
		The target system will reset the HC05EVS when the RESET line is asserted low. Also requires placing a jumper in platform board jumper header J3.	
Port A Interrupt Mask Option Control, SW1		Each port A bit is individually configurable. In the left position, the option is **not** selected.	X
		In the right position, the option **is** selected.	

Clock Source Select Header, W1

Jumper header W1 determines the clock-signal source. The diagram here illustrates the jumper header where the pin marked COMMON is always connected to one of the three clock source pins via the fabricated jumper. The default configuration, between CAN and COMMON, selects the 4-MHz canned oscillator clock source (at board location XY1).



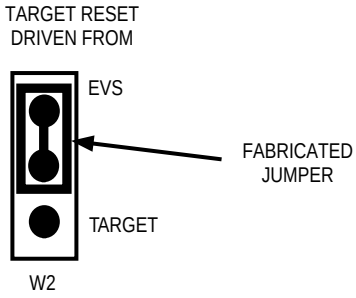
Another possible clock source is a user supplied clock source, coming through the target cable connected to J2. To use this source, reposition the W1 jumper header between the T_OSC1 and COMMON pins.

NOTE: *The user supplied source through the target cable should be a CMOS level square wave.*

NOTE: *The W1 configuration between MMDS05 and COMMON is not correct for an M68EM05P18 that is part of an HC05EVS system.*

Reset Select Header, W2

Jumper header W2 controls the path of a target reset. The diagram here shows the factory configuration: The fabricated jumper in the EVS position enables the HC05EVS to control resets when you press the user or master reset switch.



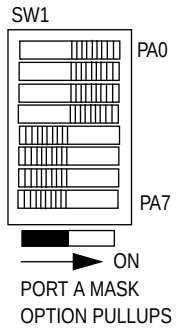
Alternatively, you can enable the target system to reset the H05EVS. To do so:

- Reposition the M68EM05P18 W2 jumper to the TARGET position, and
- Insert a fabricated jumper into the HC05EVS platform board header J3.
- Provide RESET signal to connector J2 pin 2 (T_RST*)

Interrupt Mask Control Switch, SW1

The eight positions of switch SW1 enable or disable the port A interrupt mask options. Each position controls one port A line. A switch in the left position, OFF, disables the option; a switch in the right position, ON, enables the option.

If a mask option is enabled (switched ON) and the corresponding bit of the port A data direction register is configured as an input, a low on the port A pin generates an interrupt. This diagram shows a possible setting. Interrupt masks are disabled for port A lines 0 through 3 and are enabled for port A lines 4 through 7.



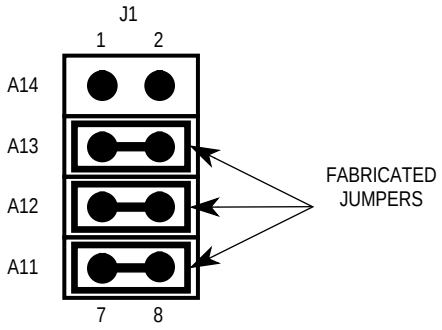
The default setting for all eight positions of SW1 is OFF.

Remaining System Installation

When you have configured headers W1 and W2 and set switch SW1, you have finished the M68EM05P18 configuration.

NOTE: *Ensure that the power to the HC05EVS is off before moving any jumper settings on the platform board.*

Find platform board jumper header J1 near the power connector. Make sure that three fabricated jumpers are installed, per the diagram here.



To install the M68EM05P18 on the platform board, fit together EM connectors P1 and P2 (on the bottom of the board) and platform board connectors P3 and P4. Snap the corners of the EM onto the plastic standoffs.

At this point, you are ready to make remaining cable connections, as necessary, and restore power. For instructions, consult the *HC05EVS Operations Manual* (HC05EVSOM/D).

MC68HC(8)05P18 Emulation

NOTE: *Be aware that if the computer operating properly (COP) mask option has been selected as enabled, your code must clear the COP watchdog timer counter to avoid a COP reset. The counter is cleared by writing a logical 0 to bit 0 at location $3FF0. This should be the first check when code is not operating as expected.*

The MC68HC(8)05P18 MCU is emulated on the M68EM05P18 emulation module. The resident MCU (socket XU5) should be an EEPROM device (an MC68HC805P18).

The following paragraphs detail known differences between the performance of an MC68HC805P18 MCU run in single-chip operation versus the way certain features will perform during emulation.

Port A Pullups/ Interrupts

In single-chip mode operation:

The simple port A I/O feature and the associated interrupt/pullup options are implemented through the port A pins of the MC68HC(8)05P18 MCU. With this implementation, an interrupt service routine could poll the external IRQ pin using BIL and BIH statements and determine if the source of an interrupt was the external IRQ pin or one of the enabled port A interrupts.

In emulation:

The port A I/O function is rebuilt off-chip and the enabled interrupt/pullup options will generate interrupts through the external IRQ pin. An interrupt service routine using BIL and BIH instructions could not determine if an interrupt was generated via an external IRQ pin or one of the enabled port A interrupts. The proper way to differentiate between a port interrupt and an external interrupt is to have the interrupt service routine poll possible port A interrupts. If none are low, then the interrupt was driven by an external IRQ.

Mask Option Control

In single-chip mode operation:

For an MC68HC805P18 MCU, the mask options will be determined by which options have been programmed in the MOR EEPROM locations ($3F00–$3F01). These registers must be programmed using a dedicated programmer.

In emulation:

The first byte of mask options (MOR1–$3F00) is controlled initially by what has been programmed in the MOR1 EEPROM location (MOR1–$3F00). Alternatively, the mask options can be controlled via software and allow mask option changes during a debug session. Option changes can be accomplished by command entry (for instance, the MM command) or by execution of user code (for instance, STA instruction).

The procedure for changing MOR1 options during an emulation session requires manipulation of the reserved register at location $0011 and the MOR1 location. First, set bit 6 of register $0011 (write a $40 to location $0011). If you use the memory modify (MM) command, a "Write did not verify" message should be ignored. The mask options can then be set by writing the desired mask option register byte value to the MOR1 location ($3F00). To continue using the modified mask options, leave register $0011 bit 6 set to 1.

The selected mask options will return to the default options programmed in the MOR EEPROM location MOR1 if the MCU takes any reset or bit 6 of register $0011 is cleared (write a $00 to $0011).

The second byte of mask options (MOR2–$3F01) is always controlled through the eight positions of DIP switch SW1. The top position controls the port A0 pin pullup/interrupt option and the bottom position controls the port A7 pin pullup/interrupt option. Each option will be enabled if its respective position is ON.

Port C Bit 7 Sharing with the A/D Subsystem

In single-chip mode operation:

The port C bit 7 pin is shared with the A/D subsystem. When the A/D is enabled, the pin becomes the V_{REFH} input. The external port C bit 7 is not available to the CPU. Port C bit 7 data (PC7) and data direction (DDRC7) bits are still accessible from the CPU, though they have no effect on the external PC7/V_{REFH} pin. If the A/D subsystem is disabled, port C bit 7 functionality will be restored to the external pin, and the last conditions stored in PC7 and DDRC7 bits will determine data and direction for the simple I/O.

In emulation:

Port C is rebuilt external to the MCU while the V_{REFH} input for the A/D continues to be at the MCU pin. To prevent the port C bit 7 source from affecting the V_{REFH} function, port C bit 7 should be made an input (by clearing the DDRC7 bit) before enabling the A/D.

HC05EVS Limitations

Limitations that apply to using your M68EM05P18 in an HC05EVS are explained here.

1. **CLI/RTI.** You cannot trace a clear interrupt mask (CLI) or return from interrupt (RTI) instruction with an interrupt enabled and pending, due to MCU interrupt handling. Attempting such a trace causes an interrupt in the monitor map, which forces a software reset of the HC05EVS. User breakpoints remain in the user map as SWI instructions; you must remove such SWI instructions.
2. **Branch.** Do not trace a conditional branch instruction (such as BRCLR) that branches to itself. Because the monitor places an SWI instruction on the object of the branch, the system never would execute the instruction. However, it would appear to you that the instruction had executed. You can enter a GO command while the PC points to this type of instruction as long as the instruction is not a breakpoint address.
3. **IRQ/SWI.** Whenever possible, avoid mixing interrupt requests (IRQs) and user software interrupts (SWIs) to prevent a possible IRQ-SWI timing problem. A concurrent hardware interrupt and SWI could cause an HC05EVS failure that could stop program execution. To recover from such a failure (which occurs infrequently), press the master reset switch (SW3).
4. **Memory Map.** You must be aware of the memory map of the MCU being emulated and be sure to use only valid ROM locations. The HC05EVS does not provide protection to limit user programs to the exact amount of MCU ROM available. (For information about memory maps, consult the technical data book for the MCU.)
5. **COP.** The computer operating properly (COP) update register serves as a ROM location for the resident MCU. Accordingly, the platform board write-protect jumper header must enable write protection. Otherwise, any writes to the COP update register change the value stored in user pseudo ROM.

Schematics

Contents

M68EM05P18 Schematics

Refer to the following pages for the four sheets of schematics for the M68EM05P18 emulation module.

M68EM05P18 Schematics

M68EM05P18 Schematics (Sheet 1 of 4)

NOTES, UNLESS OTHERWISE SPECIFIED

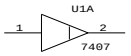
1. VCC PIN LOCATIONS :

   VCC IS APPLIED TO PIN 8 OF ALL 8-PIN IC's, PIN 14 OF ALL 14-PIN IC's, PIN 16 OF ALL 16-PIN IC's, PIN 20 OF ALL 20-PIN IC's, ETC.

2. GROUND PIN LOCATIONS :

   GROUND IS APPLIED TO PIN 4 OF ALL 8-PIN IC's, PIN 7 OF ALL 14-PIN IC's, PIN 8 OF ALL 16-PIN IC's, PIN 10 OF ALL 20-PIN IC's, ETC.

3. DEVICE TYPE, PIN NUMBERS, AND REFERENCE DESIGNATOR OF GATES ARE SHOWN AS FOLLOWS :



7407 = DEVICE TYPE
1 AND 2 = PIN NUMBERS
U1A = REFERENCE DESIGNATORS

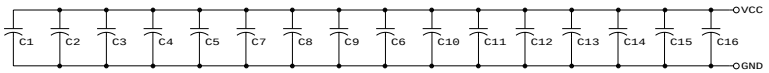
4. RESISTANCE VALUES ARE IN OHMS.
5. RESISTORS ARE 1/4 WATT, 5%.
6. CAPACITANCE VALUES ARE IN MICROFARADS.

M68EM05P18 EMULATION MODULE

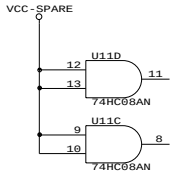
REVISIONS

ECN #	SCH REV	PWB REV	DESCRIPTION	DATE
	3	B	NEW REV OF PWB	3/20/95
	4	C	NEW REV OF PWB. ADD 2 CHANNELS OF A/D	12/30/95
	5	C	Fix EM-WE signal for register latches.	2/22/96

Decouple Caps for ICs as labeled.
All caps are 0.1 uF @ 50 V



Spare Gates



ORCAD IV FLAT FILES

|LINK
|5P18R5S2.SCH
|5P18R5S3.SCH
|5P18R5S4.SCH

COMPUTER GENERATED DRAWING : DO NOT REVISE MANUALLY

CSIC DEVELOPMENT TOOLS

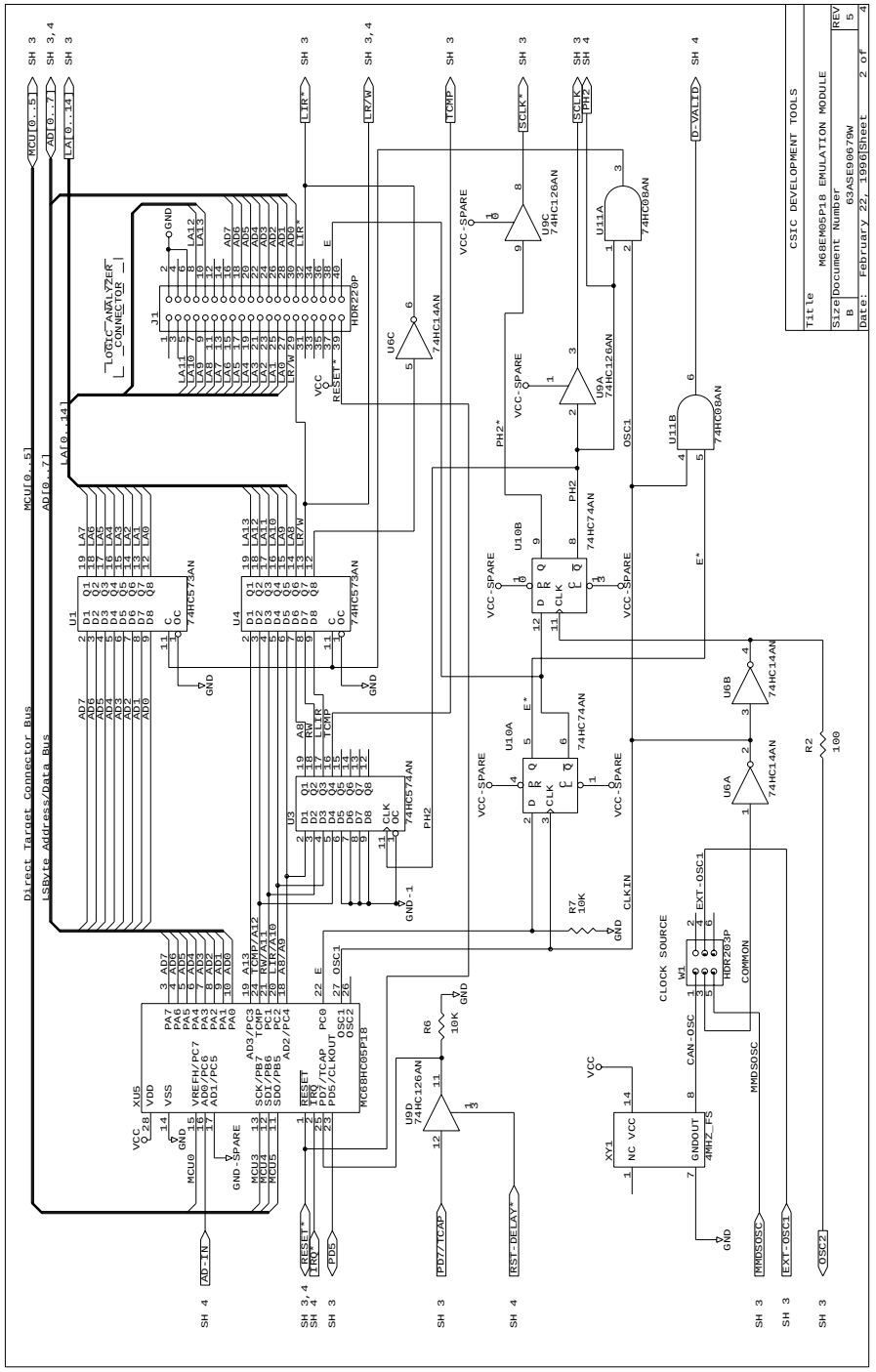
Title: M68EM05P18 EMULATION MODULE

Size	Document Number	REV
B	63ASE90679W	5

Date: February 22, 1996 Sheet 1 of 4

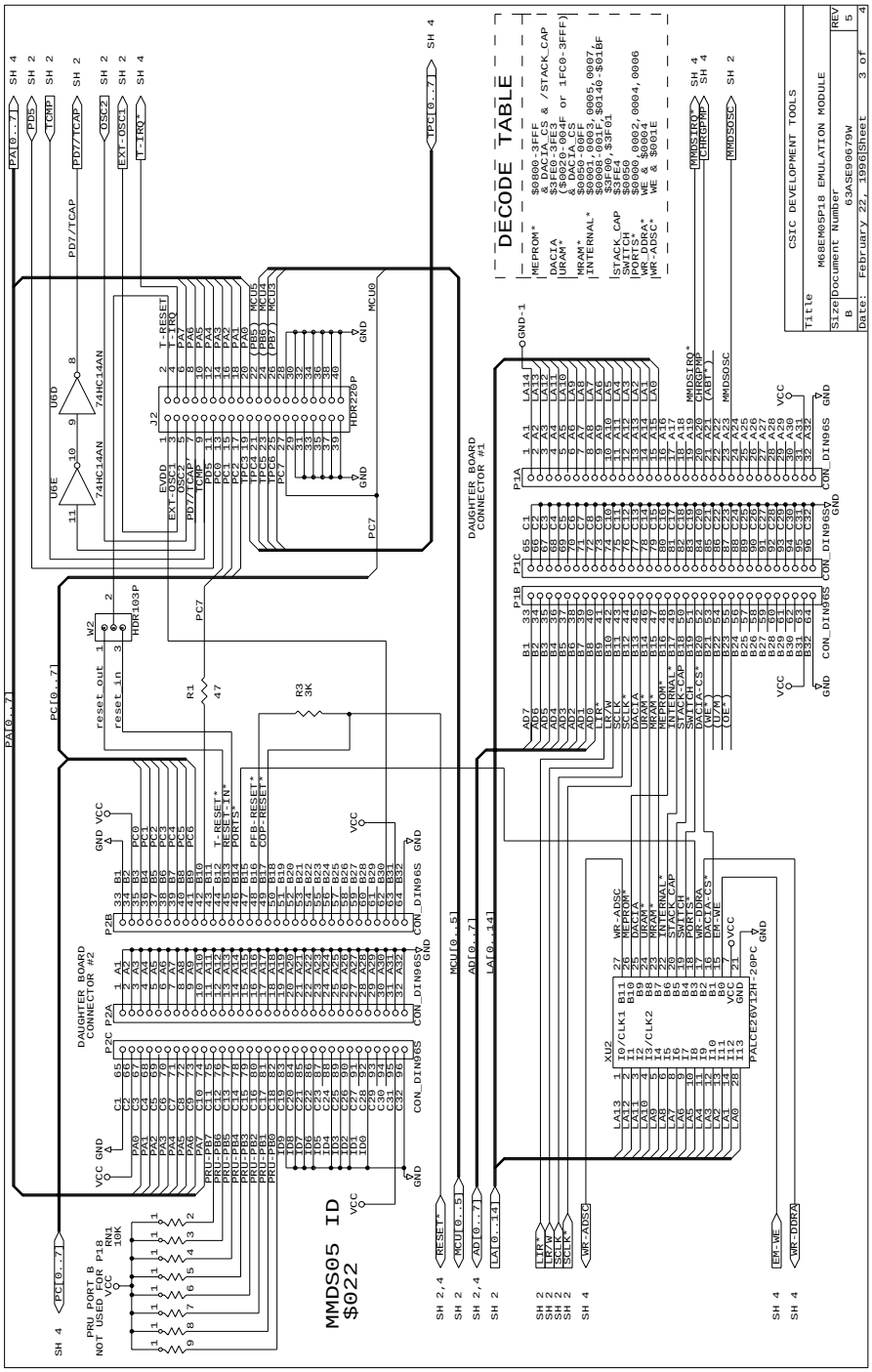
M68EM05P18 Schematics

M68EM05P18 Schematics (Sheet 2 of 4)



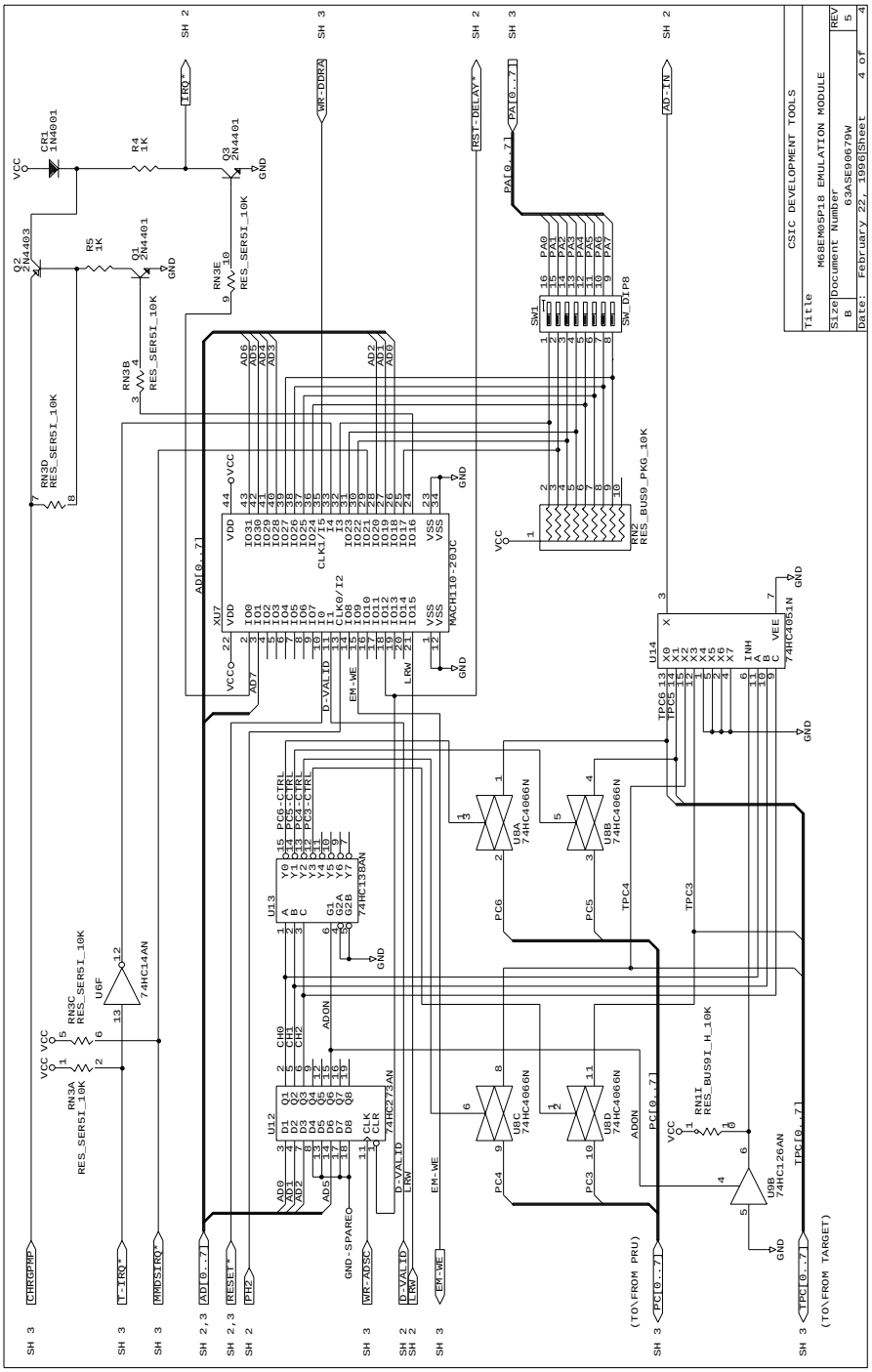
M68EM05P18 Schematics

M68EM05P18 Schematics (Sheet 3 of 4)



M68EM05P18 Schematics

M68EM05P18 Schematics (Sheet 4 of 4)



M68EM05P18 Schematics

Note Page

Note Page

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