M68EM05V12

Emulation Module
User's Manual

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Revision History

This table summarizes differences between this revision and the previous revision of this emulation module user's manual.

Previous Revision	None
Current Revision	Original Release
Date	09/96

Revision History

General Description

Contents

Introduction

The M68EM05V12 gives the Motorola development tool the ability to emulate target systems based on MC68HC705V12 and MC68HC05V12 microcontroller units (MCUs). By substituting a different emulation module (EM), the Motorola development tool can be enabled to emulate other MCUs. Refer to *Motorola's Development Tool Selector Guide*, order number SG173/D, for a complete list of available EMs.

This hardware user's manual explains connection, configuration, and operation information specific to the M68EM05V12 emulation module. The module can be installed in two Motorola development systems, the MMDS or MMEVS. To configure your M68EM05V12 for either development system, follow the instructions given in See **MMDS/MMEVS Configuration and Operation** on page 19.

Motorola's complete emulation system consists of the emulation module described in this manual as well as other separately purchased options described in the following paragraphs.

The following items are included with the M68EM05V12 emulation module:

- **An M68EM05V12 emulation module (EM)** — The printed circuit board that enables system functionality for MC68HC(7)05V12 MCUs. The female connectors, on the bottom of the module, mate with male connectors on a development system platform board.
- **Configuration software** — 3 1/2-inch diskette containing personality files for this module

Separately purchased Motorola modular development tool options include:

- **An MMEVS platform board (M68MMPFB0508)** — The MMEVS is an economical development tool that provides real-time in-circuit emulation. The unit's integrated design environment includes an editor, an assembler, a user interface, and a source-level debugging program.
- **An MMDS0508 modular development system (M68MMDS0508)** — The MMDS is a high-performance development tool that has all the capabilities of the MMEVS. In addition, it also has a bus state analyzer and real-time memory windows.
- **Flex cable target assembly** — Refer to **Target Cable Assemblies** on page 12 for more information.

User-supplied components include:

- **Host computer** — See the appropriate development tool user’s manual for minimum requirements.
- **Power supply** — +5 Vdc is required for the MMEVS.

Emulation Module Layout

Figure 1 shows the layout of the M68EM05V12. Jumper header W1 and W2 control the voltage reference inputs to the analog-to-digital subsystem. Jumper headers W3, W4, and W5 are used in configuring the BDLC subsystem. W6 controls the voltage applied to the $\overline{IRQ}/V_{PP}$ pin. Jumper header W7 lets you select the clock-signal source. Jumper headers W8 ,W9, and W10 are used in configuring the gauge driver subsystem with your target system.

Target connectors J2 and J3 are the interface to a target system; these connectors use a separately purchased target cable assembly. When you install the M68EM05V12 in the MMDS, the target cable passes through the slit in the station module enclosure. Connector J1 connects to an optional logic analyzer.

DIN connectors P1 and P2 connect the EM and a development system platform board. Lever terminal connector P3 is for inputting the gauge driver battery voltage and for bus data link controller (BDLC) interface.

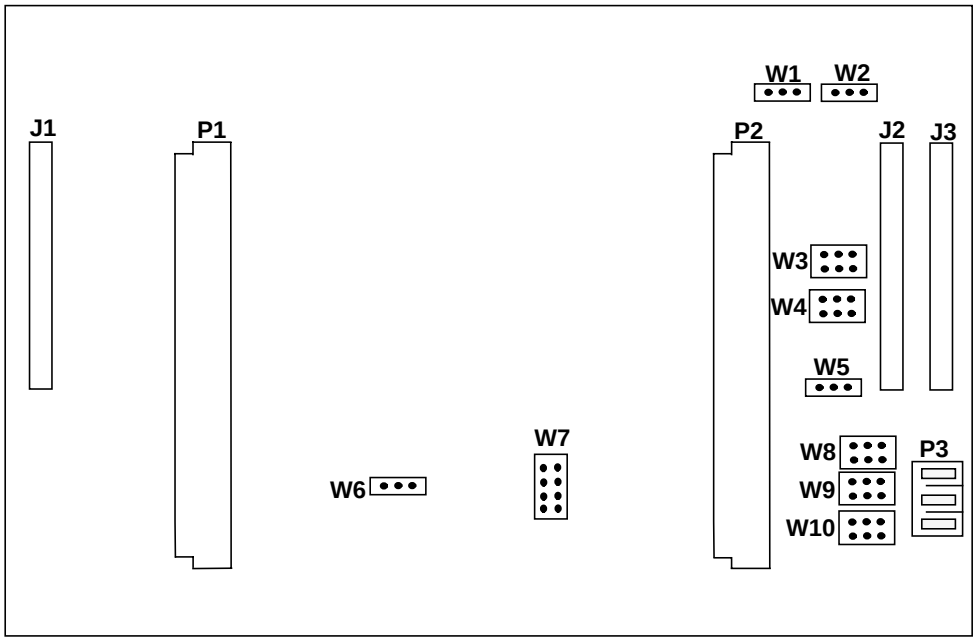


Figure 1. M68EM05V12 Emulation Module

Target Cable Assemblies

To connect your M68EM05V12 to a target system, a separately purchased target cable assembly is needed. Cable assemblies are available to support 68-pin PLCC packages.

The target cable connects to the emulator via connectors J2 and J3 on the M68EM05V12 emulation module. Pin assignments and signal descriptions for connectors J2 and J3 can be found in **Target Cable Connector Pin Assignments** on page 14.

Figure 2 represents a target cable assembly. An assembly consists of a flex cable and a target head adapter. One end of the flex cable plugs onto M68EM05V12 connectors J2 and J3 with orientation shown in **Figure 2**. The other end of the flex cable plugs into the target head adapter. The target head adapter then inserts into a PLCC socket in a target system.

The MC68HC705V12 target cable assembly consists of:

- Flex cable M68CBL05C
- Target head adapter M68TC05V12FN68

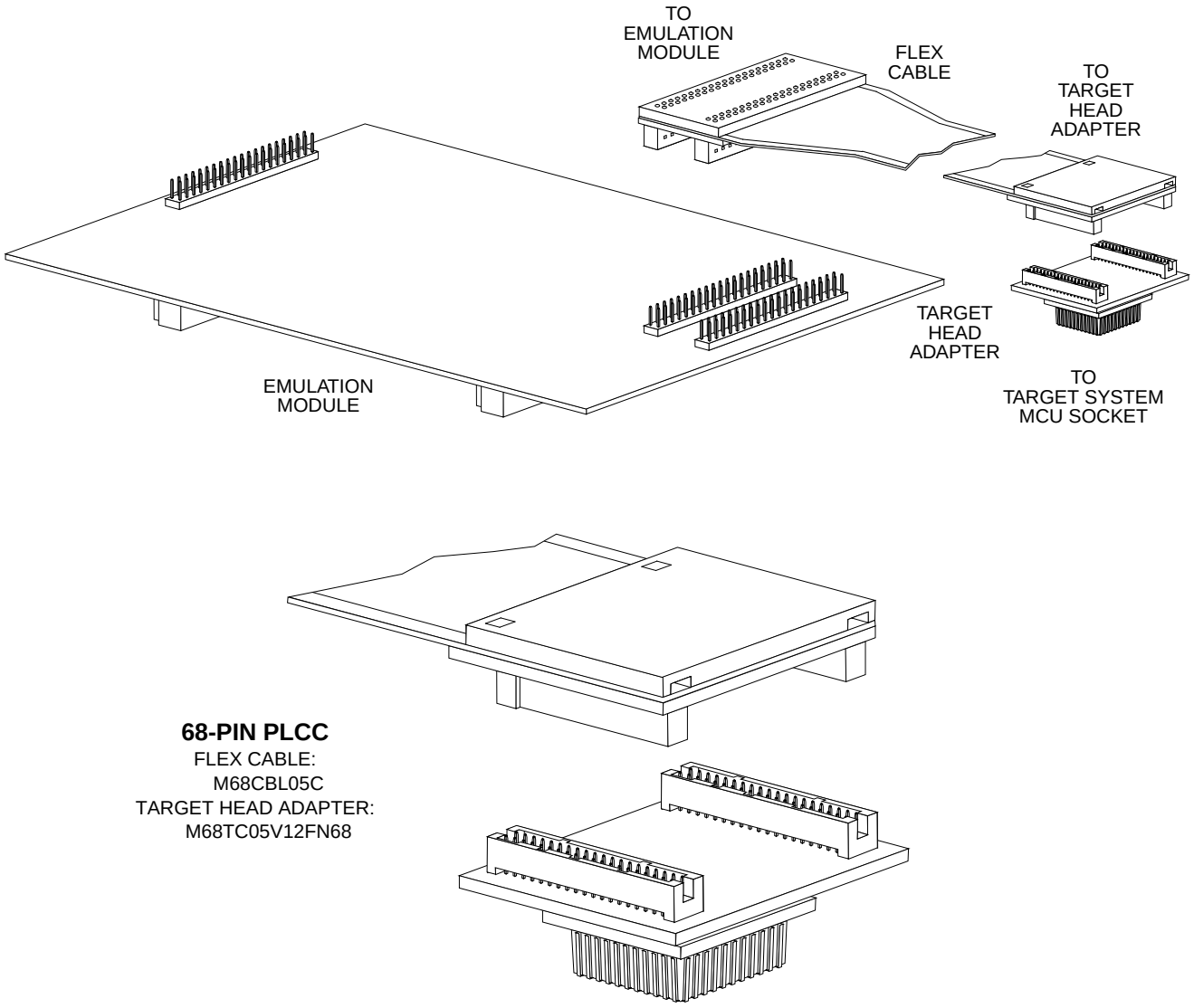


Figure 2. Target Cable Assembly

Connector Information

The connectors on the M68EM05V12 module provide access to the user mode emulation signals (J2 and J3) as well as select internal signals (J1). Connectors J2 and J3 are used for a cable interface to a user's target system, while connector J1 is used to connect a logic analyzer.

Target Cable Connector Pin Assignments

Figure 3 shows the pin assignments for connector J2 and J3. **Table 1** lists signal descriptions for connector J2; **Table 2** lists signal descriptions for connector J3.

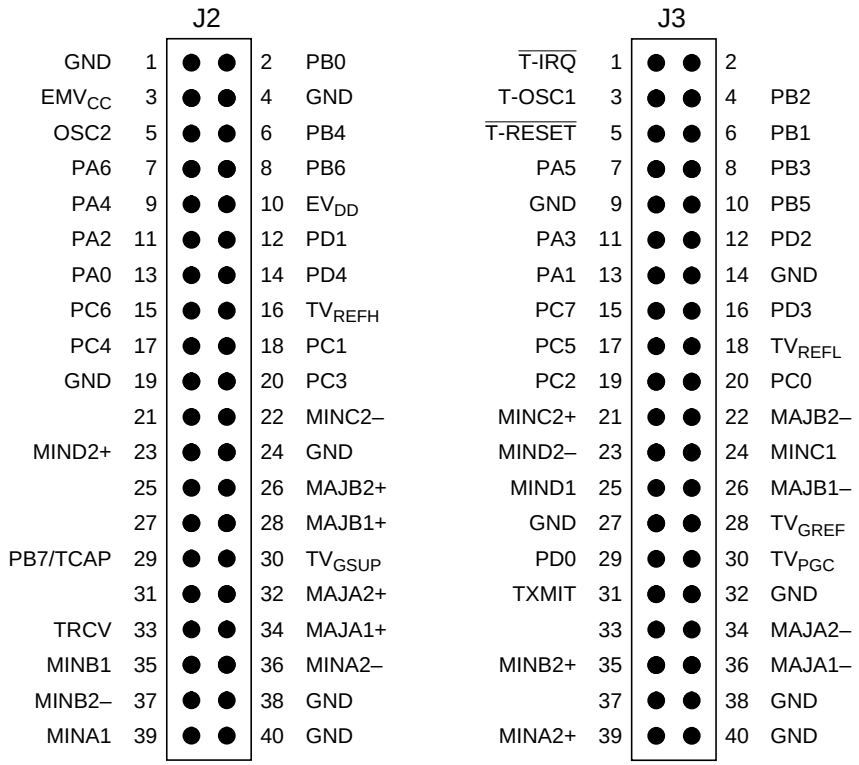


Figure 3. Target Connector Pin Assignment

Table 1. Connector J2 Signal Descriptions

Pin	Mnemonic	Signal
1, 4, 19, 24, 38, 40	GND	GROUND
2, 6, 8, 29	PB0, PB4, PB6, PB7/TCAP	PORT B (Bits 0, 4, 6, 7) – General-purpose I/O lines controlled by software via data and data direction registers If the SPI subsystem is enabled, PB0 becomes the slave select input. If the PWM subsystem is enabled, PB4 becomes the PWMA output. If the 16-bit timer is enabled, PB6 becomes the TCMP output and PB7 becomes the TCAP input. (Other port B lines on connector J3)
3	EMV_{CC}	+5 Vdc POWER – Connection to the system voltage V_{CC}
5	OSC2	OSCILLATOR 2 – Output clock signal. Inversion of the OSC1 clock input to the MCU
7, 9, 11, 13	PA6, PA4, PA2, PA0	PORT A (Bits 6, 4, 2, 0) – General-purpose I/O lines controlled by software via data and data direction registers (Other port A lines on connector J3)
10	EV_{DD}	EXTERNAL VOLTAGE DETECT – Connected to target V_{CC}, used to sense target power applied, for target status in MMDS status window.
12, 14	PD1, PD4	PORT D (Bits 1, 4) – General-purpose input lines A/D LINES – If the analog-to-digital subsystem is enabled, these lines become converter input lines AD1 and AD4, respectively. (Other port D lines on connector J3)
15, 17, 18, 20	PC6, PC4, PC1, PC3	PORT C (Bits 6, 4, 1, 3) – General-purpose I/O lines controlled by software via data and data direction registers If the port C interrupt capability of the external interrupt subsystem is selected, each pin can generate an interrupt if its DDR bit is set to input. (Other port C lines on connector J3)
16	TV_{refh}	Possible source for the positive (high) reference voltage input for the A/D subsystem. Input is controlled by jumper header W2.
21, 25, 27, 31	NC	No connection
22	MINC2–	MINC2– – Minor gauge C full H-bridge coil driver pins. (Other minor C lines on connector J3)
23	MIND2+	MIND2+ – Minor gauge D full H-bridge coil driver pins (Other minor D lines on connector J3)
26, 28	MAJB2+, MAJB1+	MAJB2+, MAJB1+ – Major gauge B full H-bridge coil driver pins (Other major B lines on connector J3)
30	TV_{gsup}	V_{gsup} – The regulated gauge voltage input. Use of this input is controlled by jumper headers W8, W9, and W10.
32, 34	MAJA2+, MAJA1+	MAJA2+, MAJA1+ – Major gauge A full H-bridge coil driver pins (Other major A lines on connector J3)
33	TRCV	The receive digital input (RXP) for the BDLC subsystem. Use of this input is controlled by jumper headers W3, W4, and W5.
35, 37	MINB1, MINB2–	MINB1, MINB2– – Minor gauge B full H-bridge coil driver pins (Other minor B lines on connector J3)
36, 39	MINA2–, MINA1	MINA2–, MINA1 – Minor gauge A full H-bridge coil driver pins (Other minor A lines on connector J3)

Table 2. Connector J3 Signal Descriptions

Pin	Mnemonic	Signal
1	$\overline{\text{TIRQ}}$	TARGET INTERRUPT REQUEST – Active-low input signal from the target that asynchronously applies an MCU interrupt
2, 33, 37	NC	No connection.
3	TOSC1	OSCILLATOR 1 – A possible clock source input for the M68EM05V12 board. System bus frequency is OSC1 ÷ 2. Use of this signal is controlled by jumper header W7.
4, 6, 8, 10	PB2, PB1, PB3, PB5	PORT B (Bits 2, 1, 3, 5) – General-purpose I/O lines controlled by software via data and data direction registers. (Other port B lines on connector J2) If the SPI subsystem is enabled, PB2, PB1, and PB3 become the MISO, SCK, and MOSI lines, respectively. If the PWM subsystem is enabled, PB5 becomes the PWMB output.
5	$\overline{\text{TRESET}}$	Active-low bidirectional signal to/from the target system driven low to pull the MCU into reset.
7, 11, 13	PA5, PA3, PA1	PORT A (Bits 5, 3, 1) – General-purpose I/O lines controlled by software via data and data direction registers. (Other port A lines on connector J2)
9, 14, 27, 32, 38, 40	GND	GROUND
12, 16, 29	PD2, PD3, PD0	PORT D (Bits 2, 3, 0) – General-purpose input lines A/D LINES – If the analog-to-digital subsystem is enabled, these lines become converter input lines AD2, AD3, and AD0, respectively. (Other port D lines on connector J2)
15, 17,19, 20	PC7, PC5, PC2, PC0	PORT C (Bits 7, 5, 2, 0) – General-purpose I/O lines controlled by software via data and data direction registers. If the port C interrupt capability of the external interrupt subsystem is selected, each pin can generate an interrupt if its DDR bit is set to input. (Other port C lines on connector J2)
18	TV_{refl}	Possible source for the negative (low) reference voltage input for the A/D subsystem. Input is controlled by jumper header W1.
21, 24	MINC2+, MINC1	MINC2+, MINC1 – Minor Gauge C full H-bridge coil driver pins (Other minor C lines on connector J2)
23, 25	MIND2–, MIND1	MIND2–, MIND1 – Minor gauge D full H-bridge coil driver pins (Other minor D lines on connector J2.)
22, 26	MAJB2–, MAJB1–	MAJB2–, MAJB1– – Major gauge B full H-bridge coil driver pins (Other major B lines on connector J)
28	TV_{gref}	V_{GVref} – The feedback pin for the gauge power regulator circuit. Use of this input is controlled by jumper headers W8, W9, and W10.
30	TV_{PGC}	V_{PGC} – The gauge power control pin for the external pass device. Use of this input is controlled by jumper headers W8, W9, and W10.
31	TXMIT	The transmit digital output (TXP) for the BDLC subsystem. Use of this output is controlled by jumper headers W3, W4, and W5.
34, 36	MAJA2–, MAJA1–	MAJA2–, MAJA1– – Major gauge A full H-bridge coil driver pins (Other major A lines on connector J2)
35	MINB2+	MINB2+ – Minor gauge B full H-bridge coil driver pins (Other minor B lines on connector J2)
39	MINA2+	MINA2+ – Minor gauge A full H-bridge coil driver pins (Other minor A lines on connector J2)

Logic Analyzer Connector Pin Assignments

Figure 4 shows the pin assignments for logic analyzer connector J1. This connector provides easy access to many of the signals used internally. **Table 3** lists signal descriptions for this connector.

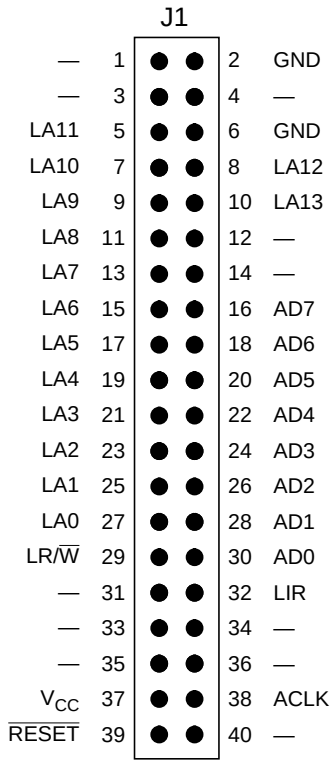


Figure 4. Connector J1 Pin Assignments

Table 3. Logic Analyzer Connector J1 Signal Descriptions

Pin	Mnemonic	Signal
1, 3, 4, 12, 14, 31, 33, 34, 35, 36, 40	NC	No connection
2, 6	GND	GROUND
10, 8	LA13–LA12	LATCHED ADDRESSES (Bits 13–12) — MCU latched output address bus
5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27	LA11–LA0	LATCHED ADDRESSES (Bits 11–0) — MCU latched output address bus
16, 18, 20, 22, 24, 26, 28, 30	AD7–AD0	DATA BUS (Bits 7–0) — MCU multiplexed I/O bus
29	LR/$\overline{W}$	LATCHED READ/WRITE — The MCU's write signal is latched and used on the emulator to control emulator memory accesses.
32	$\overline{LIR}$	LOAD INSTRUCTION REGISTER — Active-low signal indicating an opcode fetch cycle is in process.
37	V_{CC}	+5 Vdc POWER — Connection to the system voltage V_{CC}
38	ACLK	ANALYZER CLOCK — The latched addresses are valid on the latched address bus at the rising edge of ACLK. Also, data is valid on the AD BUS at ACLK's rising edge.
39	$\overline{RESET}$	RESET — Active-low signal; will be asserted during internally or externally caused resets

MMDS/MMEVS Configuration and Operation

Contents

Introduction

The following paragraphs explain how to configure and use your M68EM05V12 as part of an MMDS or MMEVS system. For other parts of system installation and configuration, see either the *MMDS0508 Operations Manual* (MMDS0508OM/D) or *MMEVS05/MMEVS08 Operations Manual* (MMEVS0508OM/D).

The topics covered in this chapter are:

- **Setting M68EM05V12 Jumper Headers** on page 21 explains how to set the M68EM05V12 jumper headers.
- **Using Lever Terminal Connector P3** on page 28 details usage of other possible connections to the emulation module.
- **Remaining System Installation** on page 29 covers the final steps to system installation.
- **Personality Files Usage** on page 30 discusses the personality file used on the M68EM05V12 board.
- **MC68HC(7)05V12 Emulation** on page 31 explains special considerations for emulating with this module.

NOTE: *You can configure an M68EM05V12 already installed in the system platform board. To do so, remove system power and then follow the guidance of this chapter.*

CAUTION: *Be sure to switch off power before you reconfigure an installed EM. Reconfiguring EM jumper headers with the power on can damage emulation circuits.*

Setting M68EM05V12 Jumper Headers

The M68EM05V12 has 10 jumper headers, W1–W10. **Table 4** provides a quick reference for configuration options. Refer to the paragraphs that follow for a more detailed explanation.

Table 4. Jumper Header Positions

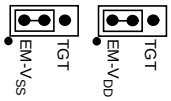
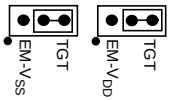
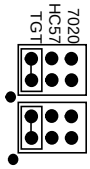
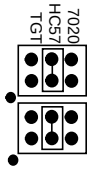
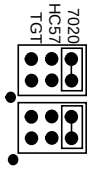
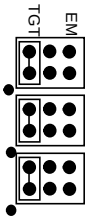
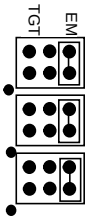
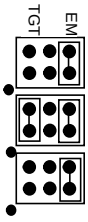
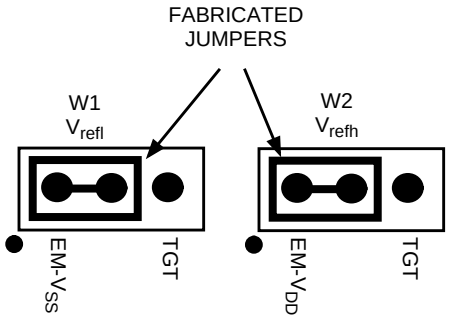
Jumper Header	Position	Description	Factory Setting
A/D Converter Voltage Reference Headers, W1 and W2		Tie V_{refl} to ground and V_{refh} to +5 Vdc.	X
		Tie V_{refl} and V_{refh} pins to their respective input pins on connectors J2 and J3.	
BDLC, TXP, and RXP Control Headers, W3 and W4		Tie TXP and RXP pins to their respective pins on connectors J2 and J3.	X
		The HC57 position currently is not used.	
		Tie TXP and RXP pins to use the HIP7020 transceiver circuits. Position W5 to 7020 position. Transceiver connection is at BUS terminal of P3.	
BUS Control Header, W5		The HC57 position currently is not used.	
		Tie BUS connection at P3 to HIP7020 transceiver circuits.	X

Table 4. Jumper Header Positions (Continued)

Jumper Header	Position	Description	Factory Setting
IRQ Volts Select Header, W6		Normal usage is 12 volts during reset, 5 volts during operation.	X
		V_{batt} voltage at P3 is tied to the $\overline{IRQ}$ pin.	
Clock Source Select, W7		Select the 4.194304-MHz crystal oscillator located on the EM board at Y1.	X
		Select the 4-MHz canned oscillator located on the EM board at XY2.	
		Select the clock originating from the platform board. The frequency, set to 2 MHz on power up, is controlled by the OSC command.	
		Select a user-supplied clock source. The clock is input to the TOSC1 pin on connector J3 through a target cable assembly.	
Gauge Control Headers, W8, W9, and W10		Tie V_{gref}, V_{GSUP}, and V_{PGC} pins to their respective pins on connectors J2 and J3. The required external circuitry for gauge driver power supply should be on the target system.	X
		Utilize the on-board voltage regulator. Ties V_{gref}, V_{GSUP}, and V_{PGC} pins to required circuits populated on EM. A V_{batt} voltage should be connected to P3.	
		Enable V_{GSUP} to drive gauges connected to J2 and J3 while utilizing the on-board voltage regulator. Ties V_{gref}, V_{GSUP}, and V_{PGC} pins to required circuits populated on EM. V_{batt} required at P3.	

A/D Converter Voltage Reference Headers – W1 and W2

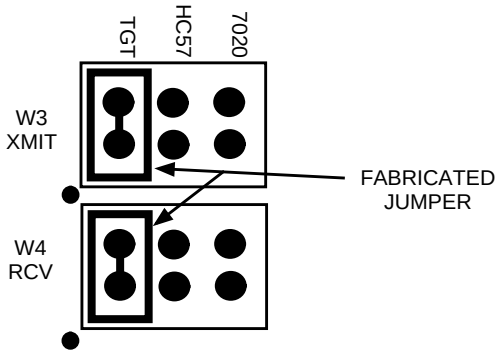
The A/D voltage reference headers control the input to the voltage reference low pin (V_{refl}) and the voltage reference high (V_{refh}) pin of the MCU. The factory configured position applies the EM ground to the V_{refl} pin and +5 volts to the V_{refh} pin.



Alternatively, the reference voltages can be supplied through the target cable connected to connectors J2 and J3 of the M68EM05V12 emulation module. To do so, reposition the W1 and W2 jumper to the TGT position.

BDLC XMIT and RCV Control Headers – W3 and W4

The transmit and receive headers control the path of the transmit and receive signals of the BDLC subsystem. The factory configured position, TGT, routes the lines directly to the target connectors J2 and J3.



Alternatively, the transmit and receive lines can be routed to utilize the Harris HIP7020 circuits populated on the emulation module. If W3 and W4 are configured to use this circuit, then header W5 must be configured to the 7020 position to route the transceiver's BUS signal to the BUS lever terminal of connector P3.

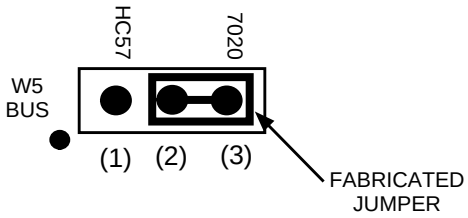
To use the HIP7020 transceiver circuits, position the W3 and W4 jumpers in the 7020 position. Ensure that the associated components are populated. They are:

- R2 62 kΩ
- R3 15 kΩ
- U10 HIP7020, 8-pin SOIC package
- C7 0.1 μF
- TP1 1-pin header connected to the loop back enable

Note that the HC57 position of W3 and W4 jumpers is not used.

BUS Control Header – W5

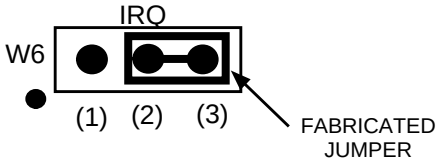
Jumper header W5 controls the path of the BUS signal to and from the HIP7020 transceiver circuits. In the 7020 position, the BUS signal from the HIP7020 transceiver circuits is connected to the BUS lever terminal of connector P3. Note that proper configuration of this header is dependent on configuration of BDLC headers W3 and W4.



The HC57 position is not used on the M68EM05V12 emulation module.

IRQ Volts Select Header – W6

Jumper header W6 controls the source voltage applied to the MCU's $\overline{IRQ}/V_{PP}$ pin. The diagram below shows the factory configuration. The fabricated jumper between pins 2 and 3 selects the normal configuration. For normal use, the system applies a +12-V charge pump voltage to the $\overline{IRQ}/V_{PP}$ pin during reset. Out of reset, the system supplies +5 volts to the $\overline{IRQ}/V_{PP}$ pin, unless the IRQ input is asserted low.



The +12 volts from the charge pump is not adequate to program the EPROM of an MC68HC705V12 MCU. Instead, to program this EPROM, you must apply the V_{epgm} voltage (supplied through V_{batt} terminal of connector P3). To do so, reposition the W6 fabricated jumper between pins 1 and 2.

CAUTION: *When removing power from the system, remove the V_{batt} voltage before you turn off the MMDS power switch. Doing otherwise could damage the emulation circuits.*

See **Using Lever Terminal Connector P3** on page 28 for more information about connector P3.

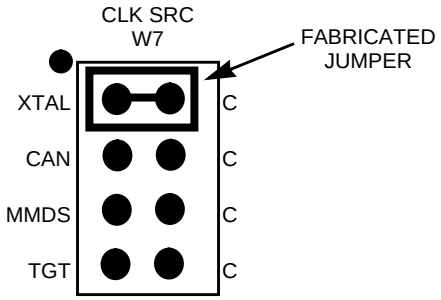
Clock Source Select Header – W7

Jumper header W7 is used to determine the source of the clock signal. The diagram here illustrates the jumper header where the pins marked C indicate common pins. The default configuration selects the 4.194304- MHz crystal clock source at location Y1.

The 4-MHz canned oscillator clock source at board location XY2 can be selected by positioning the shunt between CAN and C.

There are two other possible clock sources. One source, from the platform board, requires repositioning the W7 jumper between pins MMDS and C and then using the system's OSC command to select a frequency.

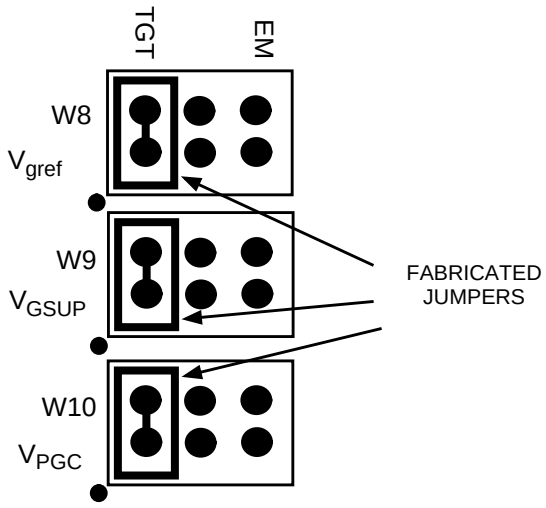
For a user-supplied clock source, coming through target cable that is connected to J2 and J3, reposition the W7 jumper between TGT and C.



NOTE: *The user-supplied source through the target cable should be a CMOS-level square wave.*

Gauge Control Headers – W8, W9, and W10

The gauge headers control the path of the V_{gref}, V_{GSUP}, and V_{PGC} signals of the gauge driver subsystem. The factory-configured position, TGT, routes the lines directly to the target connectors J2 and J3.



Alternatively, these headers can be configured to utilize the voltage regulator circuits populated on the M68EM05V12 emulation module. For this option, position the fabricated jumpers in the EM position. Note that if the emulation module voltage regulator circuits are used, you must supply +12 volts to the V_{batt} lever terminal of connector P3.

CAUTION: *When removing power from the system, remove the V_{batt} voltage before you turn off development system power. Doing otherwise could damage the emulation circuits.*

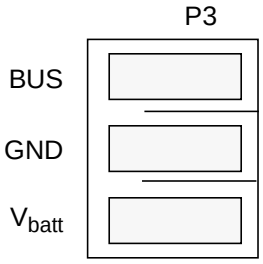
If you want the EM voltage regulator circuits to drive gauges (through V_{GSUP}) connected to the M68EM05V12 emulation module target connectors J2 and J3, position an additional jumper in the V_{GSUP} (W9) header, so that a jumper resides in both the TGT and EM positions.

Using Lever Terminal Connector P3

Lever terminal connector P3 is a 3-pin connector. The diagram below illustrates the component where the V_{batt} input would be used for inputting a 12-Vdc supply to power the on-board voltage regulator circuits.

The BUS terminal is used for the transceiver I/O when utilizing the on-board transceiver circuit.

The GND terminal is for connecting to on-board ground when utilizing one of the other terminals.



CAUTION: *To avoid damaging emulator circuits, the development system voltage must be turned on before you supply the V_{batt} source voltage through the P3.*

Remaining System Installation

When headers W1–W10 have been configured, you have completed M68EM05V12 configuration.

- Ensure that the power to the development tool is off.
- If installing the M68EM05V12 in an MMDS station module, remove the panel from the station module top.
- Fit together EM connectors P1 and P2 on the bottom of the board and platform board DIN connectors. Snap the corners of the EM onto the plastic standoffs.
- Connect the target cable, if appropriate.
- If installing in an MMDS, replace the panel.

At this point, you are ready to make remaining cable connections, as necessary, and restore power.

For instructions, consult either the *MMEVS05/MMEVS08 Operations Manual* (MMEVS0508OM/D) or *MMDS0508 Operations Manual* (MMDS0508OM/D).

Personality Files Usage

The development system uses a specific personality file to emulate an MC68HC(7)05V12 MCU: file 00029Vxx.MEM. The debugger software loads this personality file upon power-up. The file is on an individual disk shipped with the M68EM05V12.

NOTE: *Note that personality file names follow the pattern 00ZZZVxx.MEM, where ZZZ is the EM identifier or MCU name and xx is the version of the file.*

MC68HC(7)05V12 Emulation

NOTE: *Be aware that if the computer operating properly (COP) mask option has been selected as enabled, your code must clear the COP watchdog timer counter to avoid a COP reset. The counter is cleared by writing a logic 0 to bit 0 at location $3FF0. This should be the first check when code is not operating as expected.*

The following information details known differences between the performance of an MC68HC705V12 MCU run in single-chip operation versus the way certain features will perform during emulation.

Mask Option Register (MOR) Control

In single-chip mode operation:

The MCU mask options will be determined by which options have been programmed in the MOR EPROM location ($3C00). This register must be programmed using a dedicated programmer.

In emulation:

The MCU mask options initially are determined by which options have been programmed in the MOR EPROM location ($3C00). This register must be programmed using a dedicated programmer.

Alternatively, the mask options can be controlled via software and allow setting of mask options during a debug session.

The procedure for changing options during an emulation session requires manipulation of the EPROM programming register at location $000D and the MOR location ($3C00). Option changes can be accomplished by command entry (for instance, the MM command) or by execution of user code (for instance, STA instruction). First set bit 7 (MORON bit) by writing $80 to the EPROM programming register. If you use the memory modify (MM) command, a “Write did not verify” message should be ignored. Then write the desired mask option register byte value to the MOR location ($3C00).

On the emulator, a MOR RAM register will be written to when the user attempts to write to the MOR location. The MCU will logical OR the MOR EPROM bits with the MOR RAM bits. This results in the ability

to select a previously disabled mask option, but previously selected mask options (programmed in the MOR EPROM) cannot be defeated. Mask option selections take effect immediately. Any reset will deselect mask options selected by writing to the MOR RAM location.

Reading the Mask Option Register

In single-chip operation:

The data read at location $3C00 is determined by the MORON bit (bit 7) in the programming register. By setting the MORON bit, the data read at $3C00 will be the contents of the EPROM mask option register. When the MORON bit is cleared, the first byte of the boot ROM code is located at $3C00.

In emulation:

Like single-chip, the user is able to verify the contents of the EPROM MOR location by first setting the MORON bit in the programming register. However, changes made to mask options during a debug session by using the method outlined in **Mask Option Register (MOR) Control** above cannot be verified directly by reading back of any location. The user must test the mask option enabled to verify that it is indeed being enabled.

$\overline{IRQ}/V_{PP}$ Input Pin

In single-chip mode:

The $\overline{IRQ}/V_{PP}$ pin drives the asynchronous IRQ interrupt function of the CPU. The pin also is used for programming voltage when programming the user EPROM or the MOR.

In emulation:

The $\overline{IRQ}/V_{PP}$ signal supplied to connector J2 through a target cable drives only the asynchronous IRQ interrupt function.

NOTE: *A V_{PP} voltage should not be supplied to the $\overline{IRQ}/V_{PP}$ pin in a target application while the emulator is connected.*

Pullup on $\overline{IRQ}$

In single-chip mode:

The $\overline{IRQ}$ pin has no pullup. Your application must pull the $\overline{IRQ}$ pin to V_{DD} level to prevent interrupts.

In emulation:

The $\overline{IRQ}$ pin is pulled up on the module. Be aware that an application without the $\overline{IRQ}$ pin pulled high will emulate correctly but will fail in the application because of a floating IRQ line. The $\overline{IRQ}$ pin pulled high on the module causes these results.

Programming the 256-Byte EEPROM Array

In single-chip mode operation:

The 256-byte EEPROM array at locations $0240 to $033F can be programmed during normal operation of the device. User code modifies the array on a single byte basis by manipulation of the programming register located at address $001C.

In emulation:

Like single-chip, the 256-byte EEPROM array can be programmed during normal operation of the device. User code modifies the array on a single byte basis by manipulation of the programming register located at address $001C.

Alternatively, the array can be modified using memory altering commands of the debugger. The commands that will modify the array are assemble (ASM), block fill (BF), load S19 file (LOAD), and memory modify (MM).

Illegal Address Operation

In single-chip:

The MCU will be reset internally on an opcode fetch of an illegal address.

In emulation:

The reset will not occur. Instead, the MCU will set a latched bit that can be read at bit 3 of register $3F. The bit is cleared by any reset.

Schematics

Contents

M68EM05V12 Schematics

Refer to the six sheets of schematics for the M68EM05V12 emulation module.

Schematics

M68EM05V12 Schematics (Sheet 1 of 6)

NOTES, UNLESS OTHERWISE SPECIFIED

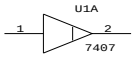
1. VCC PIN LOCATIONS :

   VCC IS APPLIED TO PIN 8 OF ALL 8-PIN IC's, PIN 14 OF ALL 14-PIN IC's, PIN 16 OF ALL 16-PIN IC's, PIN 20 OF ALL 20-PIN IC's, ETC.

2. GROUND PIN LOCATIONS :

   GROUND IS APPLIED TO PIN 4 OF ALL 8-PIN IC's, PIN 7 OF ALL 14-PIN IC's, PIN 8 OF ALL 16-PIN IC's, PIN 10 OF ALL 20-PIN IC's, ETC.

3. DEVICE TYPE, PIN NUMBERS, AND REFERENCE DESIGNATOR OF GATES ARE SHOWN AS FOLLOWS :



7407 = DEVICE TYPE
1 AND 2 = PIN NUMBERS
U1A = REFERENCE DESIGNATORS

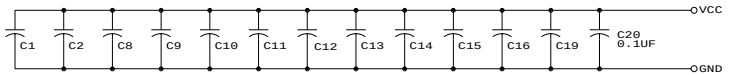
4. RESISTANCE VALUES ARE IN OHMS.
5. RESISTORS ARE 1/4 WATT, 5%, UNLESS OTHERWISE SPECIFIED.
6. CAPACITANCE VALUES ARE IN MICROFARADS, 10%.

M68EM05V12 EMULATION MODULE

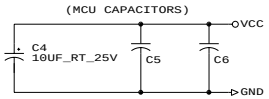
REVISIONS

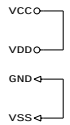
ECN #	PCB REV	SCH REV	DESCRIPTION	DATE
	O	1	First Rev of PWB	9/30/95
107	O	2	Correct the logic used for latching DDRC and PORTC data.	4/5/96
113	O	3	Do cuts and jumps to support pin swap on Rev 2.0 silicon.	5/30/96

Decouple Caps for ICs as labeled.
All caps are 0.1 uF @ 50 V

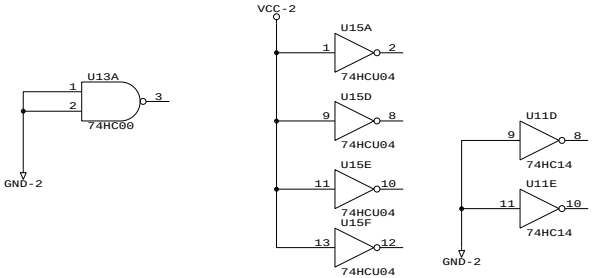


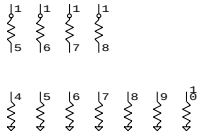
(MCU CAPACITORS)





Spare Gates





0RCAD 386+ FLAT FILES

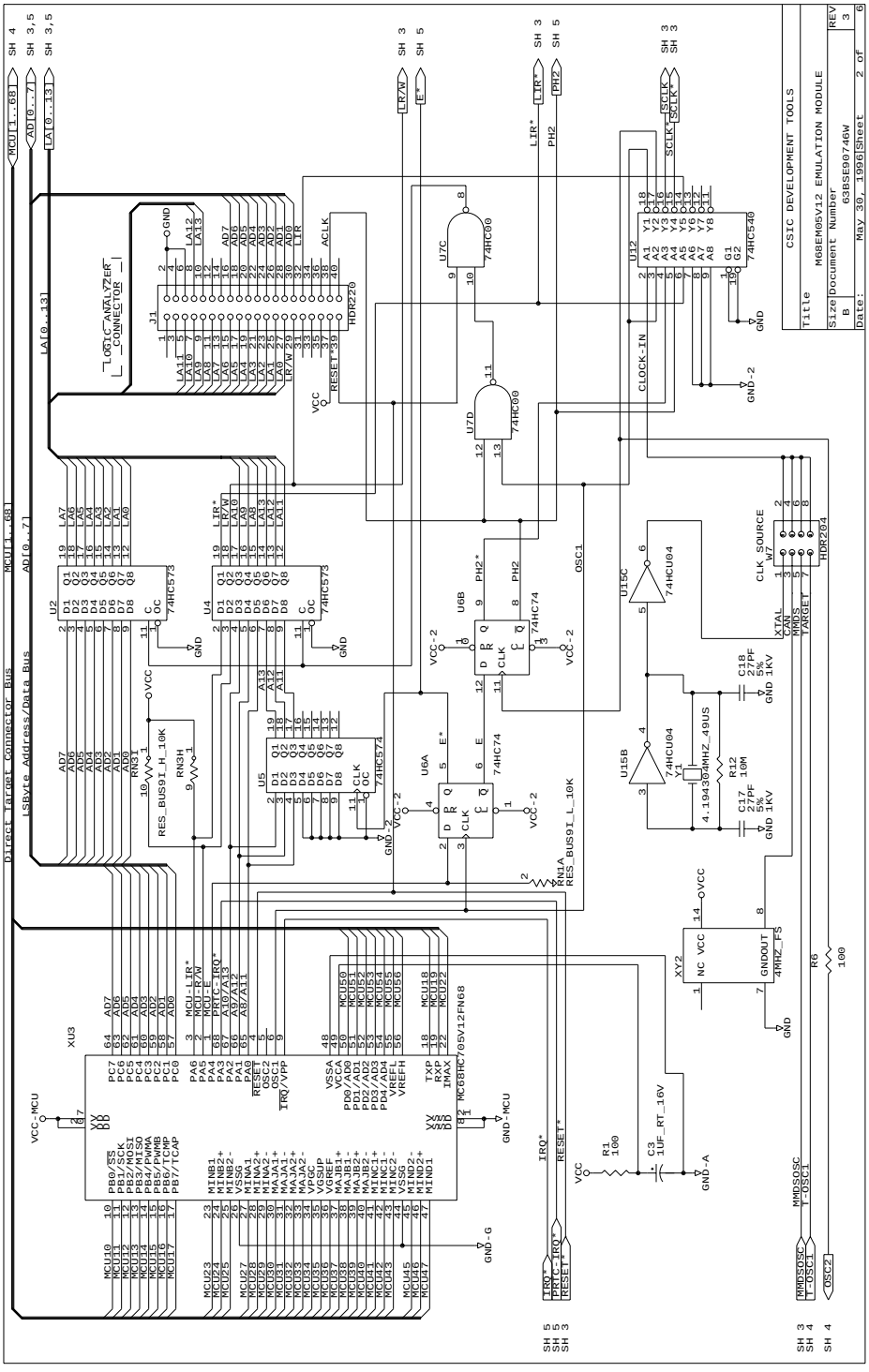
LINK
5V12R3S2.SCH
5V12R3S3.SCH
5V12R3S4.SCH
5V12R3S5.SCH
5V12R3S6.SCH

COMPUTER GENERATED DRAWING : DO NOT REVISE MANUALLY

CSIC DEVELOPMENT TOOLS		
Title: M68EM05V12 EMULATION MODULE		
Size: B	Document Number: 63BSE90746W	REV: 3
Date: May 30, 1996	Sheet 1 of 6	

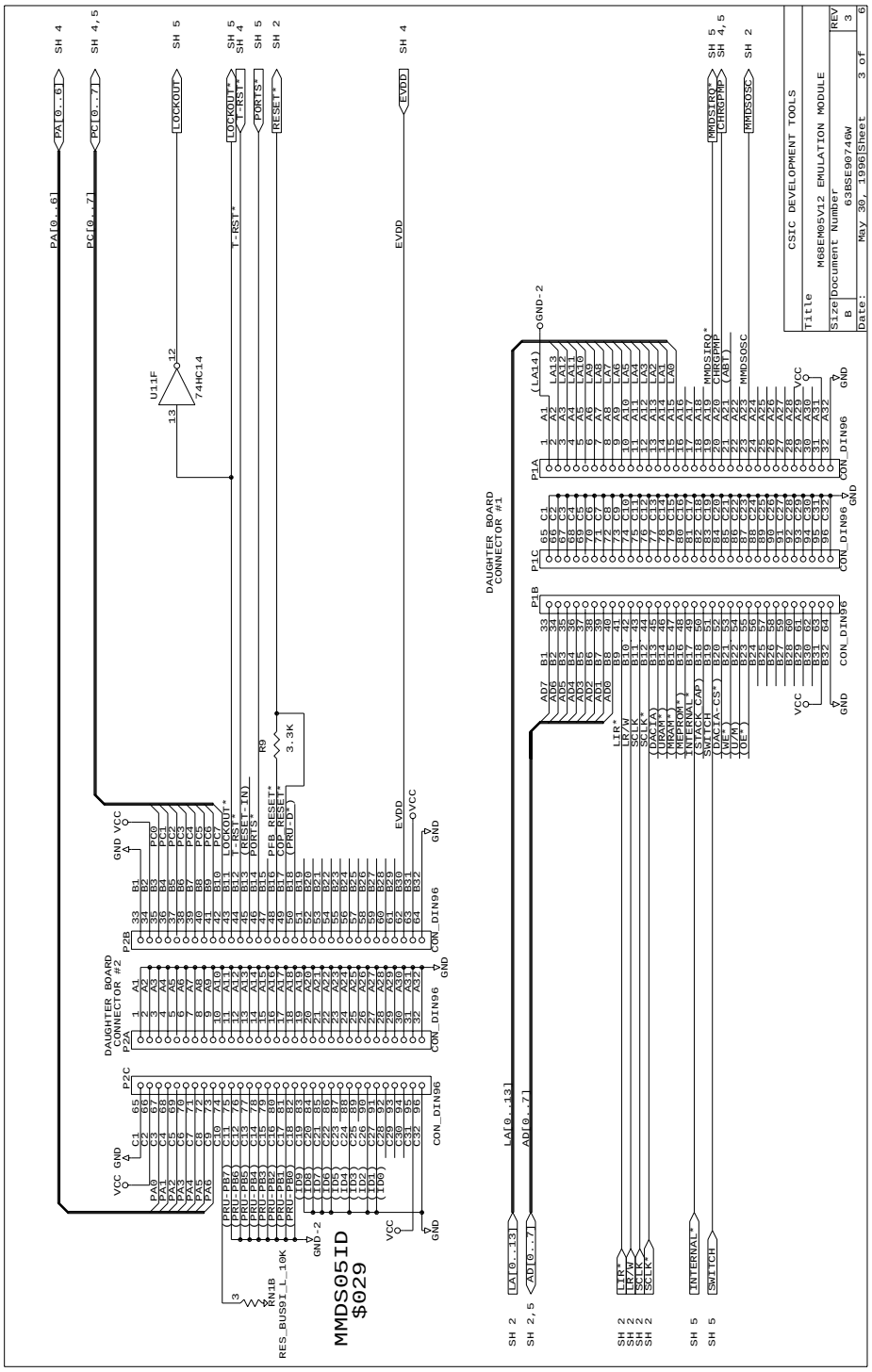
Schematics

M68EM05V12 Schematics (Sheet 2 of 6)



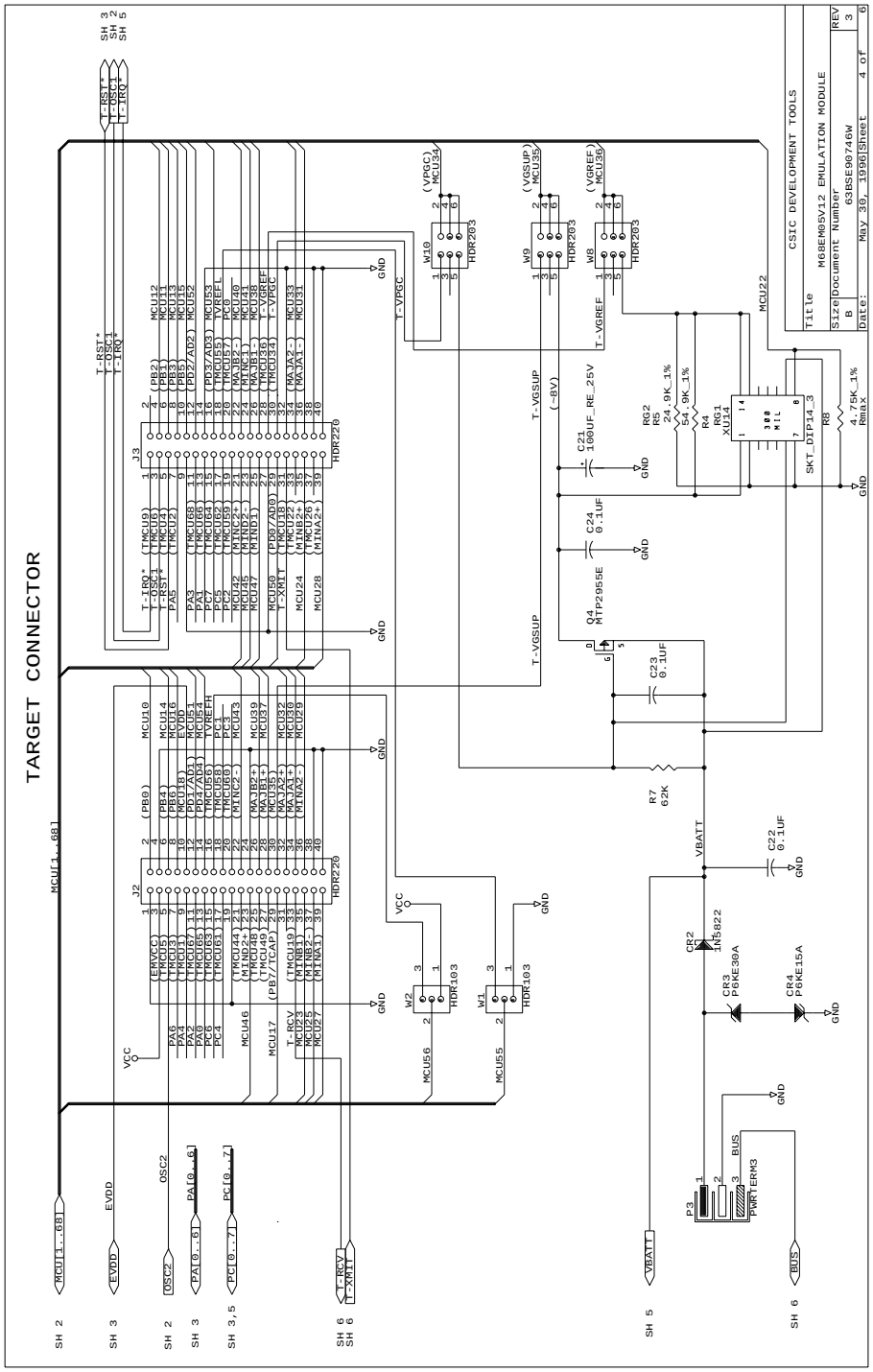
Schematics

M68EM05V12 Schematics (Sheet 3 of 6)



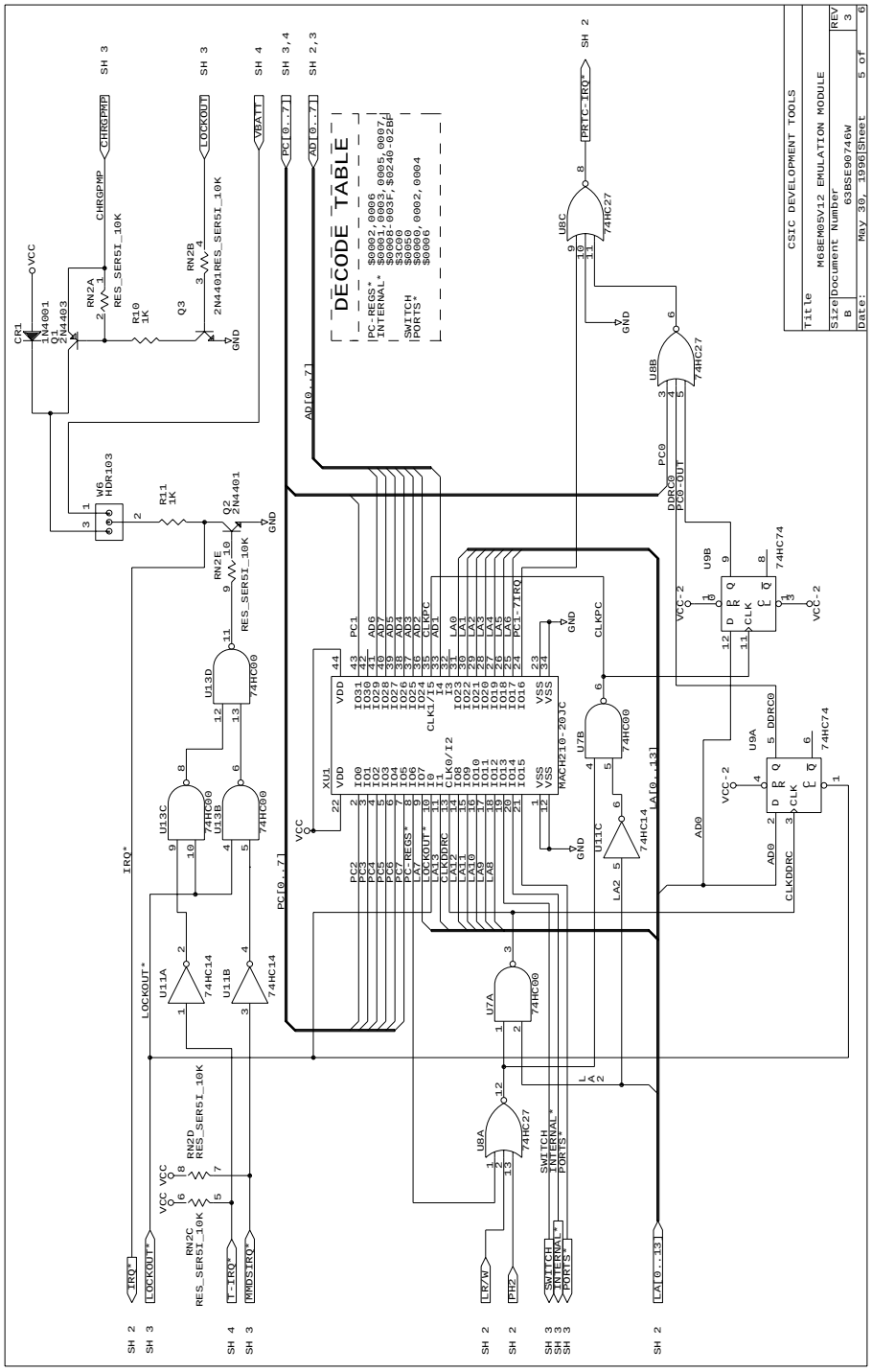
Schematics

M68EM05V12 Schematics (Sheet 4 of 6)



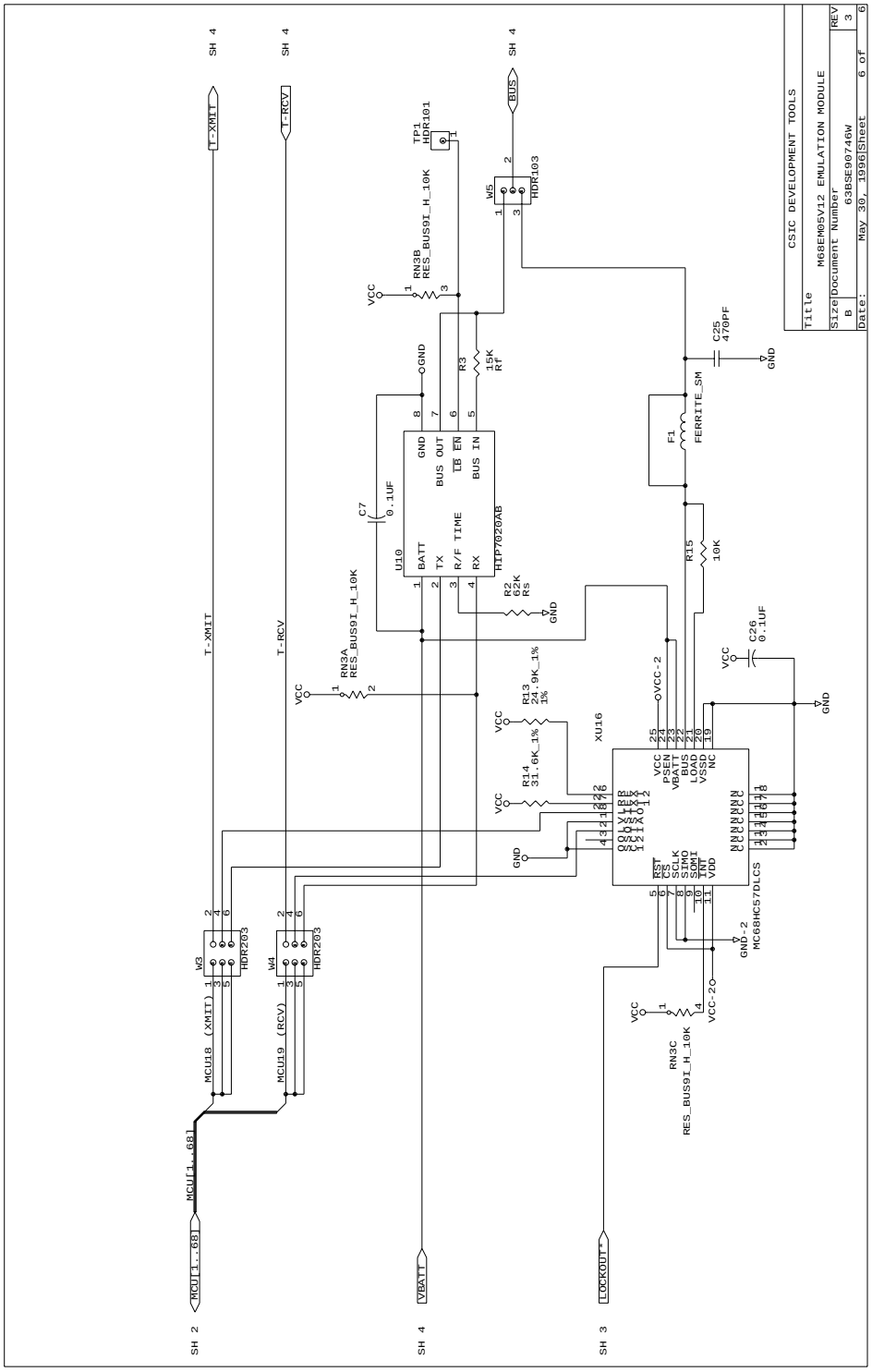
Schematics

M68EM05V12 Schematics (Sheet 5 of 6)



Schematics

M68EM05V12 Schematics (Sheet 6 of 6)



Schematics