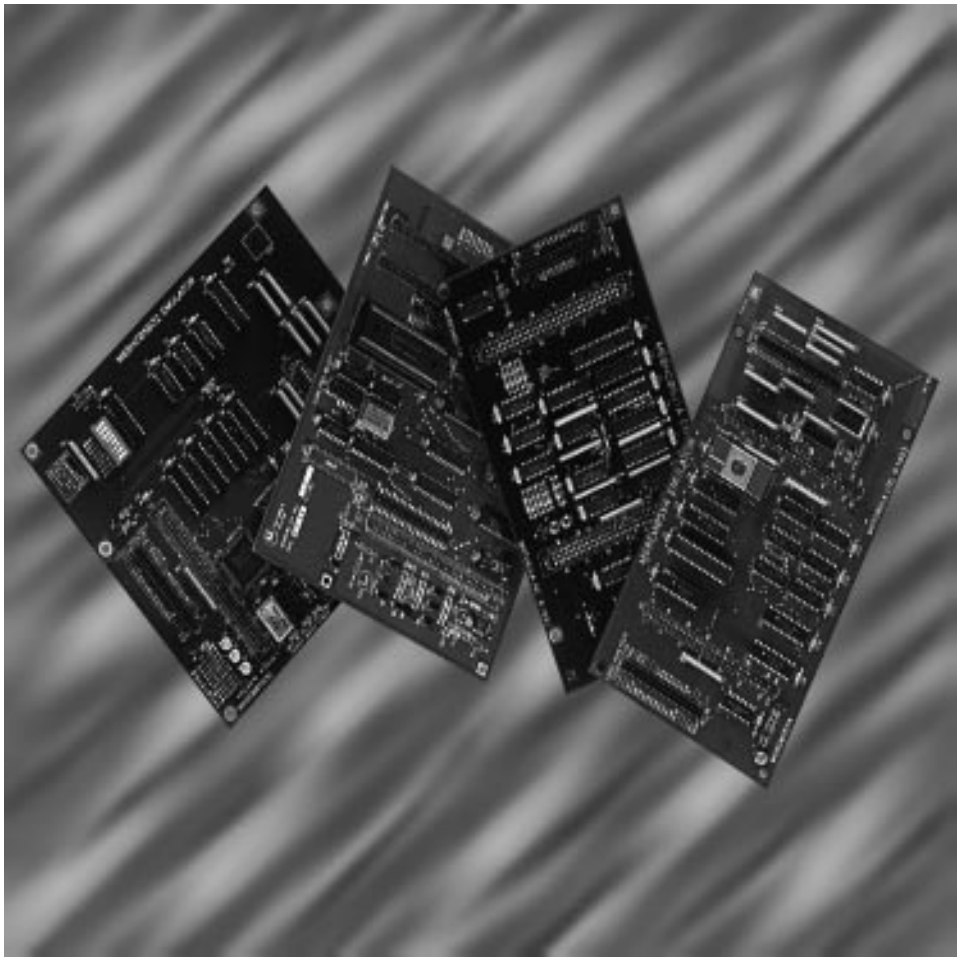
M68EM08AX48UM/D
Rev. 1.0

# M68EM08AX48

## EMULATION MODULE
## USER'S MANUAL



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# M68EM08AX48

## Emulation Module
## User's Manual

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## Revision History

This table summarizes differences between this revision and the previous revision of this emulation module user's manual.

| | |
|---|---|
| **Previous Revision** | None |
| **Current Revision** | Original release |
| **Date** | 09/96 |

# Revision History

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# General Description

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## Introduction

The M68EM08AX48 gives your Motorola development tool the ability to emulate target systems based on MC68HC08AX48 microcontroller units (MCUs). The MC68HC08AX48 is designed to be a 5 V-only emulator, operating at 5 volts and up to an 8-MHz bus frequency.

By substituting a different emulation module (EM), your Motorola development tool can be enabled to emulate other MCUs. Refer to *Motorola's Development Tool Selector Guide*, order number SG173/D, for a complete list of available EMs.

This hardware user's manual explains connection, configuration, and operation information specific to the M68EM08AX48 emulation module. The module can be installed in two Motorola development systems. To configure your M68EM08AX48 for either an MMDS or an MMEVS, follow the instructions given in **Configuration and Operation** on page 15.

In this manual, MMDS0508 and MMEVS0508 are referred to as MMDS.

## Emulation Components

Motorola's complete emulation system consists of the emulation module described in this manual as well as other separately purchased options described in the following paragraphs.

The following items are included with the M68EM08AX48 emulation module:

- **An M68EM08AX48 emulation module (EM)** — The printed circuit board that enables system functionality for M68EM08AX48 MCUs. The female connectors, on the bottom of the module, mate with male connectors on a development system platform board. The EM also has a connector for the target cable assembly.
- **Configuration software** — 3 1/2-inch diskette containing personality files for this module.

Separately purchased Motorola modular development tool options include:

- **An MMEVS0508 platform board (M68MMPFB0508)** — The MMEVS is an economical development tool that provides real-time in-circuit emulation. The unit's integrated design environment includes an editor, an assembler, a user interface, and a source-level debugging program.
- **An MMDS0508 modular development system (MMDS0508)** — The MMDS is a high-performance development tool that has all the capabilities of the MMEVS. In addition, it also has a bus state analyzer and real-time memory windows.
- **Flex cable target assembly** — Refer to **Target Cable Assemblies** on page 12 for more information.

User supplied components include:

- **Host computer** — see the appropriate development tool user's manual for minimum requirements.
- **Power supply** — +5 Vdc @ 1.0 amp required for the MMEVS.

## EM Layout

**Figure 1** on page 11 shows the layout of the M68EM08AX48. Connector J1 connects to an optional logic analyzer. Target connectors J2 and J3 are the interface to a target system. Terminal connector P1 allows the user to supply an external battery voltage and monitor the bus signal. **Connector Information** on page 23 gives pinouts and signal descriptions for these connectors.

Test point TP1 is a test signal for the analog transceiver module, if bonded out on the MCU installed in XU3. Headers W1–W3 and W6 allow use of either target-based or local signals. W4 and W5 allow loading options for testing minimum or maximum loading. The MC68HC08 device is run by an oscillator clock selected by W7. Expansion header connectors P2 and P3 connect the EM and the control board.

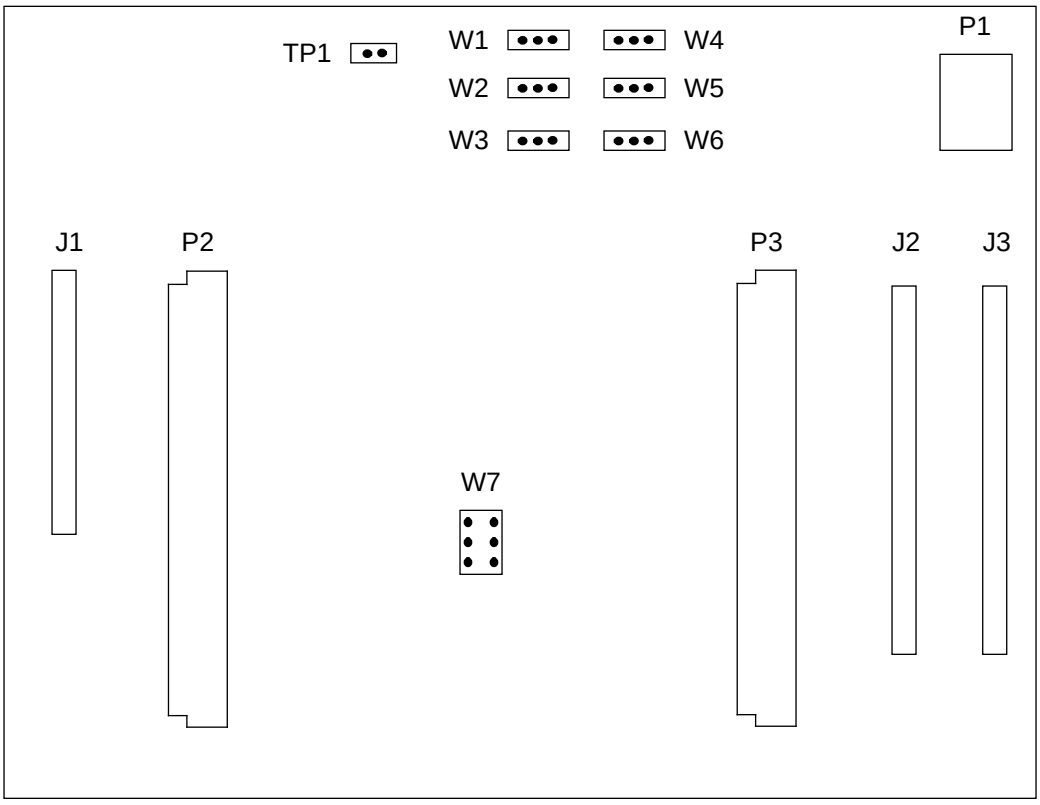


**Figure 1. M68EM08AX48 Emulation Module**

## Target Cable Assemblies

To connect your M68EM08AX48 to a target system, you need a separately purchased target cable assembly. Cable assemblies are available for the 64-pin QFP and 52-pin PLCC MCU packages.

The target cable connects to the emulator via connector J2 and J3 on the M68EM08AX48 emulation module. Pin assignments and signal descriptions for connectors J2 and J3 can be found in **Target Cable Connectors – J2 and J3** on page 26.

**Figure 2** represents a target cable assembly. An assembly for 64-pin QFP package consists of a flex cable and a QFP target head adapter. The assembly for 52-pin PLCC consists of a flex cable and a PLCC target head adapter. One end of the flex cable plugs onto M68EM08AX48 connector J2 and J3 with orientation shown in **Figure 2**. The other end of the flex cable plugs into the target head adapter. The 64-pin QFP target head adapter then inserts into a TQSOCKET and then a TQPACK installed on the users target system. The 52-pin PLCC target head adapter inserts into a PLCC footprint in a target system.

The MCU package in your target system determines the target cable assembly components required:

- For a 64-pin QFP package, use flex cable M68CBL05C and target head adapter M68TC08AX48FU64. A TQSOCKET w/guides (M68TQS064SAG1) and a TQPACK (M68TQP064SAM01) are included with the target head adapter.
- For a 52-pin PLCC package, use flex cable M68CBL05B and target head adapter M68TB08AX48B52.

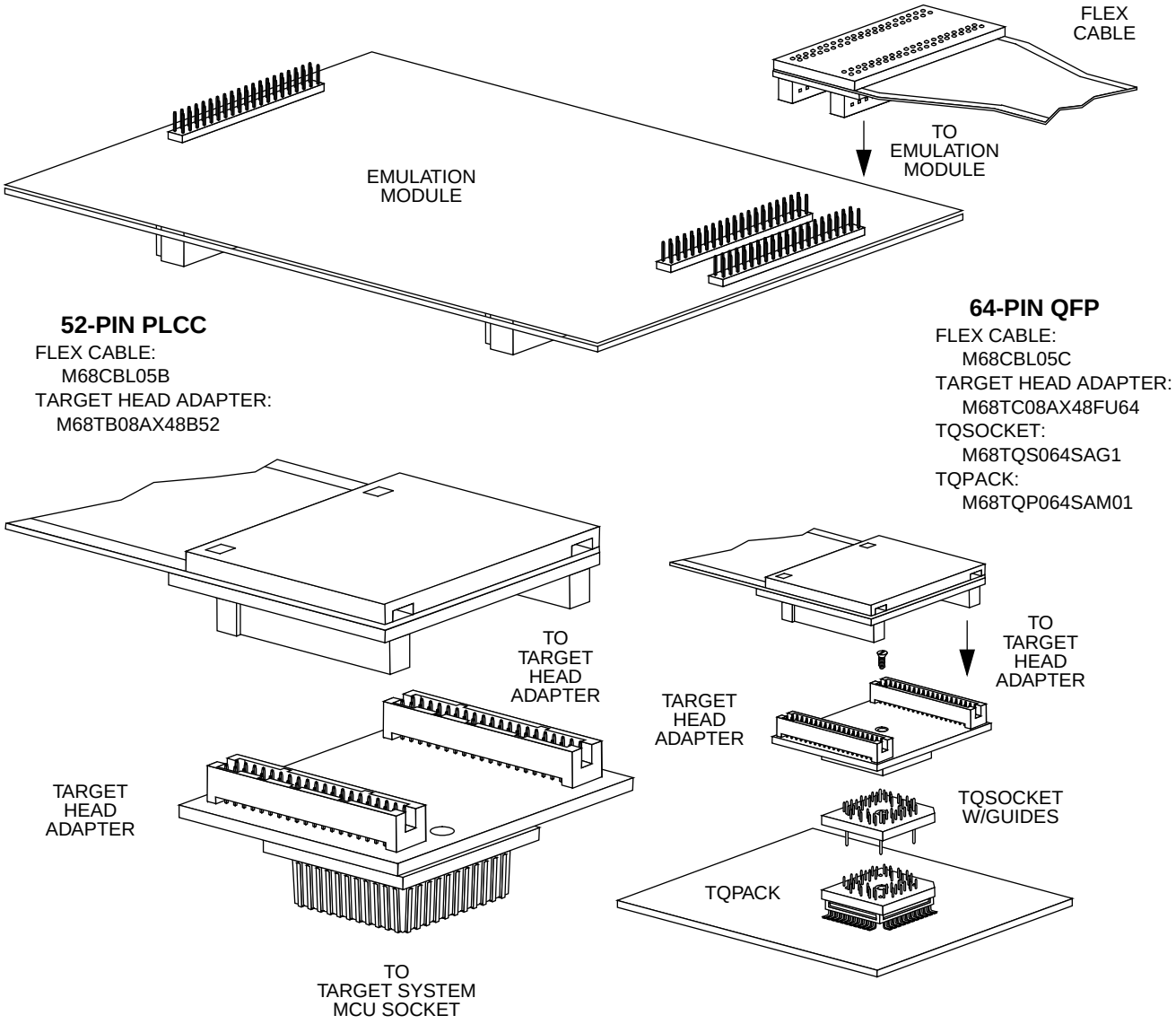


**Figure 2. Target Cable Assembly**

# Configuration and Operation

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## Introduction

The following paragraphs explain how to configure and use your M68EM08AX48 as part of an MMDS or MMEVS system. For other parts of system installation and configuration, see either the *MMDS0508 Operations Manual* (MMDS0508OM/D) or *MMEVS0508 Operations Manual* (MMEVS0508OM/D).

The topics covered in this chapter are:

- **Setting M68EM08AX48 Jumper Headers** on page 17 explains how to set the M68EM08AX48 jumper headers.
- **Remaining System Installation** on page 21 covers the final steps to system installation.
- **Setting M68EM08AX48 Jumper Headers** on page 17 explains how to adjust the M68EM08AX48 MCU operating voltage.
- **Personality File Usage** on page 20 discusses the personality file used on the M68EM08AX48 board.
- **MC68HC08AX48 Emulation** on page 20 explains special considerations for emulating with this module.

***NOTE:*** *You can configure an* M68EM08AX48 *already installed in the system platform board. To do so, remove system power and then follow the guidance of this chapter.*

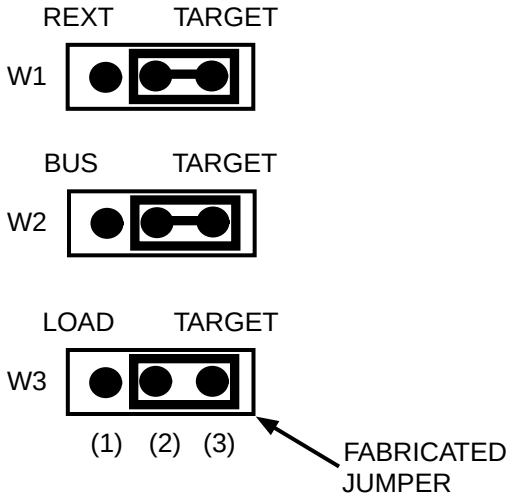
***CAUTION:*** *Be sure to switch off power before you reconfigure an installed EM. Reconfigure EM jumper headers with the power on can damage emulation circuits.*

## Setting M68EM08AX48 Jumper Headers

Your M68EM08AX48 has seven user-selectable jumper headers – W1 through W7. **Digital BDLC Bond Out Option**, **Analog Transceiver Bond Out Option** on page 18, and **Clock Source Select Header – W7** on page 19 explain how to configure these components. The M68HC08AX48 can be bonded out in two different configurations: one with the analog transceiver and the other with the digital BDLC.

### Digital BDLC Bond Out Option

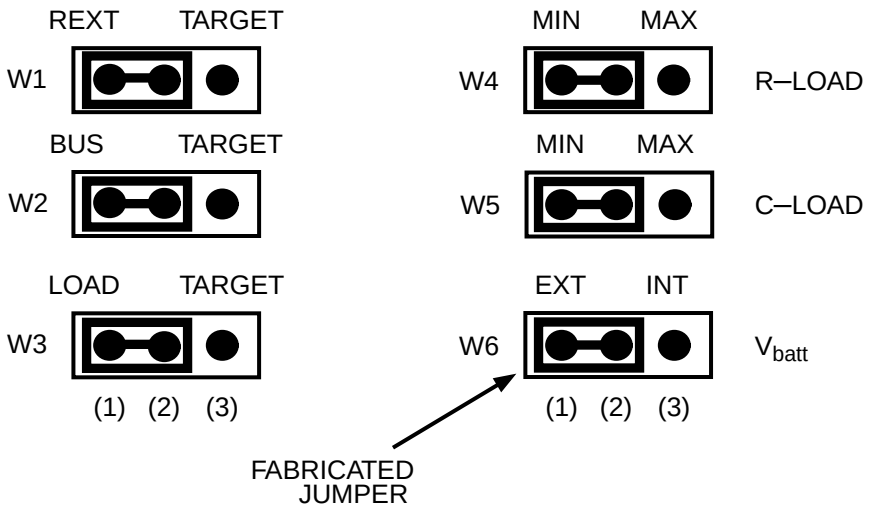
Jumper headers W1–W3 should be set in the pin 2–3 position; this allows MCU pins 9, 10, and 12 to be routed to the target connector J2 pins 5 and 6 and J3 pin 8, respectively. W4–W6 have no effect in the digital bond out.




W4 – W6 – NO EFFECT ON MCU

### Analog Transceiver Bond Out Option

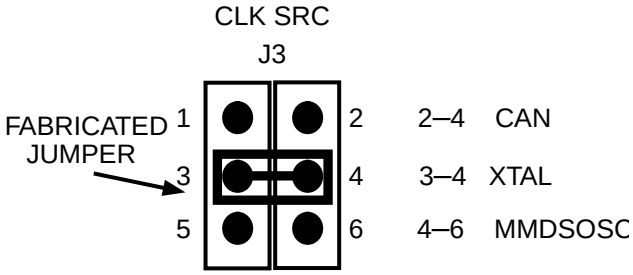
Jumper headers W1–W3 can be in the pin 1–2 position, allowing the MCU pin 9 to be connected to a 1%, 31.6-K resistor. MCU pins 10, 11, and 12 are connected to a loading circuit with W4, W5, and W6, supplying the load and $V_{batt}$ source. For minimum resistive load (11 K ohms), W4 should be set in position 1–2. A 330 ohm load is set when in position 2–3. For minimum capacitive load (470 pF), W5 should be set in position 1–2. A 0.015-µF load is set when in position 2–3. W6 is used to determine the source of $V_{batt}$, MCU pin 12. In position 1–2, the user must supply the voltage through terminal connector P1 pin 3. In position 2–3, the $V_{batt}$ voltage is supplied by an on board +12 volts. You can install jumpers in the 2–3 position and in headers W1–W3 and provide your own REXT and bus loading components in his target application. In this case, jumpers W4–W6 have no effect.



**Clock Source Select Header – W7**

Jumper header W7 is used to determine the source of the clock signal. The diagram below shows the factory configuration: The W7 fabricated jumper between pins 3 and 4 selects the crystal oscillator clock source (at board location Y2). This is the default selection.

The other possible clock sources originate from the MMDS control board or from a user-supplied CAN oscillator clock source (at board location XY1). For the MMDS frequency, reposition the W7 jumper between pins 4 and 6, then use the MMDS OSC command to select a frequency. For the CAN oscillator source, reposition the W7 jumper between pins 2 and 4, and supply the desired CAN oscillator in socket XY1.



## Personality File Usage

Your MMDS uses a specific personality file to emulate an MC68HC08AX48 MCU: file 00417Vxx.MEM. This file is included on a separate disk shipped with the M68EM08AX48. This file name follows the pattern for all personality files, **00ZZZVxx.MEM**, where **ZZZ** is the EM identifier of MCU name and **xx** is the version of the file.

The purpose of memory definitions is seen in the way the MMDS handles writes to the two memory types. During user code execution, attempts to write to a location mapped as ROM will generate a write protect error, and user code execution is halted. Code should never write to a ROM location. A write to a location mapped as RAM does not stop code execution.

With an understanding of MMDS handling of memory mapping, the user can customize the MMDS to emulate within the needs of the application. The memory settings may be altered using the MMDS SETMEM command.

## MC68HC08AX48 Emulation

**Notes**

The MC68HC08AX48 comes with various bond out options. The analog transceiver and digital BDLC can be bonded out differently. Make sure that the correct MCU is installed.

**Differences**

There are no known differences between the performance of an MC68HC08AX48 MCU run in single-chip operation or how certain features will perform during emulation.

## Remaining System Installation

When headers W1–W7 have been configured, the M68EM08AX48 has been reconfigured.

- Ensure that the power to the development tool is off.
- If installing the M68EM08AX48 in an MMDS station module, remove the panel from the station module top.
- Fit together EM connectors P1 and P2 (on the bottom of the board) and platform board DIN connectors. Snap the corners of the EM onto the plastic standoffs.
- Connect the target cable, if appropriate.
- If installing in an MMDS05, replace the panel.

At this point, you are ready to make remaining cable connections, as necessary, and restore power.

For instructions, consult either the *MMEVS05/MMEVS08 Operations Manual* (MMEVS0508OM/D) or the *MMDS0508 Operations Manual* (MMDS0508OM/D).

## Troubleshooting

If the emulator board fails to communicate with the host computer, the following tests may help isolate the cause:

- Check the RS232 connections, if the correct COM port is identified on the command line, and if power is on. Refer to the operations manual for more information.
- Check for an oscillator at header W3 pin 4. See **Clock Source Select Header – W7** on page 19 for more information.
- Check for T12 on the logic analyzer connector. If this is not present, the part may be in stop, wait, single-chip, or reset modes.

# Connector Information

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## $V_{batt}$ Supply and Bus Connector – P1

**Figure 3** shows the pin assignments for terminal connector – P1, which supplies the user-supplied voltage to the $V_{batt}$ pin (MCU pin 11) and BUS signal (MCU pin 10). These signals are used only if the analog transceiver is bonded out.


**Figure 3. Terminal Connector – P1**

## Logic Analyzer Connector – J1

**Figure 4** shows the pin assignments for logic analyzer connector – J1. This connector provides for easy access of many of the signals used internally to the emulator. **Table 1** on page 25 lists signal descriptions for this connector.

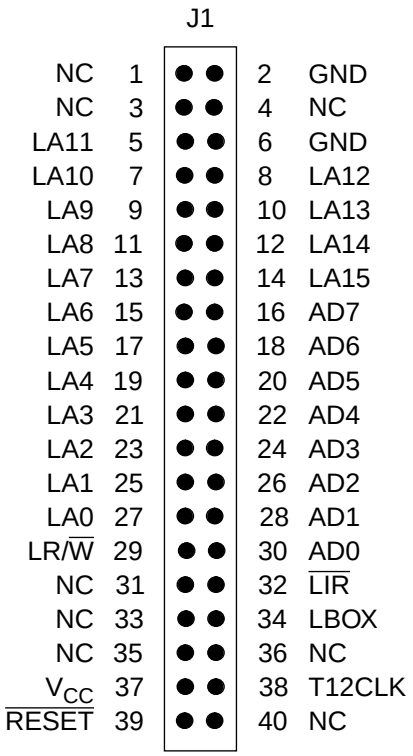


**Figure 4. Connector – J1 Signal Descriptions**

## Table 1. Connector – J1 Signal Descriptions

| Pin | Mnemonic | Signal |
|---|---|---|
| 1, 3, 4, 31, 33, 35, 36, 40 | NC | No Connection |
| 2, 6 | GND | Ground |
| 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27 | LA11–LA0 | Latched Address (Bits 11–0) |
| 8, 10, 12, 14 | LA12–LA15 | Latched Address (Bits 12–15) |
| 16, 18, 20, 22, 24, 26, 28, 30 | AD7–0 | Data Bus (Bits 7–0) – MCU multiplexed I/O data bus |
| 29 | LR/$\overline{W}$ | Latch Read/Write – Active-high output signal that indicates the direction of data transferred on the bus |
| 32 | $\overline{LIR}$ | Load Instruction Register – Signal that indicates an instruction is starting |
| 34 | LBOX | Last Box – Active-high signal indicating last cycle of current instruction is in process |
| 37 | $V_{CC}$ | +5 Vdc Power – Input voltage used by the EM |
| 38 | T12CLK | System Clock – Clock signal located at the internal bus frequency |
| 39 | $\overline{RESET}$ | Reset – Active-low bidirectional signal |

## Target Cable Connectors – J2 and J3

**Figure 5** shows the pin assignments for connector – J2 and J3. **Table 2** on page 27 lists signal descriptions for connector – J2, and **Table 3** on page 28 lists connector – J3 signals.

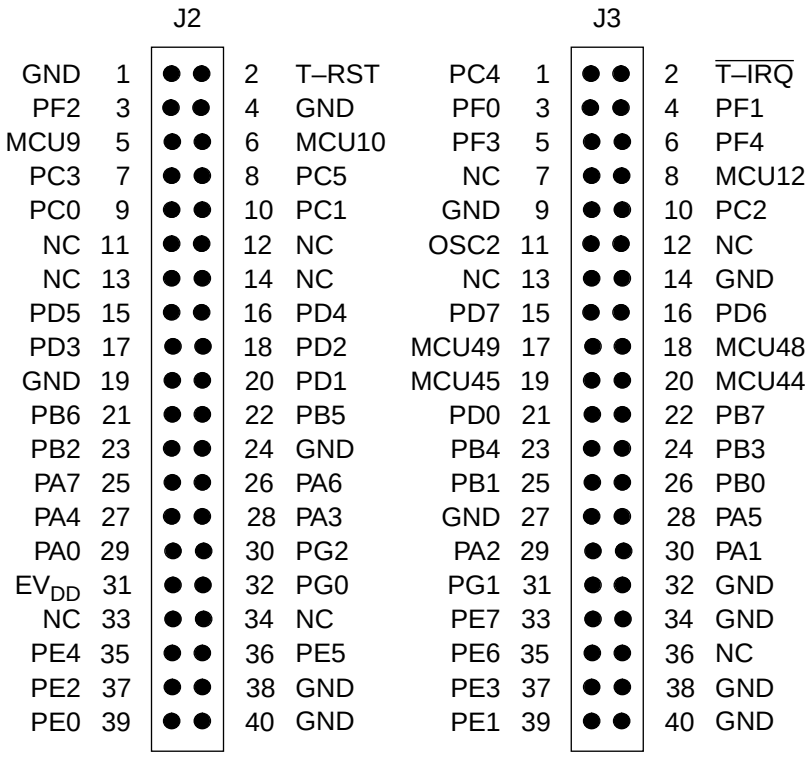


**Figure 5. Target Connector – J2 and J3 Pin Assignment**

## Table 2. Connector – J2 Signal Descriptions

| Pin | Mnemonic | Signal |
|---|---|---|
| 1, 4, 19, 24, 38, 40 | GND | GROUND |
| 11–14, 33, 34 | NC | No Connection |
| 2 | T–RST | Target Reset – Active-low input signal from the target that causes a user reset |
| 3 | PF2 | Port F (Bit 2) – 5-bit special-function port that shares four of its pins with the timer interface module |
| 5 | MCU9 | CL2RxPD if W1 set to 2–3 position and digital BDLC bond out MCU<br>REXT if W1 set to 2–3 postion and analog transceiver bond out MCU |
| 6 | MCU10 | CL2TxPD if W2 set to 2–3 position and digital BDLC bond out MCU<br>BUS if W2 set to 2–3 position and analog transceiver bond out MCU |
| 7–10 | PC3, PC5, PC0, PC1 | Port C (Bits 3, 5, 0, 1) – General-purpose I/O lines controlled by software via data direction and data registers |
| 15–18, 20 | PD5, PD4, PD3, PD2, PD1 | Port D (Bits 5, 4, 3, 2, 1) – Special-function port that shares all its pins with the analog-to-digital converter |
| 21–23 | PB6, PB5, PB2 | Port B (Bits 6, 5, 2) – Special-function port that shares all its pins with the analog-to-digital converter |
| 25 – 29 | PA7, PA6, PA4, PA3,PA0 | Port A (Bits 7, 6, 4, 3, 0) – General-purpose I/O lines controlled by software via data direction and data registers |
| 30, 32 | PG2, PG0 | Port G (Bits 2, 0) – General-purpose I/O lines controlled by software via data direction and data registers |
| 31 | $EV_{DD}$ | Target $V_{DD}$ – Sensed by MMDS circuitry, only as status indicator |
| 35, 37, 37, 39 | PE4, PE5, PE2, PE0 | Port E (Bits 4, 5, 2, 0) – Special-function port that shares two of its pins with the timer interface module, two with SCI and four with SPI |

**Table 3. Connector – J3 Signal Descriptions**

| Pin | Mnemonic | Signal |
|---|---|---|
| 1, 10 | PC4, PC2 | Port C (Bits 4, 2) – General purpose I/O lines controlled by software via data direction and data registers |
| 2 | T–IRQ | Target IRQ – Active low-input signal from the target that causes an interrupt |
| 3–6 | PF0, PF1, PF3, PF4 | Port F (Bit 0, 1, 3, 4) – 5-bit special-function port that shares four of its pins with the timer interface module |
| 7, 12, 13, 36 | NC | No connection |
| 8 | MCU12 | ALOOP if W3 set to 2–3 position and digital BDLC bond out MCU<br>LOAD if W3 set to 2–3 position and analog transceiver bond out MCU |
| 9, 14, 27, 32, 34, 38, 40 | GND | GROUND |
| 11 | OSC2 | Inverted oscillator clock output |
| 15–16, 21 | PD7, PD6, 0 | Port D (Bits 7, 6, 0) – Special-function port that shares all its pins with the analog-to-digital converter |
| 17–20 | MCU49, 48, 45, 44 | Connected to the MCU pins 49, 48, 45, 44 (currently no connects) |
| 22–26 | PB7, PB4, PB3, PB1, PB0 | Port B (Bits 7, 4, 3, 1, 0) – Special-function port that shares all its pins with the analog-to-digital converter |
| 28–30 | PA5, PA2, PA1 | Port A (Bits 5, 2, 1) – General purpose I/O lines controlled by software via data direction and data registers |
| 31 | PG1 | Port G (Bit 1) – General purpose I/O lines controlled by software via data direction and data registers |
| 33, 35, 37, 39 | PE7, PE6, PE3, PE1 | Port E (Bits 7, 6, 3, 1) – Special-function port that shares two of its pins with the timer interface module, two with SCI and four with SPI |

# Schematics

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## M68EM08AX48 Schematics

Refer to the following pages for the six sheets of schematics for the M68EM08AX48 emulation module.

# Schematics

# M68EM08AX48 Schematics (Sheet 1 of 6)

NOTES, UNLESS OTHERWISE SPECIFIED

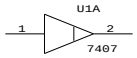
1. VCC PIN LOCATIONS :

   VCC IS APPLIED TO PIN 8 OF ALL 8-PIN IC's, PIN 14 OF ALL 14-PIN IC's, PIN 16 OF ALL 16-PIN IC's, PIN 20 OF ALL 20-PIN IC's, ETC.

2. GROUND PIN LOCATIONS :

   GROUND IS APPLIED TO PIN 4 OF ALL 8-PIN IC's, PIN 7 OF ALL 14-PIN IC's, PIN 8 OF ALL 16-PIN IC's, PIN 10 OF ALL 20-PIN IC's, ETC.

3. DEVICE TYPE, PIN NUMBERS, AND REFERENCE DESIGNATOR OF GATES ARE SHOWN AS FOLLOWS :



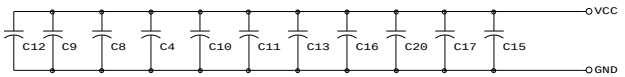

   7407 = DEVICE TYPE
   1 AND 2 = PIN NUMBERS
   U1A = REFERENCE DESIGNATORS

4. RESISTANCE VALUES ARE IN OHMS.
5. RESISTORS ARE 1/4 WATT, 5%.
6. CAPACITANCE VALUES ARE IN MICROFARADS.

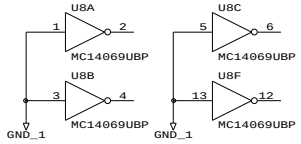
## M68HC08AX48
## CPU BOARD

| REVISIONS | | |
|---|---|---|
| REV | DESCRIPTION | DATE |
| 2 | ADPRU XCLK CHANGED TO OSC1 FROM 1MHZ CAN, XY3 NO LONGER REQUIRED. | 10/16/95 |
| 3 | DELAYED LBOX THRU 2 AC00 GATES (PREVIOUSLY SPARE), NOT ENOUGH HOLD ON LBOX TO T12 FALL, CAUSING TRACE NOT TO WORK | 10/26/95 |

Decouple Caps for ICs as labeled.
All caps are 0.1 uF @ 50 V




## Spare Gates




0RCAD IV FLAT FILES

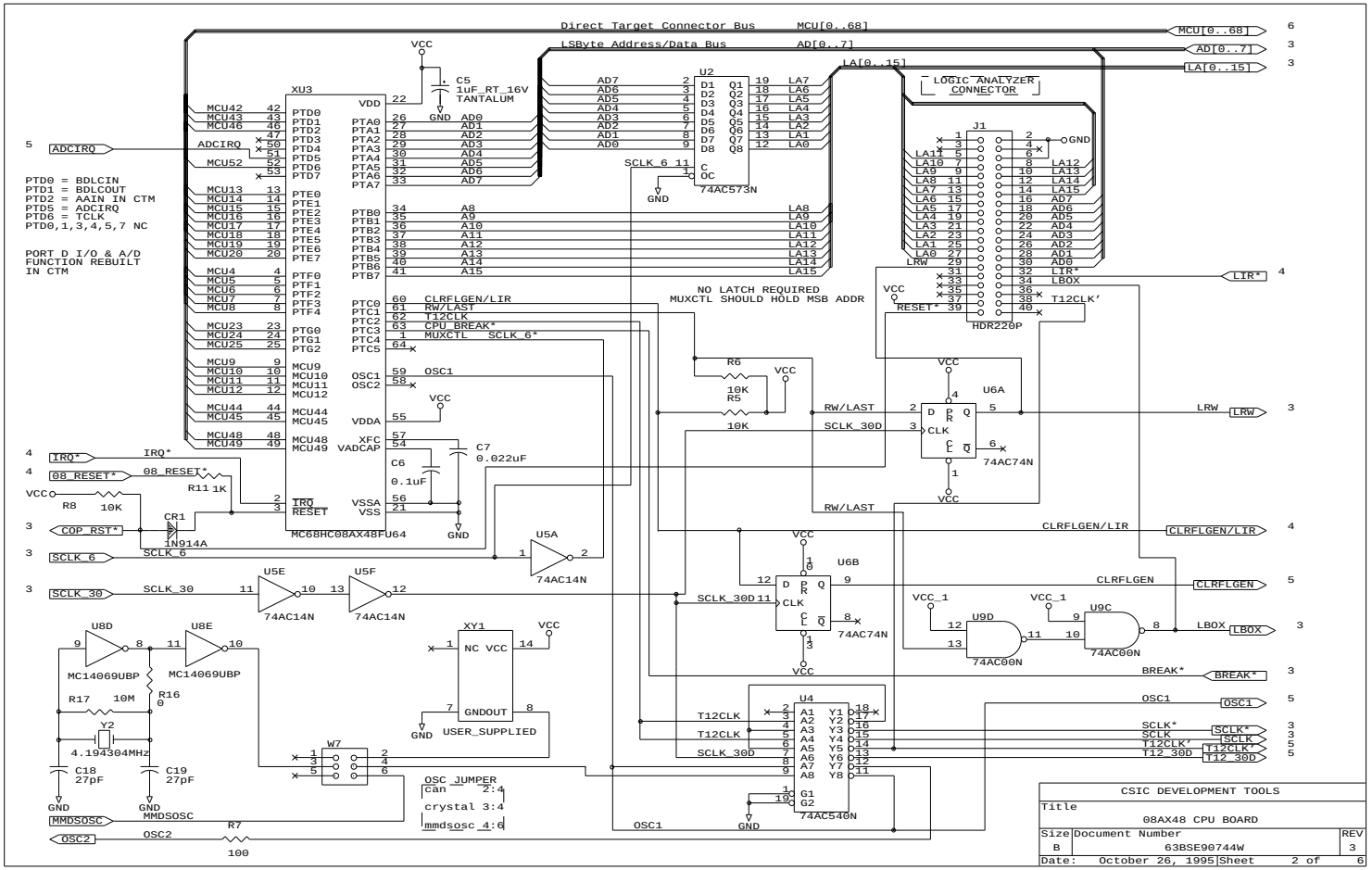
|LINK
|AX48R3S2.SCH
|AX48R3S3.SCH
|AX48R3S4.SCH
|AX48R3S5.SCH
|AX48R3S6.SCH

COMPUTER GENERATED DRAWING : DO NOT REVISE MANUALLY

| CSIC DEVELOPMENT TOOLS | | |
|---|---|---|
| Title: 08AX48 CPU BOARD | | |
| Size: B | Document Number: 63BSE90744W | REV: 3 |
| Date: October 26, 1995 | Sheet 1 of 6 | |

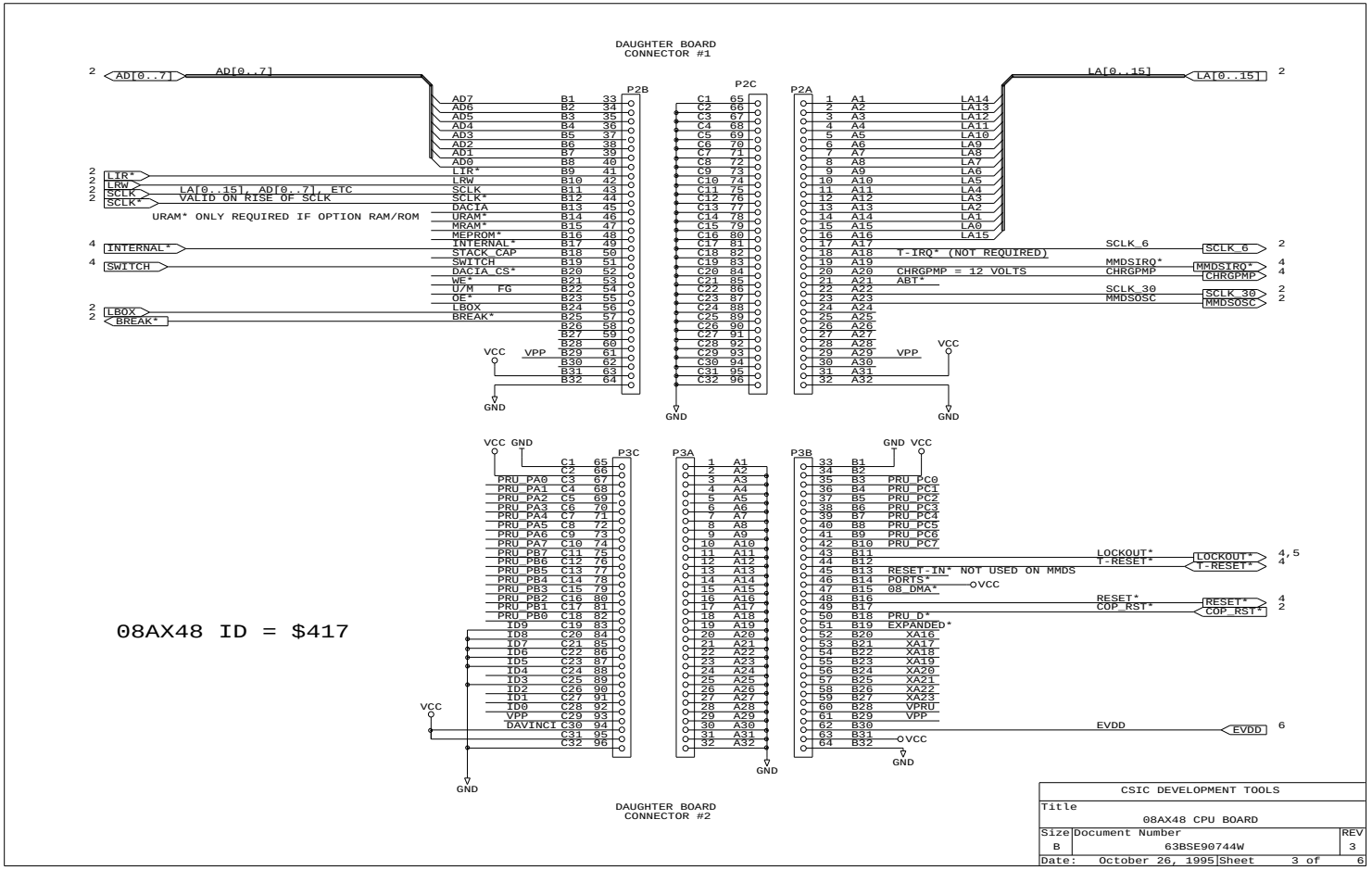
# Schematics

# M68EM08AX48 Schematics (Sheet 2 of 6)



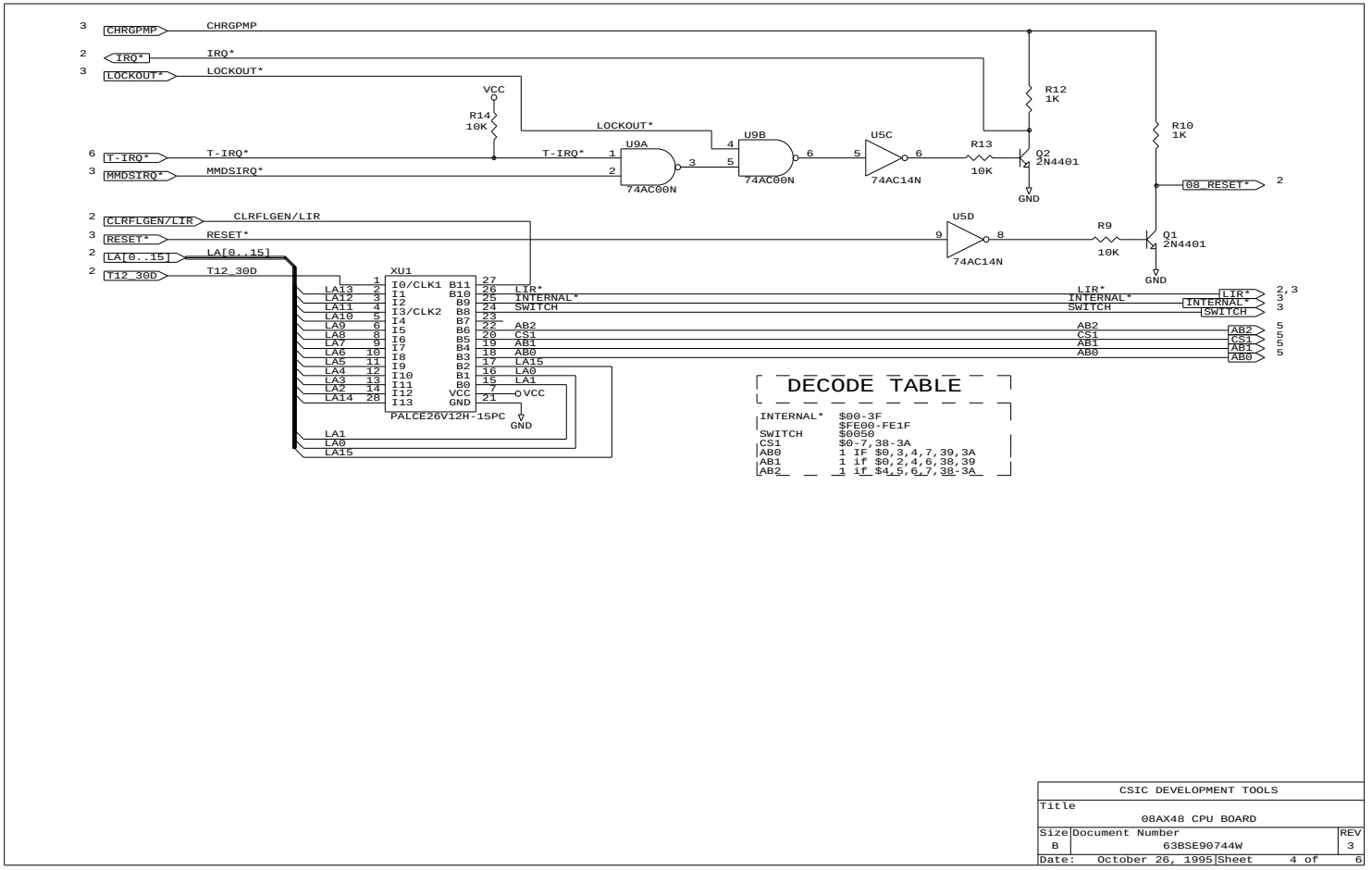
# Schematics

# M68EM08AX48 Schematics (Sheet 3 of 6)



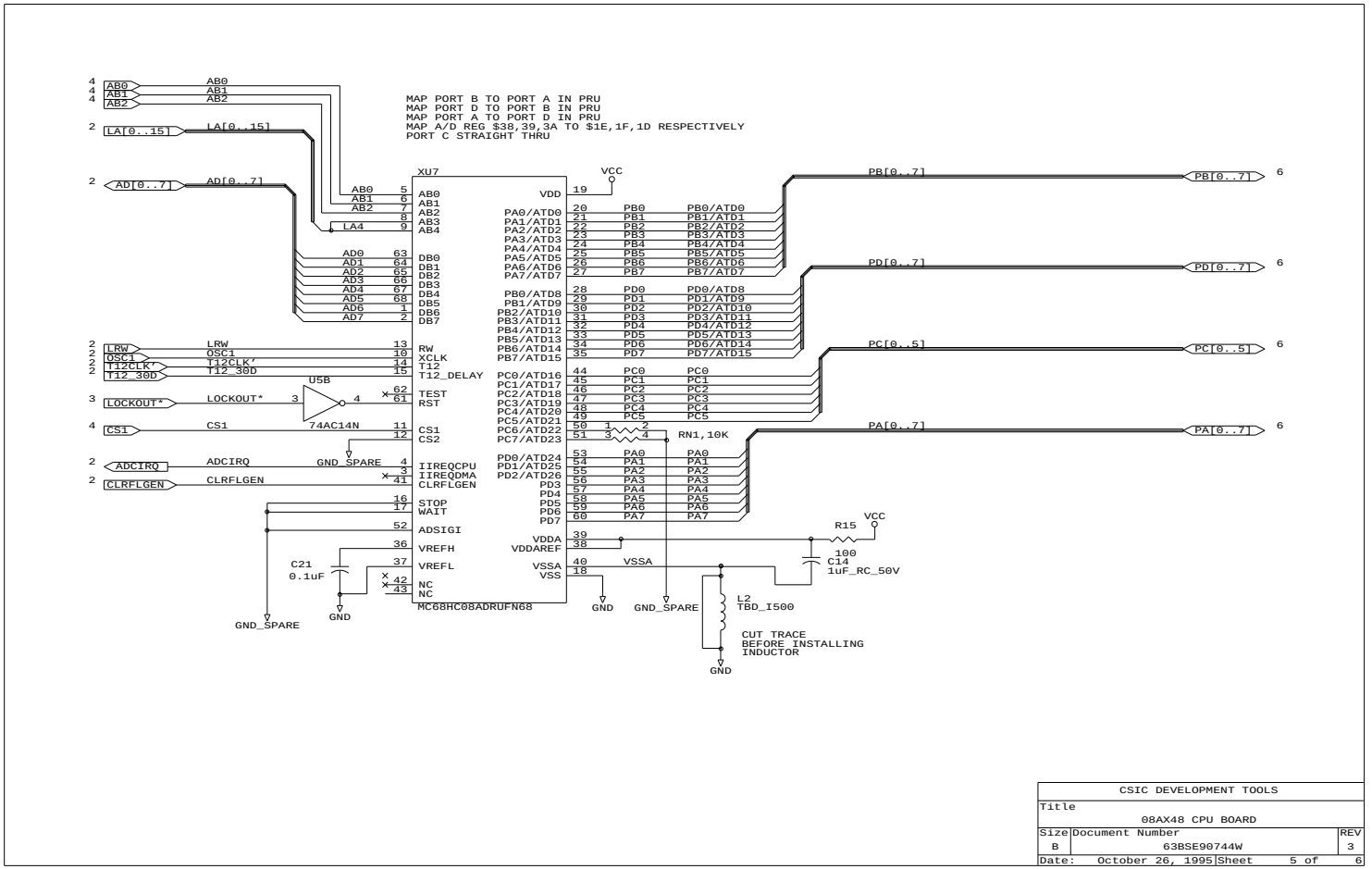
# Schematics

# M68EM08AX48 Schematics (Sheet 4 of 6)



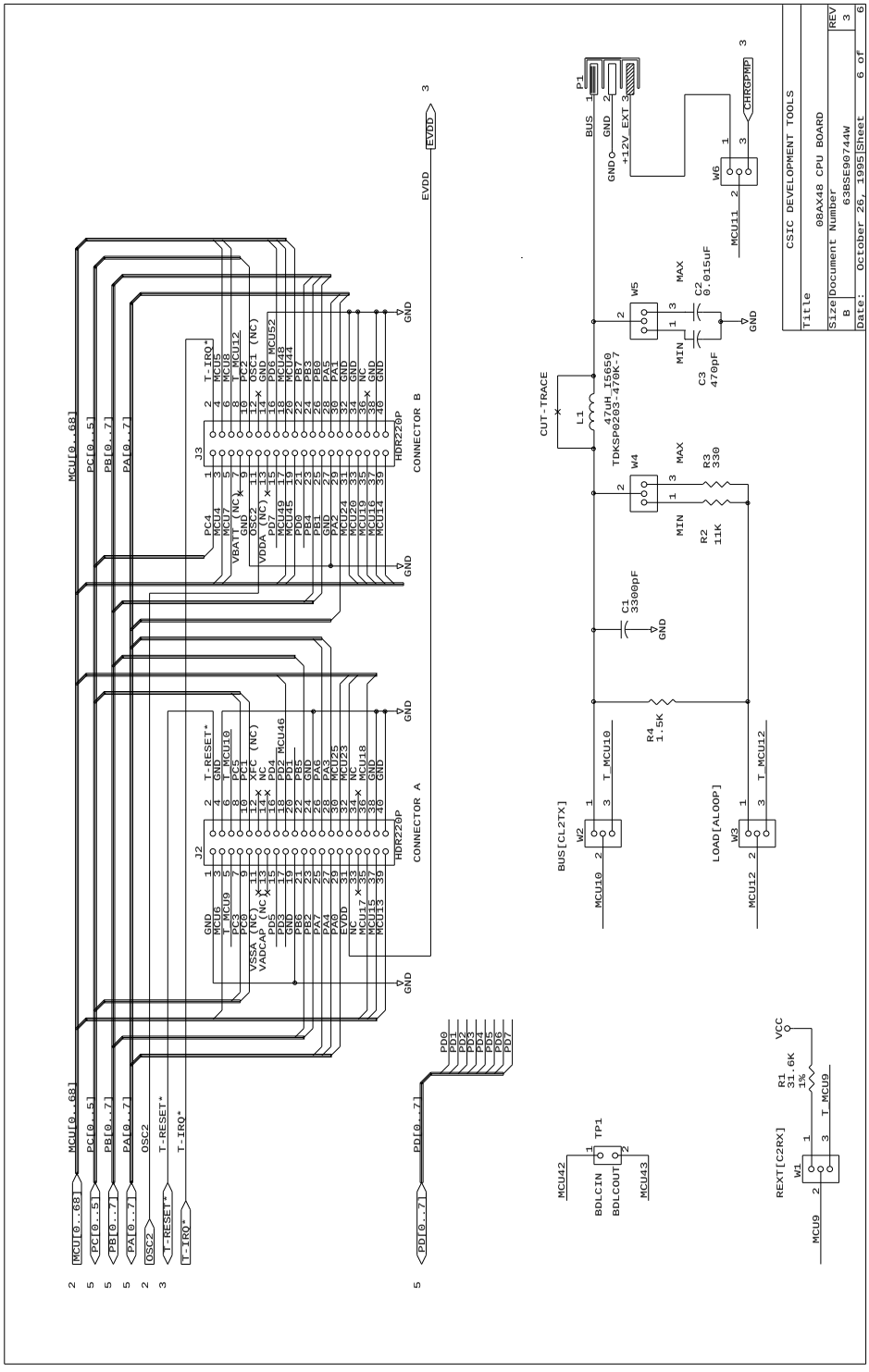
# Schematics

# M68EM08AX48 Schematics (Sheet 5 of 6)



# Schematics

## M68EM08AX48 Schematics (Sheet 6 of 6)



# Schematics

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