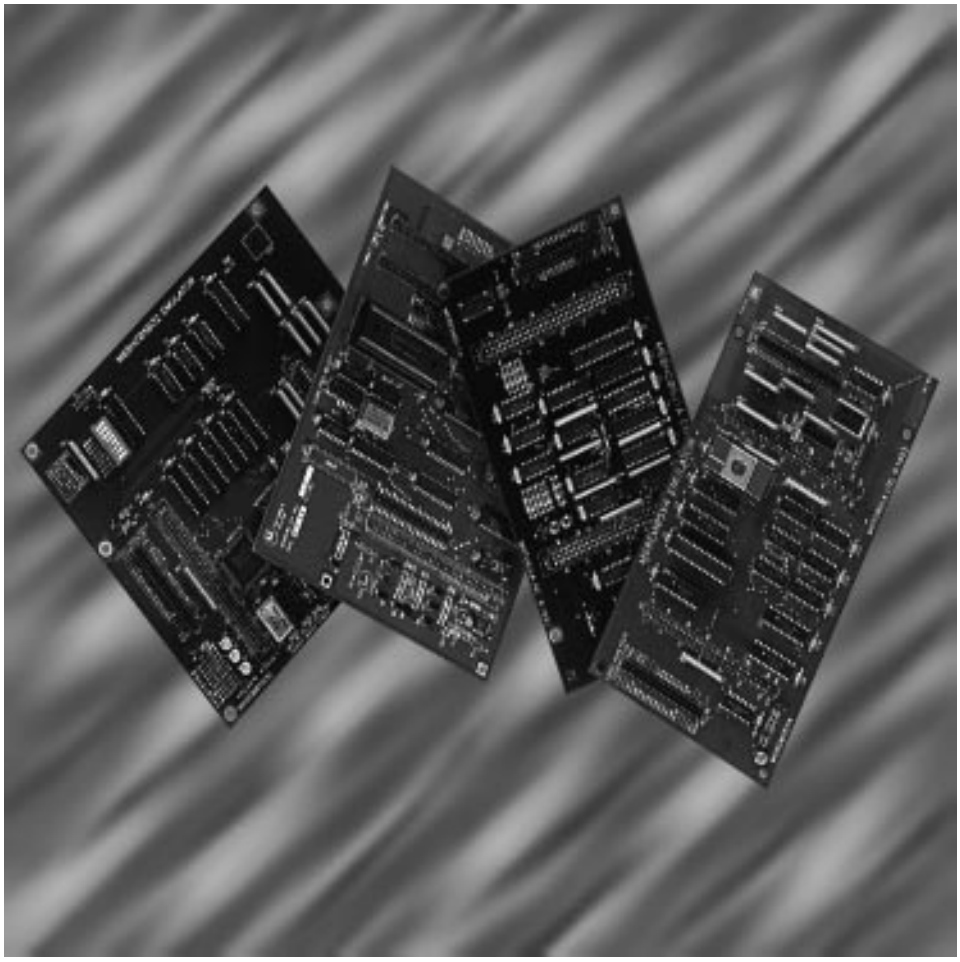
M68EM08MP16UM/D
Rev. 1.0

M68EM08MP16

EMULATION MODULE
USER'S MANUAL



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M68EM08MP16

Emulation Module
User's Manual

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Revision History

This table summarizes differences between this revision and the previous revision of this emulation module user's manual.

Previous Revision	None
Current Revision	Original release
Date	09/96

Revision History

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General Description

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Introduction

The M68EM08MP16 gives your Motorola development tool the ability to emulate target systems based on MC68HC08MP16 microcontroller units (MCUs). The M68EM08MP16 is designed to operate at 5 volts and up to an 8–MHz bus frequency.

By substituting a different emulation module (EM), the Motorola development tool can be enabled to emulate other MCUs. Refer to *Motorola's Development Tool Selector Guide*, order number SG173/D, for a complete list of available EMs.

This hardware user's manual explains connection, configuration, and operation information specific to the M68EM08MP16 emulation module. The module can be installed in two Motorola development systems. To configure your M68EM08MP16 for either an MMDS or an MMEVS, follow the instructions given in **Configuration and Operation** on page 15.

In this manual, MMDS0508 and MMEVS0508 are referred to as MMDS.

Emulation Components

Motorola's complete emulation system consists of the emulation module described in this manual as well as other separately purchased options described in the following paragraphs.

These items are included with the M68EM08MP16 emulation module:

- **An M68EM08MP16 emulation module (EM)** — The printed circuit board that enables system functionality for MC68HC08MP16 MCUs. The female connectors, on the bottom of the module, mate with male connectors on a development system platform board. The EM also has a connector for the target cable assembly.
- **Configuration software** — 3 1/2-inch diskette containing personality files for this module.

Separately purchased Motorola modular development tool options include:

- **An MMEVS0508 platform board (M68MMPFB0508)** — The MMEVS is an economical development tool that provides real-time in-circuit emulation. The unit's integrated design environment includes an editor, an assembler, a user interface, and a source-level debugging program.
- **An MMDS0508 modular development system (M68MMDS0508)** — The MMDS is a high-performance development tool that has all the capabilities of the MMEVS. In addition, it also has a power supply, a bus state analyzer, and real-time memory windows.
- **Flex cable target assembly** — Refer to **Target Cable Assemblies** on page 12 for more information.

User-supplied components include:

- **Host computer** — See the appropriate development tool user's manual for minimum requirements.
- **Power supply** — +5 Vdc is required for the MMDS.

EM Layout

Figure 1 shows the layout of the M68EM08MP16. Connector J1 connects to an optional logic analyzer. Target connectors J2 and J3 are the interface to a target system. See **Connector Information** on page 21 for pinouts and signal descriptions for these connectors.

W1 is used to select the oscillator clock for the MC68HC08 device. W2 selects either V_{CC} or a capacitor connection to the ADPRU chip depending on which mask set ADPRU is used. This header should be set at the factory and not changed. Expansion header connectors P1 and P2 connect the EM and the control board.

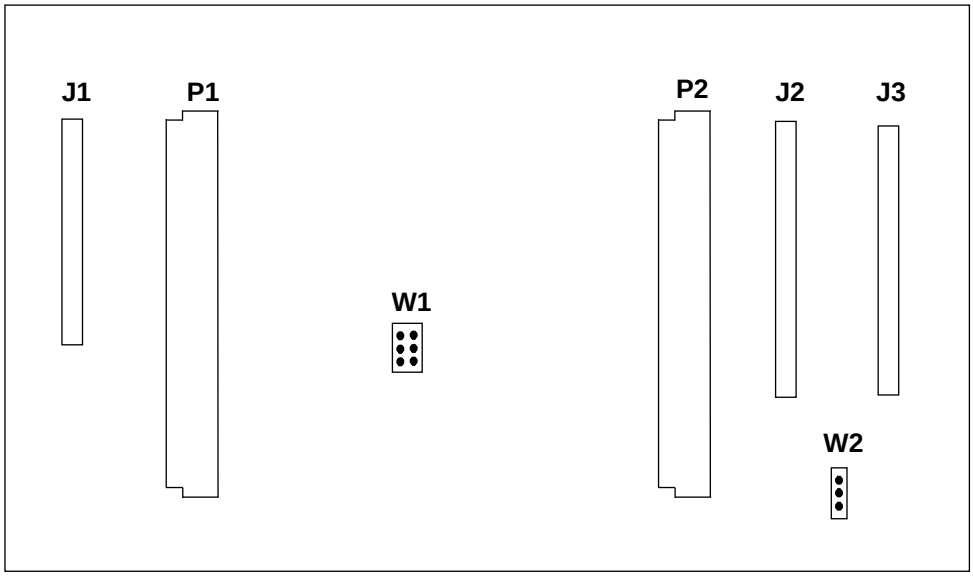


Figure 1. M68EM08MP16 Emulation Module

Target Cable Assemblies

To connect the M68EM08MP16 to a target system, you need a separately purchased target cable assembly. Cable assemblies are available for the 64-pin QFP MCU package.

The target cable connects to the emulator via connector J2 and J3 on the M68EM08MP16 emulation module. Pin assignments and signal descriptions for connectors J2 and J3 can be found in **Target Cable Connectors – J2 and J3** on page 24.

Figure 2 represents a target cable assembly. An assembly for the 64-pin QFP package consists of a flex cable and a QFP target head adapter. One end of the flex cable plugs onto M68EM08MP16 connector J2 and J3 with orientation shown in **Figure 2**. The other end of the flex cable plugs into the target head adapter. Next, the 64-pin QFP target head adapter is inserted into a TQSOCKET and then a TQPACK is installed on the user's target system.

The MCU package in the target system determines the target cable assembly components required.

- For a 64-pin QFP package, use flex cable M68CBL05C and target head adapter M68TC08MP16FU64. A TQSOCKET with guides (M68TQS064SAG1) and a TQPACK (M68TQP064SAM01) are included with the target head adapter.

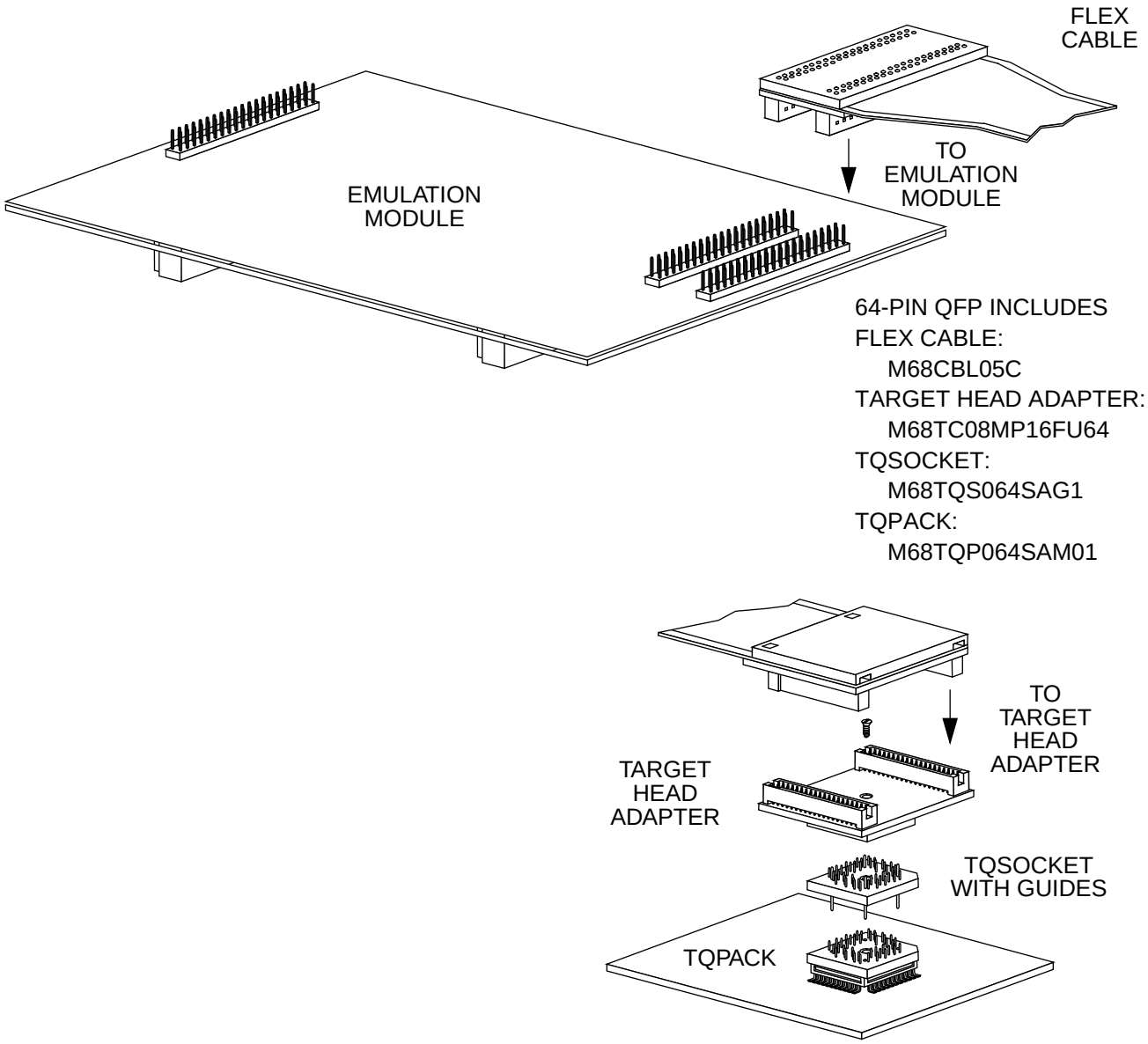


Figure 2. Target Cable Assembly

To configure the M68EM08MP16, follow the instructions of **Configuration and Operation** on page 15. For connector pinouts and signal descriptions, see **Connector Information** on page 21.

Configuration and Operation

Contents

Introduction

The following paragraphs explain how to configure and use your M68EM08MP16 as part of an MMDS or MMEVS system. For other parts of system installation and configuration, see either the *MMDS0508 Operations Manual* (MMDS0508OM/D) or *MMEVS0508 Operations Manual* (MMEVS0508OM/D).

The topics covered in this chapter are:

- **Setting M68EM08MP16 Jumper Headers** on page 16 explains how to set the M68EM08MP16 jumper headers.
- **Personality File Usage** on page 17 discusses the personality file used on the M68EM08MP16 board.
- **MC68HC08MP16 Emulation** on page 18 explains special considerations for emulating with this module.
- **Remaining System Installation** on page 18 covers the final steps to system installation.
- **Troubleshooting** on page 19 explains how to correct operating problems associated with the MC68HC08MP16 MCU .

NOTE: *You can configure an M68EM08MP16 already installed in the system platform board. To do so, remove system power and then follow the guidance of this chapter.*

CAUTION: *Be sure to switch off power before you reconfigure an installed EM. Reconfigure EM jumper headers with the power on can damage emulation circuits.*

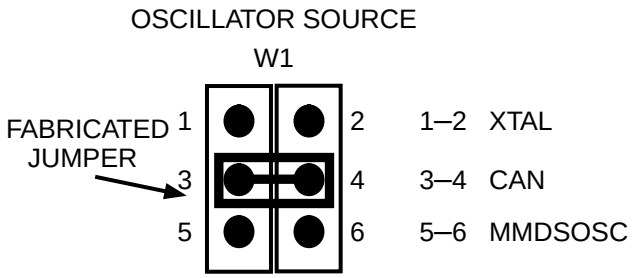
Setting M68EM08MP16 Jumper Headers

The M68EM08MP16 has only one user-selectable jumper header – W1. The following explains how to configure this component.

Clock Source Select Header – W1

Jumper header W1 is used to determine the source of the clock signal. The diagram below shows the factory configuration: the W1 fabricated jumper between pins 3 and 4 selects the CAN oscillator clock source (at board location XY1). This is the default selection.

The other possible clock sources originate from the MMDS control board or a user-supplied crystal oscillator clock source (at board location Y1). For the MMDS frequency, reposition the W1 jumper between pins 5 and 6, then use the MMDS OSC command to select a frequency. For the user-supplied crystal oscillator source, reposition the W1 jumper between pins 1 and 2 and supply the desired crystal oscillator components located at Y1, R12, R13, C12, and C13. The schematics in **Schematics** on page 27 shows the actual circuit connection.



Personality File Usage

The MMDS uses a specific personality file to emulate an MC68HC08MP16 MCU: file 0041AVxx.MEM. This file should be located on a separate disk shipped with the EM08MP16. This file name follows the pattern for all personality files, **00ZZZVxx.MEM**, where **ZZZ** is the EM identifier of the MCU name, and **xx** is the version of the file.

The purpose of memory definitions illustrates how the MMDS handles writes to the two types of memories. During user code execution, attempts to write to a location mapped as ROM will generate a write protect error, and user code execution is halted. Code should never write to a ROM location. However, a write to a location mapped as RAM does not stop code execution.

With an understanding of MMDS handling of memory mapping, the user can customize the MMDS to emulate within the needs of the application. The memory settings can be altered using the MMDS SETMEM command.

MC68HC08MP16 Emulation

Differences

The performance of an MC68HC08MP16 MCU run in single-chip operation has no known differences between it and the way certain features perform during emulation.

Remaining System Installation

When header W1 has been configured, M68EM08MP16 configuration is complete.

- Ensure that the power to the development tool is off.
- If installing the M68EM08MP16 in an MMDS station module, remove the panel from the station module top.
- Fit together EM connectors P1 and P2 (on the bottom of the board) and platform board DIN connectors. Snap the corners of the EM onto the plastic standoffs.
- Connect the target cable, if appropriate.
- If installing in an MMDS05, replace the panel.

At this point, you are ready to make remaining cable connections, as necessary, and restore power.

For instructions, consult either the *MMEVS05/MMEVS08 Operations Manual* (MMEVS0508OM/D) or the *MMDS0508 Operations Manual* (MMDS0508OM/D).

Troubleshooting

If the emulator board fails to communicate with the host computer, these tests may help isolate the cause:

- Check the RS232 connections, if the correct COM port is identified on command line, and if power is on. Refer to the operations manual for more information.
- Check for an oscillator at header W1 pin 2. Refer to **Clock Source Select Header – W1** on page 17.
- Check for T12 on the logic analyzer connector. If this is not present, the part may be in stop, wait, single-chip, or reset mode.

Connector Information

Contents

Introduction

This chapter gives pinouts and signal descriptions for MC68HC08MP16 connectors – J1, J2, and J3.

Logic Analyzer Connector – J1

Figure 3 shows the pin assignments for logic analyzer connector – J1. This connector provides easy access to many of the signals used internally to the emulator. **Table 1** on page 23 lists signal descriptions for this connector.

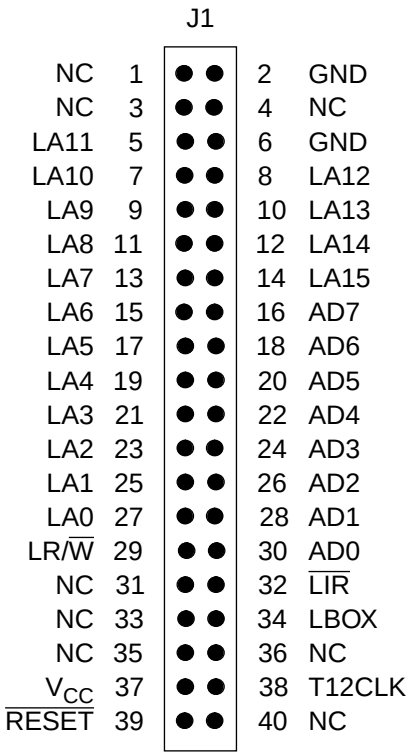


Figure 3. Connector – J1 Pin Assignments

Table 1. Connector – J1 Signal Descriptions

Pin	Mnemonic	Signal
1, 3, 4, 31, 33, 35, 36, 40	NC	No Connection
2, 6	GND	GROUND
5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27	LA11–LA0	Latched Address (Bits 11-0)
8, 10, 12, 14	LA12–LA15	Latched Address (Bits 12-15)
16, 18, 20, 22, 24, 26, 28, 30	AD7–AD0	Data Bus (Bits 7-0) – MCU multiplexed I/O data bus
29	LR/$\overline{W}$	Latch Read/Write – Signal that indicates the direction of data transferred on the bus
32	$\overline{LIR}$	Load Instruction Register – Active-low output signal that indicates an instruction is starting
34	LBOX	Last Box – Active-high signal indicating last cycle of current instruction is in process
37	V_{CC}	+5 Vdc Power – Input voltage used by the EM
38	T12CLK	System Clock – The clock signal is the same as the internal bus frequency.
39	$\overline{RESET}$	Reset – Active-low bidirectional signal

Target Cable Connectors – J2 and J3

Figure 4 shows the pin assignments for connectors – J2 and J3. **Table 2** on page 25 lists signal descriptions for connector – J2. **Table 3** on page 26 lists connector J3 signals.

J2					J3				
GND	1	2	PB4		PB2	1	2	PB3	
PB7	3	4	GND		PB5	3	4	PB6	
NC	5	6	NC		PC0	5	6	PC1	
PB0	7	8	PB1		NC	7	8	NC	
PA5	9	10	PA6		GND	9	10	PA7	
PA1	11	12	PA2		PA3	11	12	PA4	
NC	13	14	NC		PA0	13	14	GND	
NC	15	16	NC		OSC2	15	16	NC	
PF5	17	18	PF4		$\overline{\text{T–RST}}$	17	18	$\overline{\text{T–IRQ}}$	
GND	19	20	PF1		PF3	19	20	PF2	
EV_{DD}	21	22	PE7		PF0	21	22	GND	
PE4	23	24	GND		PE6	23	24	PE5	
PE1	25	26	PE0		PE3	25	26	PE2	
PWM5	27	28	NC		GND	27	28	PWM6	
PWM2	29	30	PWM1		PWM4	29	30	PWM3	
PD4	31	32	PD5		PD6	31	32	GND	
NC	33	34	NC		PD2	33	34	GND (PD3)*	
PC6	35	36	PD0		PD1	35	36	NC	
PC4	37	38	GND		PC5	37	38	GND	
PC2	39	40	GND		PC3	39	40	GND	

* J3 PIN 34 SILKSCREEN IS INCORRECT. PIN 34 SHOWS GND BUT IS ACTUALLY PD3.

Figure 4. Target Connector Pin Assignments

Table 2. Connector – J2 Signal Descriptions

Pin	Mnemonic	Signal
1, 4, 19, 24, 38, 40	GND	GROUND
5, 6, 13–16, 28, 33, 34	NC	No Connection
2, 3, 7, 8	PB4, PB7, PB0, PB1	Port B (Bits 4, 7, 0, 1) – Special-function port that shares all its pins with the analog-to-digital converter
9–12	PA5, PA6, PA1, PA2	Port A (Bits 5, 6, 1, 2) – General-purpose I/O lines, controlled by software via data direction and data registers
17, 18, 20	PF5, PF4, PF1	Port F (Bits 5, 4, 1) – 6-bit special function port that shares two of its pins with the SCI and four pins with SPI
21	EV_{DD}	Target V_{DD} – Sensed by MMDS circuitry, only as status indicator
22, 23, 25, 26	PE7, PE4, PE1, PE0	Port E (Bits 7, 4, 1, 0) – Special-function port that shares its pins with two timer interface modules
27, 29, 30	PWM5, PWM2, PWM1	PWM6–PWM1 – Dedicated pins used for the outputs of the PWM module
31, 32, 36	PD4, PD5, PD0	Port D (Bits 4, 5, 0) – Special-function input-only port that shares its pins with the current sensing and fault pins for the PWM module
35, 37, 39	PC6, PC4, PC2	Port C (Bits 6, 4, 2) – General-purpose I/O lines, controlled by software via data direction and data registers, that shares two of its pins with the analog-to-digital converter

Table 3. Connector – J3 Signal Descriptions

Pin	Mnemonic	Signal
1–4	PB2, PB3, PB5, PB6	Port B (Bits 2, 3, 5, 6) – Special-function port that shares all of its pins with the analog-to-digital converter
5, 6	PC0, PC1	Port C (Bits 0, 1) – General-purpose I/O lines, controlled by software via data direction and data registers, that shares two of its pins with the analog-to-digital converter
7, 8, 16, 36	NC	No Connection
9, 14, 22, 27, 32, 34(1), 38, 40	GND	GROUND
10, 11, 12, 13	PA7, PA3, PA4, PA0	Port A (Bits 7, 3, 4, 0) – General-purpose I/O lines controlled by software via data direction and data registers
15	OSC2	Inverted Oscillator Clock Output
17	$\overline{\text{T–RST}}$	Target Reset – Active-low input signal from the target that causes a user reset
18	$\overline{\text{T–IRQ}}$	Target IRQ – Active-low input signal from the target that causes an interrupt
19–21	PF3, PF2, PF0	Port F (Bits 3, 2, 0) – 6-bit special-function port that shares two of its pins with the SCI and four pins with SPI
23–26	PE6, PE5, PE3, PE2	Port E (Bits 6, 5, 3, 2) – Special-function port that shares its pins with two timer interface modules
28–30	PWM6, PWM4, PWM3	PWM6–1 – Dedicated pins used for the outputs of the PWM module
31, 33, 35	PD6, PD2, PD1	Port D (Bits 6, 2, 1) – Special-function input-only port that shares its pins with the current sensing and fault pins for the PWM module
37, 39	PC5, PC3	Port C (Bits 5, 3) – General-purpose I/O lines, controlled by software via data direction and data registers, that shares two of its pins with the analog-to-digital converter

1. J3 pin 34 silkscreen is incorrect. Pin 34 shows GND but is actually PD3.

Schematics

Contents

M68EM08MP16 Schematics

Refer to the following pages for the six sheets of schematics for the M68EM08MP16 emulation module.

Schematics

M68EM08MP16 Schematics (Sheet 1 of 6)

NOTES, UNLESS OTHERWISE SPECIFIED

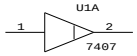
1. VCC PIN LOCATIONS :

   VCC IS APPLIED TO PIN 8 OF ALL 8-PIN IC's, PIN 14 OF ALL 14-PIN IC's, PIN 16 OF ALL 16-PIN IC's, PIN 20 OF ALL 20-PIN IC's, ETC.

2. GROUND PIN LOCATIONS :

   GROUND IS APPLIED TO PIN 4 OF ALL 8-PIN IC's, PIN 7 OF ALL 14-PIN IC's, PIN 8 OF ALL 16-PIN IC's, PIN 10 OF ALL 20-PIN IC's, ETC.

3. DEVICE TYPE, PIN NUMBERS, AND REFERENCE DESIGNATOR OF GATES ARE SHOWN AS FOLLOWS :



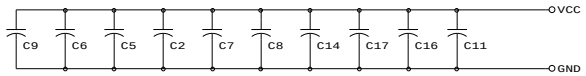
7407 = DEVICE TYPE
1 AND 2 = PIN NUMBERS
U1A = REFERENCE DESIGNATORS

4. RESISTANCE VALUES ARE IN OHMS.
5. RESISTORS ARE 1/4 WATT, 5%.
6. CAPACITANCE VALUES ARE IN MICROFARADS.

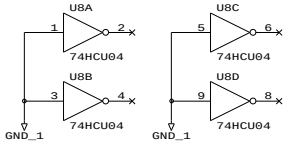
M68HC08MP16 CPU BOARD

REVISIONS		
REV	DESCRIPTION	DATE

Decouple Caps for ICs as labeled.
All caps are 0.1 uF @ 50 V



Spare Gates



0RCAD IV FLAT FILES

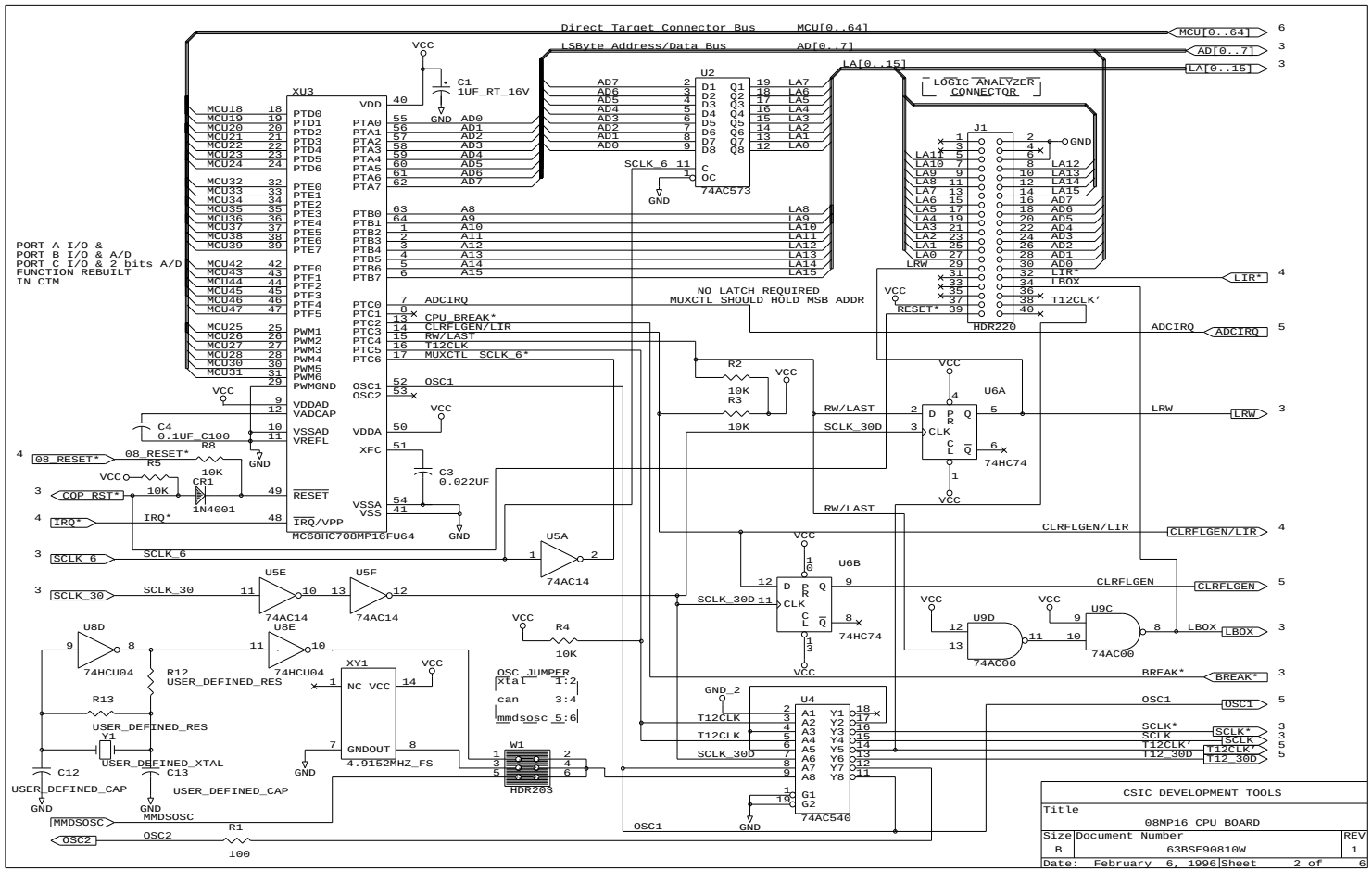
|LINK
|MP16R1S2.SCH
|MP16R1S3.SCH
|MP16R1S4.SCH
|MP16R1S5.SCH
|MP16R1S6.SCH

COMPUTER GENERATED DRAWING : DO NOT REVISE MANUALLY

CSIC DEVELOPMENT TOOLS		
Title	08MP16 CPU BOARD	
Size B	Document Number 63BSE90810W	REV 1
Date: February 6, 1996	Sheet 1 of 6	

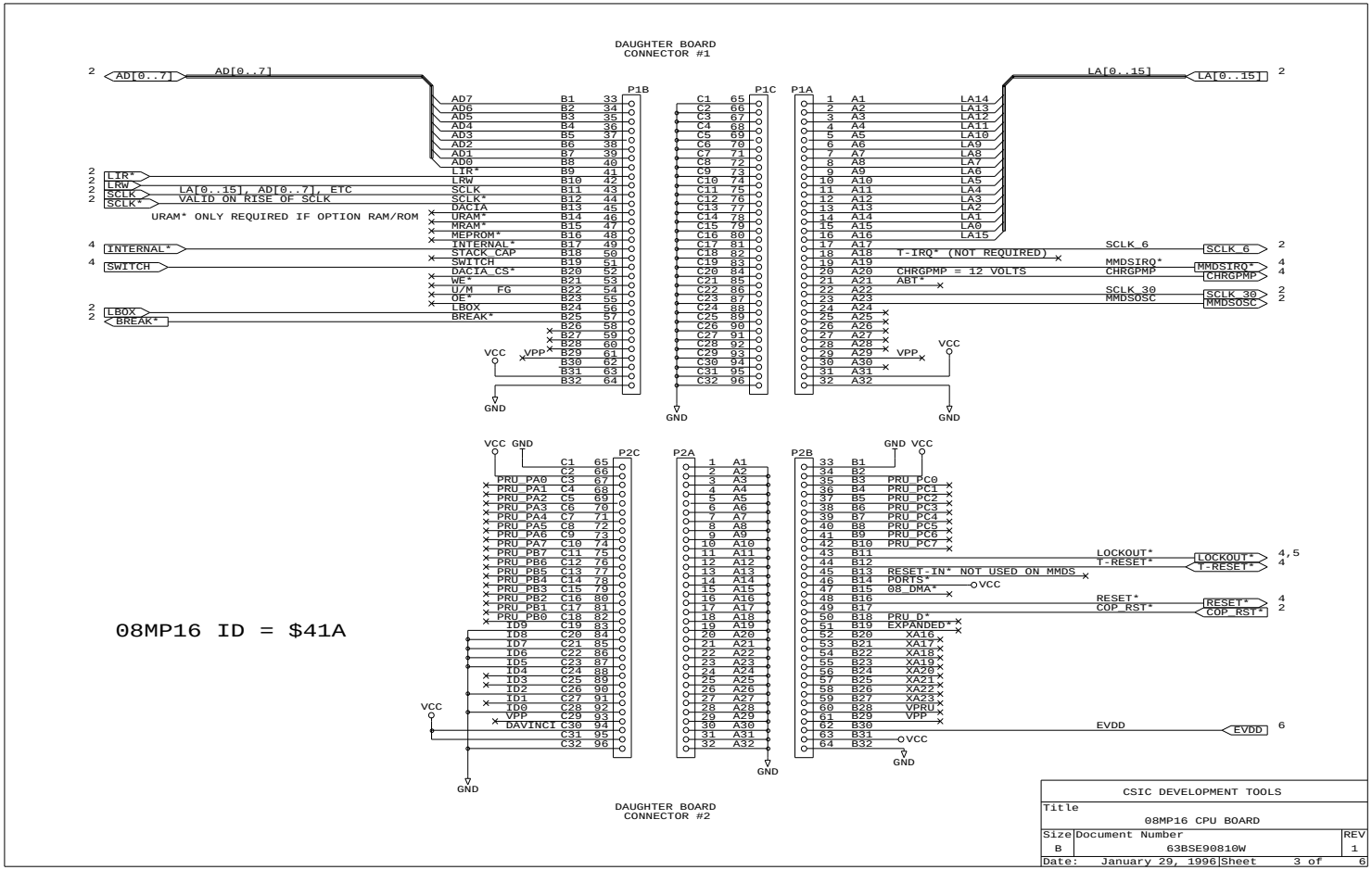
Schematics

M68EM08MP16 Schematics (Sheet 2 of 6)



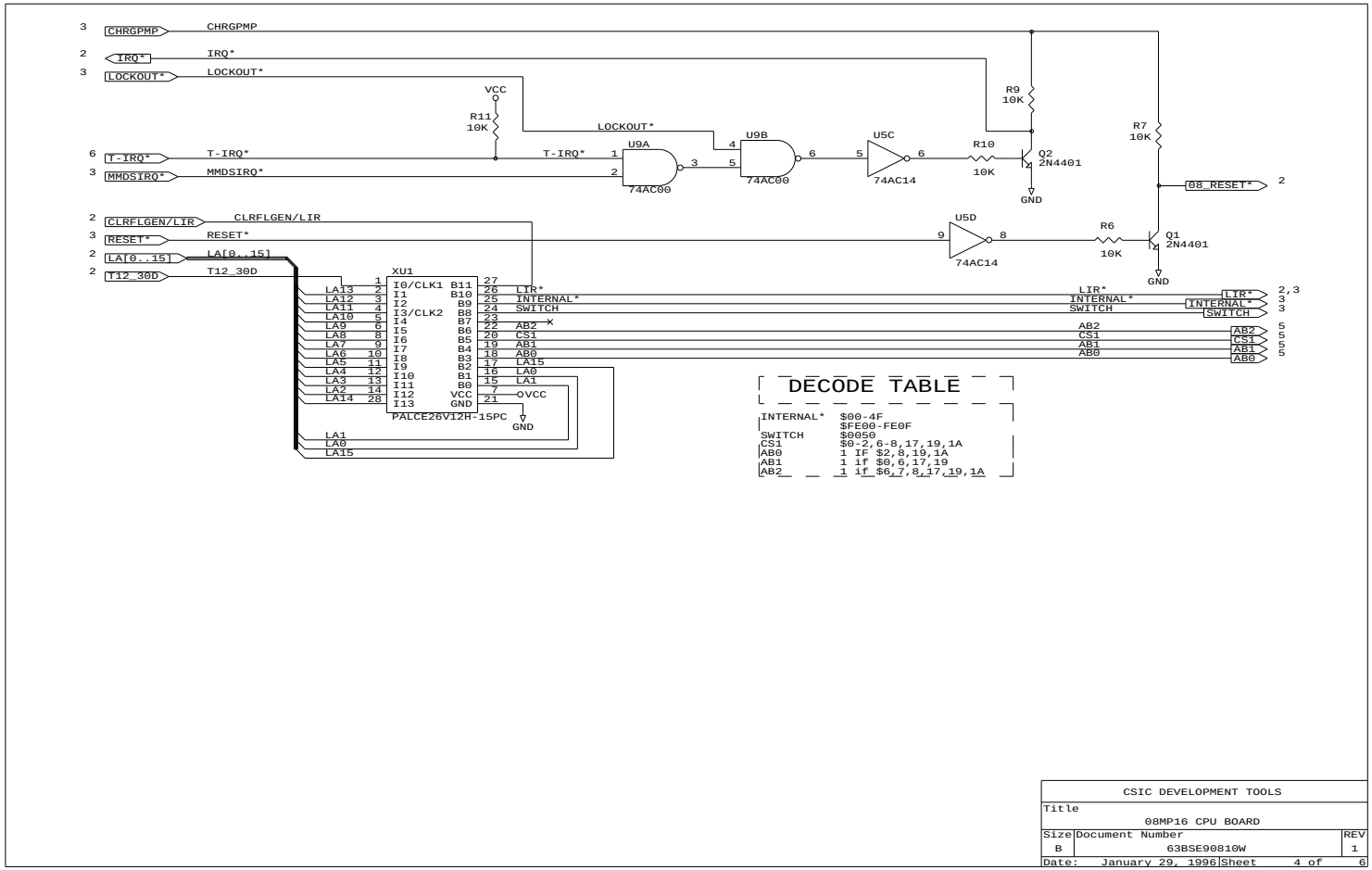
Schematics

M68EM08MP16 Schematics (Sheet 3 of 6)



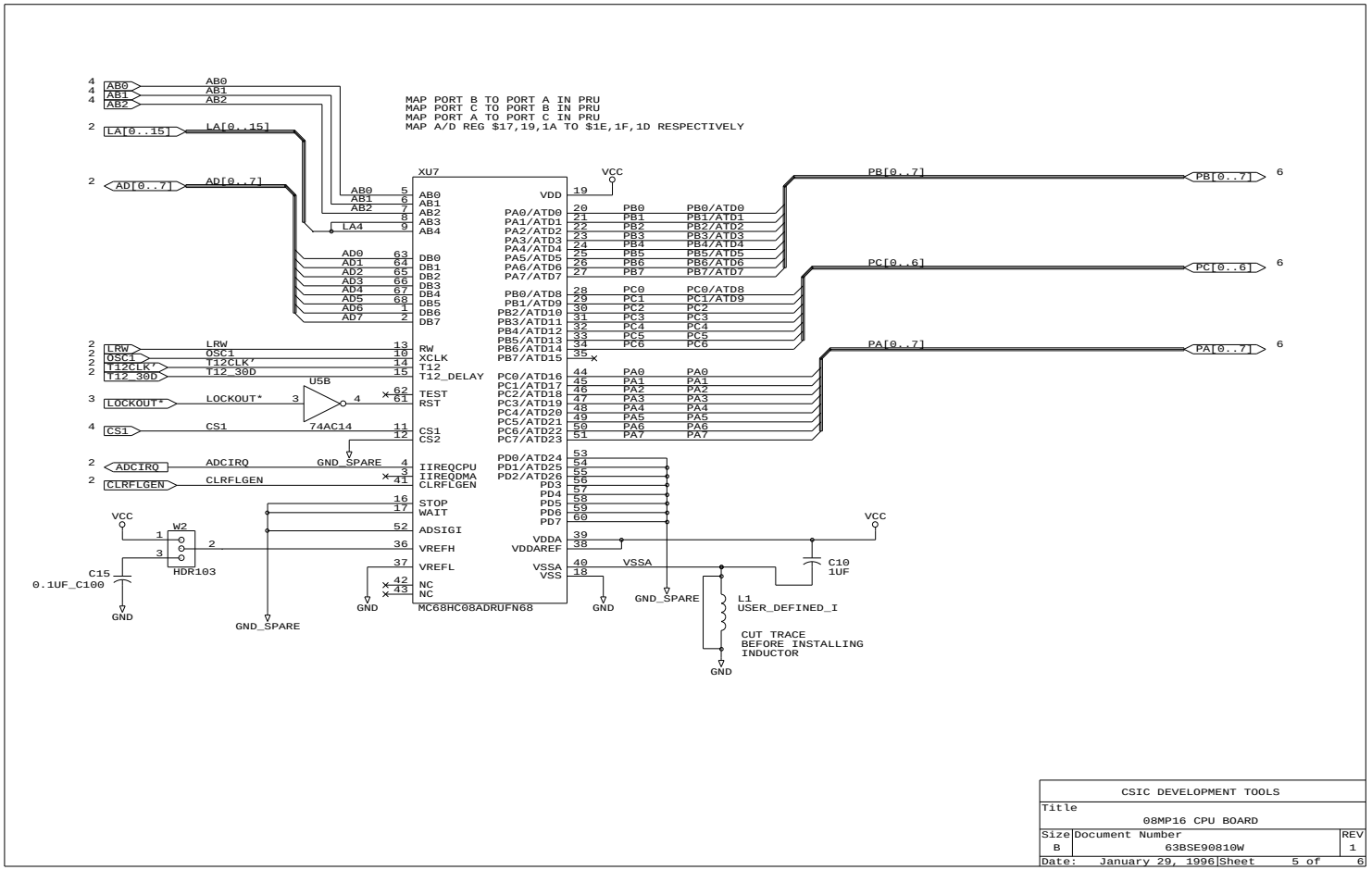
Schematics

M68EM08MP16 Schematics (Sheet 4 of 6)



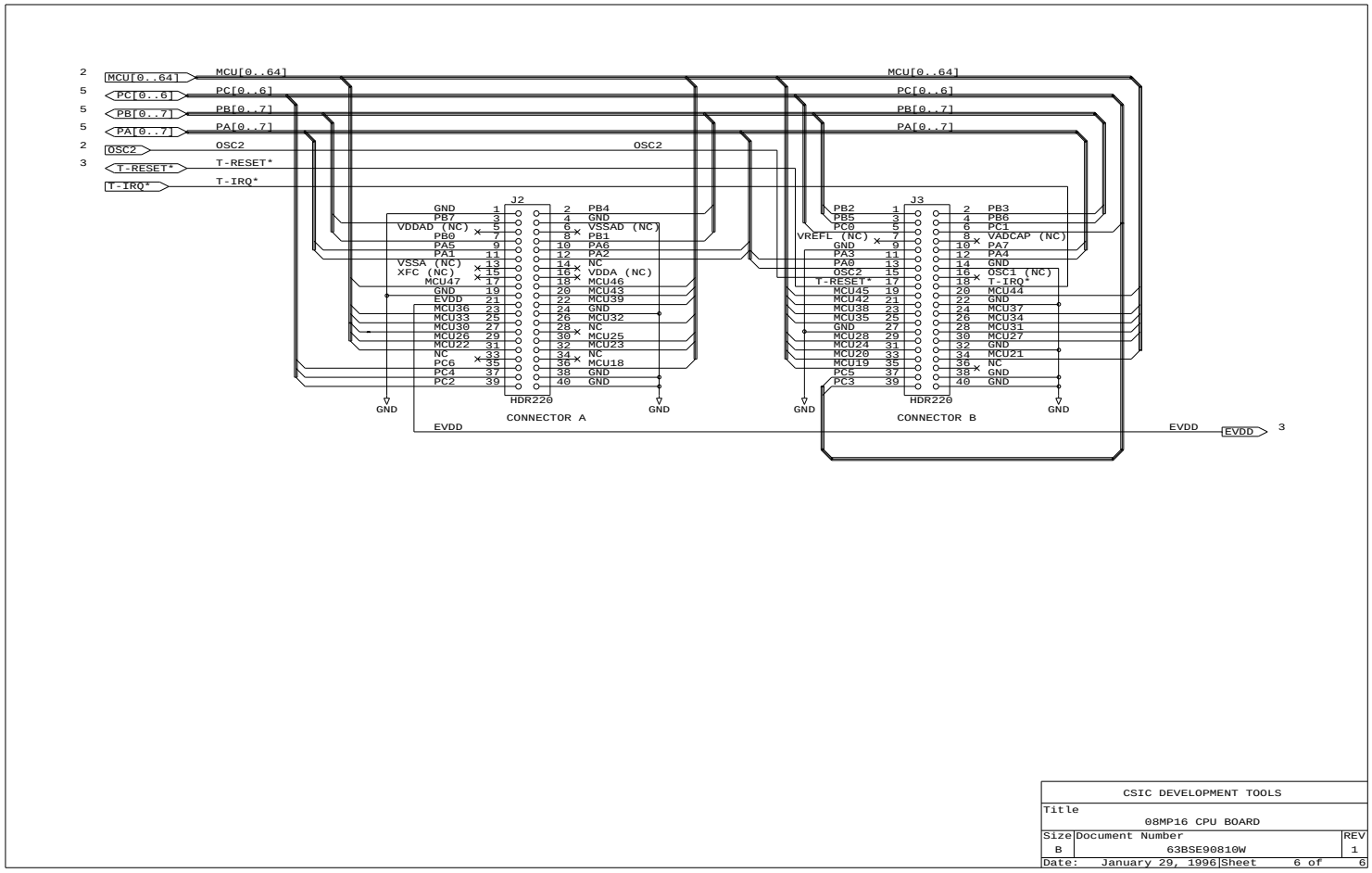
Schematics

M68EM08MP16 Schematics (Sheet 5 of 6)



Schematics

M68EM08MP16 Schematics (Sheet 6 of 6)



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Title: 08MP16 CPU BOARD		
Size: B	Document Number: 63BSE90810W	REV: 1
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Schematics

Note Page

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