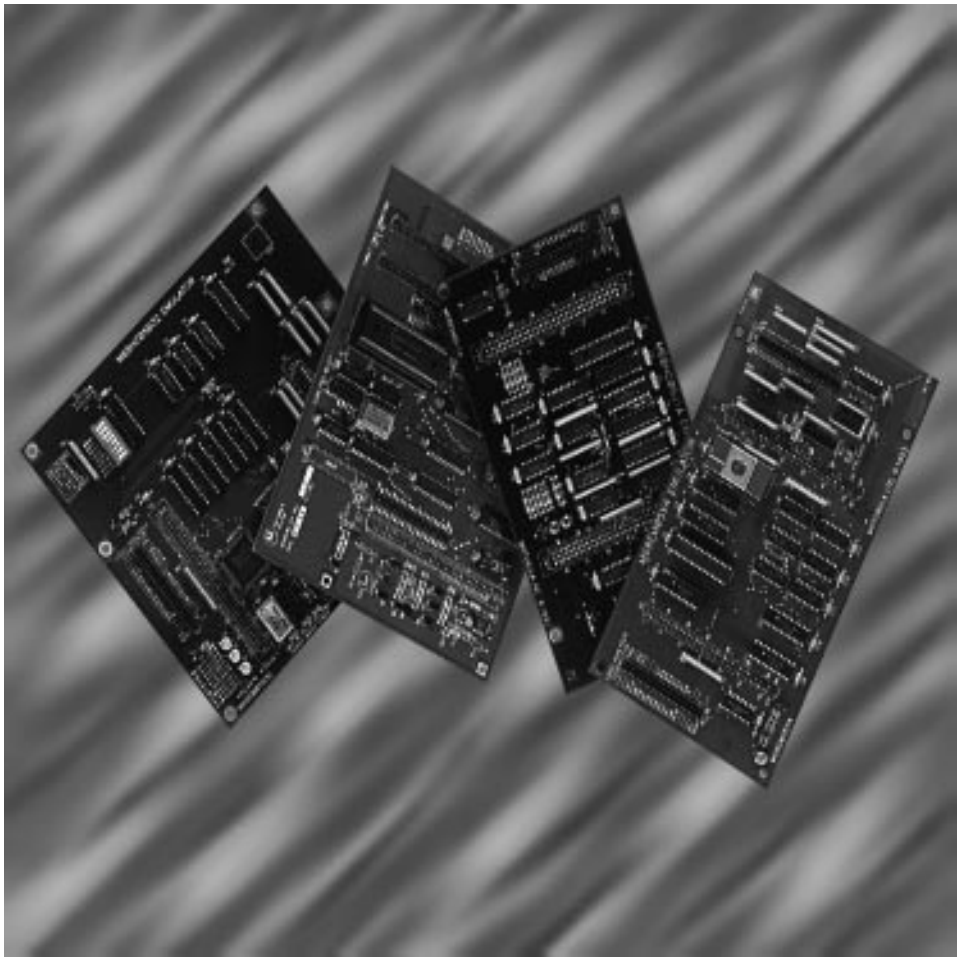
M68EML05P6AUM/D
Rev. 1.0

M68EML05P6A

EMULATION MODULE
USER'S MANUAL



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Emulation Module
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Revision History

This table summarizes differences between this revision and the previous revision of this emulation module user's manual.

Previous Revision	None
Current Revision	1.0
Date	10/96
Changes	Redesign EM to support low-voltage emulation. Update manual to reflect these changes.
Location	Throughout

Revision History

Table of Contents

General Description

Contents

Introduction

The M68EML05P6A gives your Motorola development tool the ability to emulate target systems based on MC68HC705P6A, MC68HC05P1A, MC68HC05P4A, and MC68HC05P9A microcontroller units (MCUs). The M68EML05P6A is designed to be a low-voltage emulator, operating in the 3.0 Vdc to 5.0 Vdc range at maximum rated frequencies per the general release specification.

By substituting a different emulation module (EM), the Motorola development tool can be enabled to emulate other MCUs. Refer to *Motorola's Development Tool Selector Guide*, order number SG173/D, for a complete list of available EMs.

This hardware user's manual explains connection, configuration, and operation information specific to the M68EML05P6A emulation module. The module can be installed in two Motorola development systems. To configure your M68EML05P6A for either an MMDS or an MMEVS, follow the instructions given in **MMDS/MMEVS Configuration and Operation** on page 19.

Emulation Components

Motorola’s complete emulation system consists of the emulation module described in this manual as well as other separately purchased options described in the following paragraphs.

The following items are included with the M68EML05P6A emulation module:

- **An M68EML05P6A emulation module (EM)** — The printed circuit board that enables system functionality for MC68HC(7)05PxA MCUs. The female connectors, on the bottom of the module, mate with male connectors on a development system platform board. The EM also has connectors for the target cable assembly.
- **Configuration software** — 3 1/2-inch diskette containing personality files for this module.

Separately purchased Motorola modular development tool options include:

- **An MMEVS platform board (M68MMPFB0508)** — The MMEVS is an economical development tool that provides real-time in-circuit emulation. The unit's integrated design environment includes an editor, an assembler, a user interface, and a source-level debugging program.

- **An MMDS0508 modular development system (M68MMDS0508)** — The MMDS is a high-performance development tool that has all the capabilities of the MMEVS. In addition, it also has a bus state analyzer and real-time memory windows.
- **Flex cable target assembly** — See **Target Cable Assemblies** on page 12 for more information.

User supplied components include:

- **Host computer** — See the appropriate development tool user's manual for minimum requirements.
- **Power supply** — +5 Vdc is required for the MMEVS.

Emulation Module Layout

Figure 1 shows the layout of the M68EML05P6A. Jumper header W1 controls the voltage reference input for the A/D subsystem. Jumper header W2 selects the MCU clock source. Jumper headers W3 and W4 are part of the $\overline{\text{IRQ}}$ pin voltage control circuit.

Connector J1 is used as a connection to a logic analyzer. DIN connectors P1 and P2 connect the emulation module (EM) and a development system platform board.

Target connector J2 is the interface to a target system and uses a separately purchased target cable assembly. When the M68EML05P6A is installed on the MMDS, the target cable passes through the slit in the station module enclosure.

The resident MC68HC705P6A MCU is at location U4. Switch SW2 enables or disables port A mask options. Switch SW1 controls which MCU is being emulated.

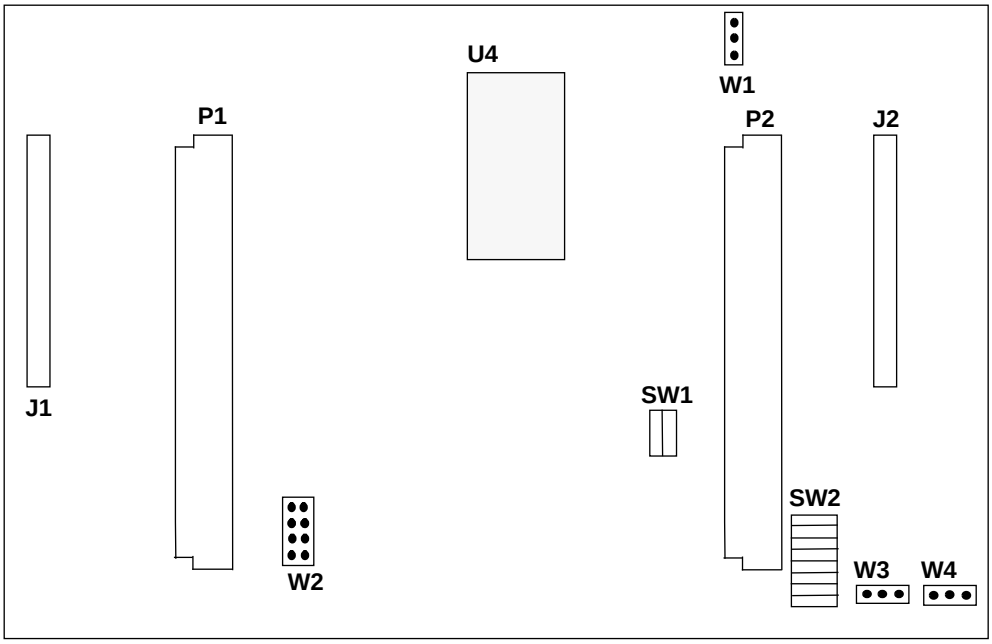


Figure 1. M68EML05P6A Emulation Module

Target Cable Assemblies

To connect your M68EML05P6A to a target system, you need a separately purchased target cable assembly. Cable assemblies are available for two MCU packages: dual in-line plastic (DIP) package and small outline integrated circuit (SOIC) package.

The target cable connects to the emulator via connector J2 on the M68EML05P6A emulation module. Pin assignments and signal descriptions for connector J2 can be found in **Target Cable Connector Pin Assignments** on page 14.

Figure 2 represents a target cable assembly. An assembly for 28-pin DIP packages consists of a flex cable and a target head adapter. The assembly for 28-pin SOIC packages requires an additional SOIC adapter. One end of the flex cable plugs onto M68EML05P6A connector J2 with orientation shown in **Figure 2**. The other end of the flex cable plugs into the target head adapter. The target head adapter then inserts into either a DIP footprint in a target system or into the SOIC adapter.

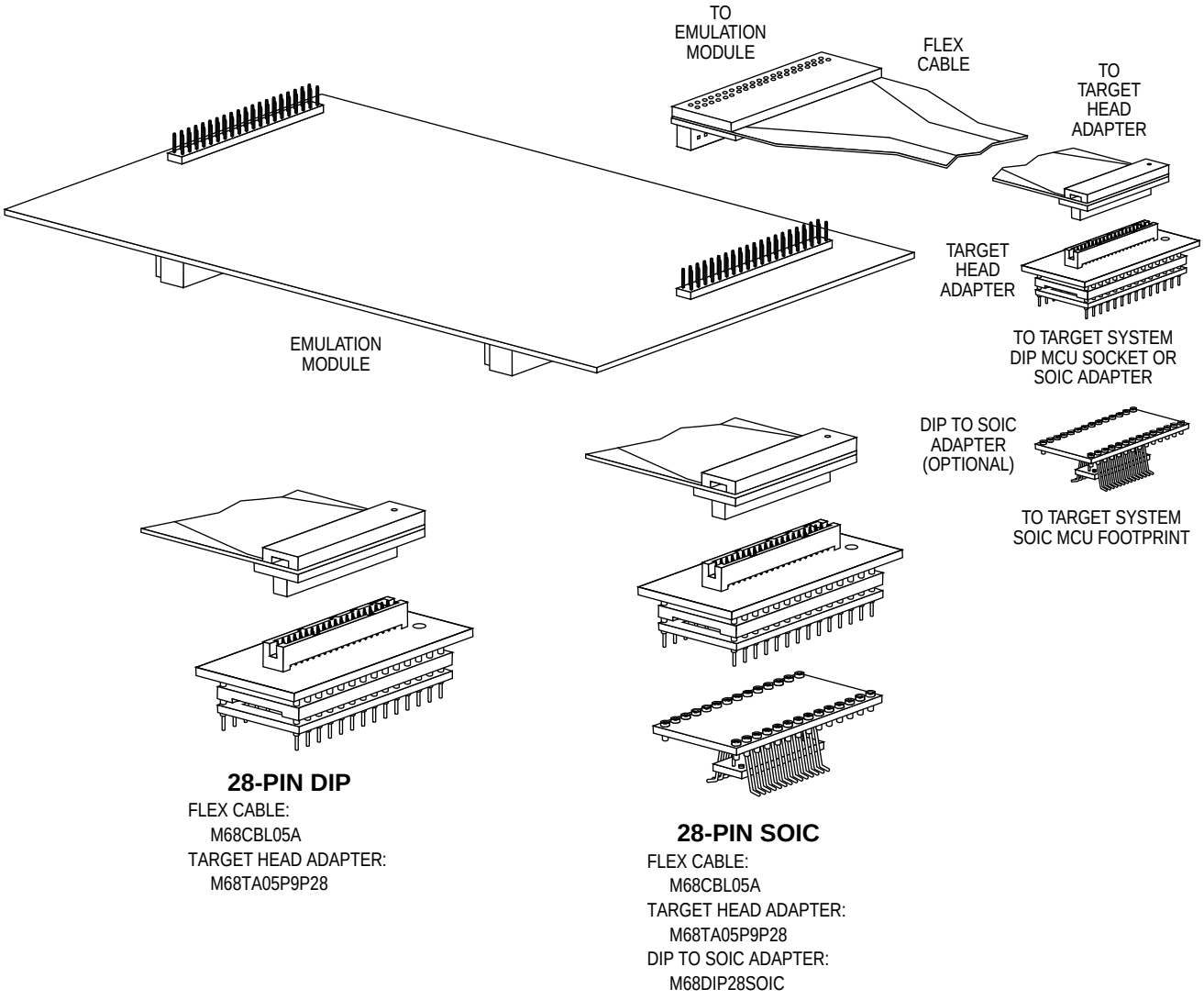


Figure 2. Target Cable Assembly

The MCU package in the target system determines the target cable assembly components required:

- For a 28-pin DIP package, use flex cable M68CBL05A and target head adapter M68TA05P9P28.
- For a 28-pin SOIC package, use the flex cable assembly for the 28-pin DIP in conjunction with SOIC adapter M68DIP28SOIC.

Connector Information

The connectors on the M68EML05P6A module provide access to the user mode emulation signals (J2) as well as select internal signals (J1). Connector J2 is used as a cable interface to a user's target system, while connector J1 is used to connect a logic analyzer.

Target Cable Connector Pin Assignments

Figure 3 shows the pin assignments for connector J2. **Table 1** lists signal descriptions for connector J2.

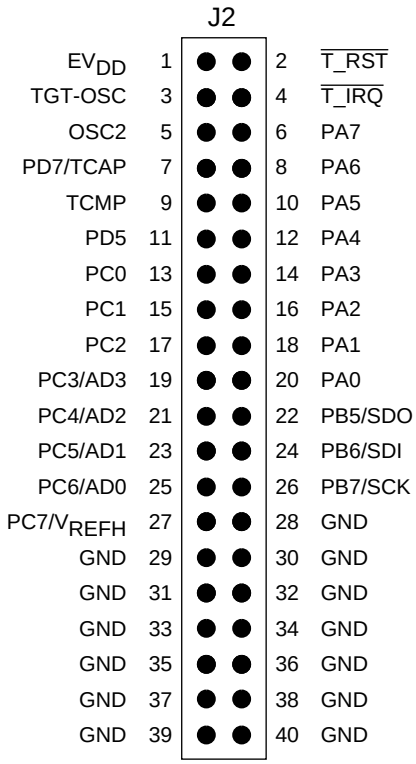


Figure 3. Target Connector Pin Assignment

Table 1. Connector J2 Signal Descriptions

Pin	Mnemonic	Signal
1	EV_{DD}	EXTERNAL VOLTAGE DETECT — V_{DD} input signal from target used by the emulator to detect target system voltage
2	T_RST	TARGET RESET — Active-low input signal that starts a system reset
3	TGT–OSC	TARGET OSCILLATOR 1 — A possible clock source input for the M68EML05P6A board; system bus frequency is OSC1 ÷ 2; signal use is controlled by jumper header W2
4	T_IRQ	TARGET INTERRUPT REQUEST — Active-low input signal from the target that asynchronously applies an MCU interrupt
5	OSC2	OSCILLATOR 2 — Output clock signal at two times the internal bus frequency
6, 8, 10, 12, 14, 16, 18, 20	PA7–PA0	PORT A (bits 7–0) — General-purpose I/O lines controlled by software via data direction and data registers
7	PD7/TCAP	PORT D (bit 7) — General-purpose input-only line TIMER CAPTURE — Input signal used by the input capture feature of the MCU programmable timer system
9	TCMP	TIMER COMPARE — Output signal used by the output compare feature of the MCU programmable timer system
11	PD5	PORT D (bit 5) — General-purpose I/O line controlled by software via data direction and data registers
13, 15, 17	PC0–PC2	PORT C (bits 0–2) — General-purpose I/O lines controlled by software via data direction and data registers
22, 24, 26	PB5–PB7 / SDO, SDI, SCK	PORT B (bits 5–7) — General-purpose I/O lines controlled by software via data direction and data registers SIOP SIGNALS — If the serial I/O port (SIOP) is enabled, these pins are the serial communications pins. Pin 22 is the serial data output (SDO), Pin 24 is the serial data input (SDI) and pin 26 is the serial clock (SCK).
19, 21, 23, 25, 27	PC3–PC7 / AD3–AD0, V_{REFH}	PORT C (bits 3–7) — General-purpose I/O lines controlled by software via data direction and data registers A/D INPUTS — If the analog-to-digital (A/D) subsystem is enabled, then the pins become A/D inputs. Pins 19, 21, 23, and 25 become A/D channel 3, 2, 1, and 0, respectively. Pin 27 is voltage reference high (V_{REFH}). Use of the V_{REFH} input is controlled by jumper header W1.
28–40	GND	GROUND

Logic Analyzer Connector Pin Assignments

Figure 4 shows the pin assignments for logic analyzer connector J1. This connector provides the emulator easy access to many of the signals used internally. **Table 2** lists signal descriptions for this connector.

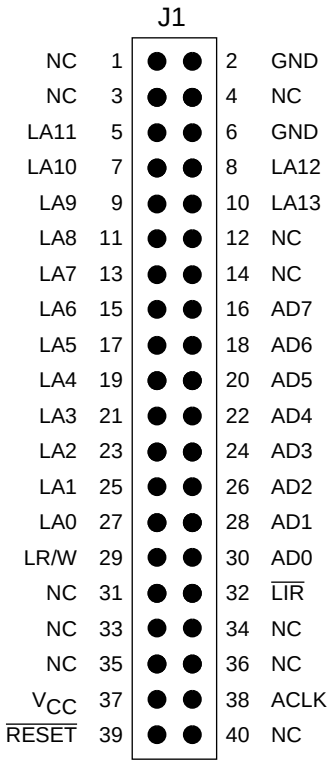


Figure 4. Connector J1 Pin Assignments

Table 2. Logic Analyzer Connector J1 Signal Descriptions

Pin	Mnemonic	Signal
1, 3, 4, 10, 12, 14, 31, 33, 34, 35, 36	NC	No connection
2, 6	GND	GROUND
5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27	LA11–LA0	LATCHED ADDRESSES (bits 11–0) — MCU latched output address bus
8	LA12	LATCHED ADDRESSES (bits 13–12) — MCU latched output address bus
16, 18, 20, 22, 24, 26, 28, 30	AD7–AD0	ADDRESS/DATA BUS (bits 7–0) — MCU multiplexed address/data bus
29	LR/W	LATCHED READ/WRITE — The MCU's write signal is latched and used on the platform board to control emulator memory accesses.
32	$\overline{\text{LIR}}$	LOAD INSTRUCTION REGISTER — Active-low signal indicating an opcode fetch cycle is in process
37	V_{CC}	+5 Vdc POWER — Connection to the system voltage V_{CC}
38	ACLK	ANALYZER CLOCK — The latched addresses are valid on the latched address bus at the rising edge of ACLK. Also, data is valid on the AD bus at ACLK's rising edge.
39	$\overline{\text{RESET}}$	RESET — Active-low signal will be asserted during internally or externally caused resets.
40	TEST	TEST — Used for factory test

General Description

MMDS/MMEVS Configuration and Operation

Contents

Introduction

The following paragraphs explain how to configure and use your M68EML05P6A as part of an MMDS or MMEVS system. For other parts of system installation and configuration, see either the *MMDS0508 Operations Manual* (MMDS0508OM/D) or *MMEVS05/MMEVS08 Operations Manual* (MMEVS0508OM/D).

The topics covered in this chapter are:

- **Setting M68EML05P6A Jumper Headers** on page 21 explains how to set the M68EML05P6A jumper headers.
- **Remaining System Installation** on page 27 covers the final steps to system installation.
- **Personality Files Usage** on page 28 discusses the personality file used on the M68EML05P6A board.
- **Emulation Specifics** on page 29 explains special considerations for emulating with this module.
- **Installing Other MCU Devices** on page 32 details possibilities for installing other MC68HC05PxA devices as the resident MCU.

NOTE: *You can configure an M68EML05P6A already installed in the system platform board. To do so, remove system power and then follow the guidance of this chapter.*

CAUTION: *Be sure to switch off power before you reconfigure an installed EM. Reconfiguring EM jumper headers with the power on can damage emulation circuits.*

Setting M68EML05P6A Jumper Headers

Your M68EML05P6A has four jumper headers – W1 through W4 and two sets of DIP switches. **Table 3** provides a quick reference for configuration options. Refer to the paragraphs that follow for a more detailed explanation.

Table 3. Jumper Header and Switch Positions

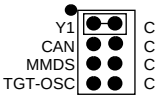
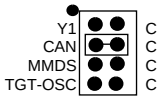
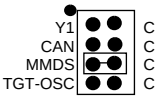
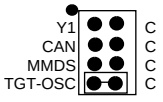
Jumper Header	Position	Description	Factory Setting
A/D Converter Voltage Reference Header, W1		Tie V_{REFH} to the L_{VDD} power plane on the EM	X
		Tie V_{REFH} pins to its input pin on connector J2	
Clock Source Select, W2		Select the crystal oscillator circuit located on the EM board at Y1. Requires populating the EM with components Y1, R8, R9, C21, and C22	
		Select the 4-MHz canned oscillator located on the EM board at XY2.	X
		Select the clock originating from the platform board. The frequency, set to 2 MHz on power up, is controlled by the OSC command.	
		Select a user supplied clock source. The clock is input to the TGT-OSC pin on connector J2 through a target cable assembly.	

Table 3. Jumper Header and Switch Positions (Continued)

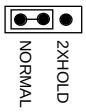
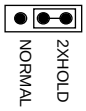
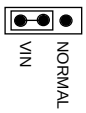
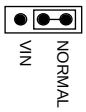
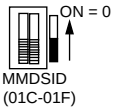
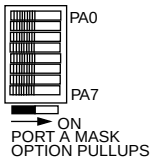
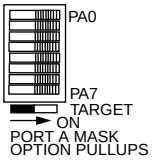
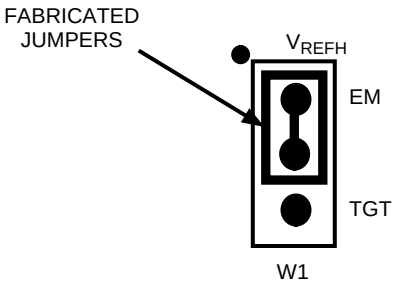
Jumper Header	Position	Description	Factory Setting
$\overline{IRQ}$ Level Select, W3		After reset, drop high voltage on $\overline{IRQ}$ to operating voltage when not asserting $\overline{IRQ}$ low.	X
		Hold high voltage on $\overline{IRQ}$ when not asserting $\overline{IRQ}$ low. For factory test only.	
$\overline{IRQ}$ Source Select, W4		Use the voltage input to P3 as the high-voltage source for the $\overline{IRQ}$ pin control. For factory test only.	
		Use the EM's chargepump (~12 V) as the high-voltage source for the $\overline{IRQ}$ pin control.	X
Emulation MCU Control, SW1	 MMDSID (01C-01F)	Switch setting determines which MCU device is emulated. Switch setting is read at start of debugger software. Switch left / Switch right / Device Emulated / EM Id no. up / up / HC05P9A / $01C up / down / HC705P6A / $01D down / up / HC05P4A / $01E down / down / HC05P1A / $01F	X

Table 3. Jumper Header and Switch Positions (Continued)

Jumper Header	Position	Description	Factory Setting
Port A Interrupt Mask Option Control, SW2		Each port A bit is individually configurable. In the left position, the option is **not** selected.	X
		In the right position, the option **is** selected.	

A/D Converter Voltage Reference Header – W1

The A/D voltage reference header controls the input to the voltage reference high (V_{REFH}) pin of the MCU. The factory configured position applies the MCU's operating voltage to the V_{REFH} pin.



Alternatively, you may supply the reference voltage through the target cable connected to connector J2 of the M68EML05P6A emulation module. To do so, reposition the W1 jumper to the TGT position.

External Clock Source Select Header – W2

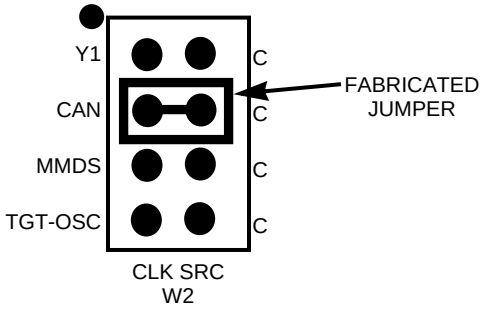
Jumper header W2 determines the source of the external clock signal. The diagram here illustrates the jumper header where the pins marked C indicate common pins. The default configuration selects the 4-MHz canned oscillator clock source at board location XY2.

The external clock has three other possible sources. One source, from the platform board, requires repositioning the W2 jumper between pins MMDS and C and then using the system's OSC command to select a frequency.

For a user supplied clock source coming through a target cable connected to J2, reposition the W2 jumper between pins TGT_OSC and C.

NOTE: *The user supplied source through the target cable should be a CMOS-level square wave.*

The fourth possible external clock source is a user supplied crystal oscillator circuit. The M68EML05P6A has been designed with an unpopulated crystal circuit. For this source, reposition the W2 jumper between pins Y1 and C and supply the components for the Y1 crystal circuit. The IC device at location U14 is an 74HCU04 inverter and provides the inverter for a standard single inverter oscillator. The user supplies the appropriate crystal, resistors, and capacitors for operating the external clock at a particular frequency. See **M68EML05P6A Schematics (Sheet 5 of 7)** on page 43 for schematic details of the crystal circuit.



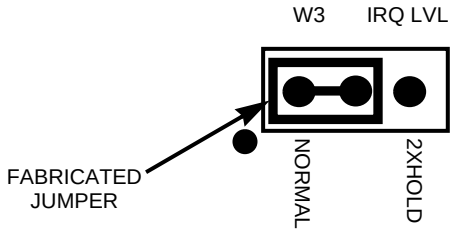
$\overline{\text{IRQ}}$ Level Control Header – W3

When the MC68HC705P6A is in reset, the $\overline{\text{IRQ}}$ voltage level is at the voltage determined by $\overline{\text{IRQ}}$ source control header W4. The $\overline{\text{IRQ}}$ level control header W3 controls the voltage level on the $\overline{\text{IRQ}}$ pin during routine operation, when the external $\overline{\text{IRQ}}$ is not asserted and the part is not in reset.

If jumper header W3 is in the NORMAL position, the $\overline{\text{IRQ}}$ level will drop to the MCU operating voltage once the part comes out of reset.

If the jumper header is in the 2XHOLD position, the $\overline{\text{IRQ}}$ level will be held at the voltage determined by $\overline{\text{IRQ}}$ source control header W4.

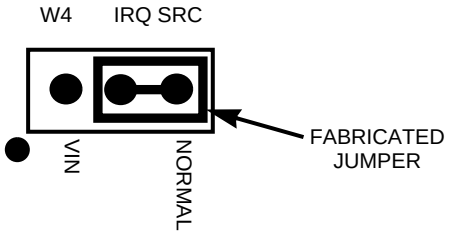
NOTE: *The only time the W3 jumper header should be in the 2XHOLD position is for factory testing.*



$\overline{\text{IRQ}}$ Source Control Header – W4

Jumper header W4 determines the source for high voltage applied to the $\overline{\text{IRQ}}$ pin. In the NORMAL position, the voltage is supplied from the development systems chargepump (~12 V). In the V_{PP} position, the voltage is supplied from the user through lever terminal connector P3.

NOTE: *The W4 jumper header should be in the V_{PP} position only for factory testing.*



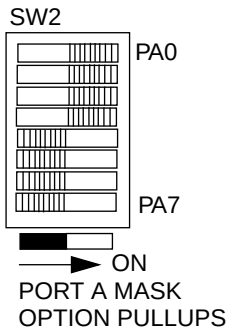
MMDS ID Control Switch – SW1

The development system software uses specific personality files to emulate the MCUs supported on the M68EML05P6A emulation module. When entering the debugger software, the set ID for the module is read and the appropriate personality file is loaded. The two positions of switch SW1, representing the two low bits of a 10-bit ID, allow multiple IDs to be read by the host software. See **Personality Files Usage** on page 28 for proper switch position.

Port A Interrupt Mask Option Control Switch – SW2

The eight positions of switch SW2 enable or disable the port A interrupt mask options. Each position controls one port A line. A switch in the left position, OFF, disables the option; a switch in the right position, ON, enables the option.

If a mask option is enabled (switched ON) and the corresponding bit of the port A data direction register is configured as an input, a low on the port A pin generates an interrupt. The diagram below shows a possible setting: interrupt masks are disabled for port A lines 0 through 3 and enabled for port A lines 4 through 7.



The default setting for all eight positions of SW2 is OFF.

Remaining System Installation

When headers W1–W4 have been configured and switches SW1 and SW2 have been set, M68EML05P6A configuration is complete.

- Ensure that the power to the development tool is off.
- If installing the M68EML05P6A in an MMDS station module, remove the panel from the station module top.
- Fit together EM connectors P1 and P2 on the bottom of the board and platform board DIN connectors. Snap the corners of the EM onto the plastic standoffs.
- Connect the target cable, if appropriate.
- If installing in an MMDS, replace the panel.

At this point, the remaining cable connections can be made, as necessary, and power restored.

For instructions, consult either the *MMEVS05/MMEVS08 Operations Manual* (MMEVS0508OM/D) or *MMDS0508 Operations Manual* (MMDS0508OM/D).

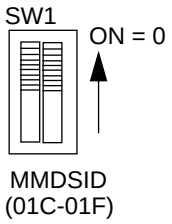
Personality Files Usage

The development system uses specific personality files to emulate the MCUs supported on the M68EML05P6A board. The debugger software loads a personality file upon power up. Switch SW1 enables the module to emulate the four MCUs supported. The diagram below shows the 2-position DIP switch that controls which MCU is emulated. The personality files needed for this module are on an individual disk included with the EM board.

NOTE: *Note that personality file names follow the pattern 00ZZZVxx.MEM, where ZZZ is the EM identifier or MCU name and xx is the version of the file.*

Table 4. SW1 Switch Settings

MCU Emulated	SW1–1	SW1–2	Associated .MEM Personality File
MC68HC05P9A	Up	Up	0001CVxx.MEM
MC68HC705P6A	Up	Down	0001DVxx.MEM
MC68HC05P4A	Down	Up	0001EVxx.MEM
MC68HC05P1A	Down	Down	0001FVxx.MEM



Emulation Specifics

The following paragraphs detail differences between the performance of an MC68HC705P6A MCU run in single-chip operation and the way certain features will perform during emulation.

Mask Option Register (MOR) Control

In single-chip mode operation:

The MCU mask options will be determined by which options have been programmed in the MOR EPROM locations ($1EFF–$1F00) of the resident MC68HC705P6A MCU. These registers must be programmed using a dedicated programmer.

In emulation:

The eight mask option bits controlling the port A pullup/interrupt feature (location $1EFF) are rebuilt externally to the MCU and are enabled through setting the 8-position DIP switch SW2.

The initial settings for the other 8-mask option bits will be determined by what has been programmed in the MOR EPROM location ($1F00). Alternatively, the mask options can be controlled via software and allow mask option changes during a debug session. Option changes can be accomplished by command entry (for instance, the MM command) or by execution of user code (for instance, STA instruction).

The procedure for changing $1F00 mask option register options during an emulation session requires manipulation of the programming register at location $001C and the MOR location $1F00. First set bit 7 of register $001C (write a $80 to location $001C). If you use the memory modify (MM) command, a "write did not verify" message should be ignored. The mask options can then be set by writing the desired mask option register byte value to the MOR location ($1F00).

The selected mask options will return to the default options programmed in the MOR EPROM location if the MCU takes any reset.

See **COP Emulation** on page 30 for further steps required to enable the computer operating properly (COP) feature.

COP Emulation

In single-chip mode operation:

The computer operating properly (COP) feature is enabled if the COP bit of the mask option register (MOR) has been programmed. The MOR register must be programmed using a dedicated programmer.

In emulation:

The COP bit in the MOR can be set by two methods. The bit can be programmed by using a dedicated programmer prior to using the MCU in the emulator. Alternatively, the option can be set during a debug session using the method outlined in **Mask Option Register (MOR) Control** on page 29.

Only setting the COP bit does not enable the mask option. In addition, a value of #$04 must be written to the reserved register $001F. If you use the memory modify (MM) command, a "write did not verify" message should be ignored.

Note that any type of MCU reset will disable the COP, and the steps required to enable the COP must be repeated.

Port A Pullups/Interrupts

In single-chip mode:

The simple port A I/O feature and the associated interrupt/pullup mask options are implemented through the port A pins of the MC68HC(7)05PxA MCU. With this implementation, an interrupt service routine could poll the external IRQ pin using BIL and BIH statements and determine if the source of an interrupt was the external IRQ pin or one of the enabled port A interrupts.

In emulation:

The port A I/O function is rebuilt off-chip and the enabled interrupt/pullup options will generate interrupts through the external IRQ pin. An interrupt service routine using BIL and BIH instructions could not determine if an interrupt was generated via an external IRQ pin or one of the enabled port A interrupts. The proper way to differentiate between a port interrupt and an external interrupt is to have the interrupt service routine poll possible port A interrupts. If none are low, then the interrupt was driven by an external IRQ.

Port C Sharing with the A/D Subsystem

In single-chip mode operation:

Port C's bit 7–3 pins are shared with the A/D subsystem. When the A/D is enabled, the pins become the A/D inputs. The external port C bits are not available to the CPU. Port C data and data direction bits are still accessible from the CPU, although they have no effect on the external port C pins. If the A/D subsystem is disabled, port C functionality will be restored to the external pin, and the last conditions stored in the port C registers will determine data and direction for the simple I/O.

In emulation:

Port C is rebuilt external to the MCU while the A/D inputs continue to be at the MCU pin. To prevent the port C source from affecting the A/D function, associated port C bits should be made an input (by clearing the DDRC bit) before enabling the A/D.

Pullup on $\overline{IRQ}$

In single-chip mode operation:

There is no pullup on the $\overline{IRQ}$ pin. Your application must pull the $\overline{IRQ}$ pin to V_{DD} level to prevent interrupts due to a floating input.

In emulation:

The $\overline{IRQ}$ pin is pulled up on the module. Be aware that an application without the $\overline{IRQ}$ pin pulled high will emulate correctly but will fail in the application because of a floating IRQ line. The $\overline{IRQ}$ pin pulled high on the module causes these results.

$\overline{IRQ}/V_{PP}$ Input Pin

In single-chip mode operation:

The $\overline{IRQ}/V_{PP}$ pin drives the asynchronous IRQ interrupt function of the CPU. The pin also is used for programming voltage when programming the user EPROM or the MOR.

In emulation:

The $\overline{IRQ}/V_{PP}$ signal supplied to connector J2 through a target cable only drives the asynchronous IRQ interrupt function.

A V_{PP} voltage should not be supplied to the $\overline{IRQ}/V_{PP}$ pin in a target application while the emulator is connected.

MC68HC05P1A Location $1F00

In single-chip mode operation:

The MC68HC05P1A ROM location $1F00 is the first byte of the upper block of user ROM.

In emulation:

The MC68HC05P1A is emulated with an MC68HC705P6A installed as the resident MCU. Because the MC68HC705P6A has the mask option register at this location, $1F00 cannot be emulated as user ROM.

Installing Other MCU Devices

With an MC68HC705P6A MCU installed as the resident MCU (location U5), the M68EM05EMP6A module will emulate the MC68HC705P6A, MC68HC05P1A, MC68HC05P4A, and MC68HC05P9A MCUs. Thus, the module is shipped with an MC68HC705P6A device installed.

Installing one of these other supported devices as the resident MCU is possible. This allows use of other MCU devices.

To install another device:

- Ensure that development system power is off.
- Replace the resident MC68HC705P6A MCU at location U5 with the new MCU device.

NOTE: *Be aware that when ROM MCUs are the resident MCU, the mask options are determined by what has been masked on the resident device.*

Schematics

Contents

M68EML05P6A Schematics

Refer to the following pages for the seven sheets of schematics for the M68EML05P6A emulation module.

Schematics

M68EML05P6A Schematics (Sheet 1 of 7)

M68EML05P6A EMULATION MODULE

REVISIONS				
ECN #	PCB REV	SCH REV	DESCRIPTION	DATE
125	0	2	Test mode timing is on E and not PH2 as expected. Change clock for early signals to PH2*. Cut LOCKOUT from U6 SETDFF pin. Cut LVDD from the U2 SETDFF pin. Diode on WR_DDRD signal to ensure write of 0 to DDRD7. Redo RESET circuit for LV Bidi.	10/21/96
126	A	3	Implement modifications from ECO 125 in new rev of PWB.	10/22/96

NOTES, UNLESS OTHERWISE SPECIFIED

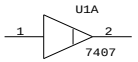
1. VCC PIN LOCATIONS :

   VCC IS APPLIED TO PIN 8 OF ALL 8-PIN IC's, PIN 14 OF ALL 14-PIN IC's, PIN 16 OF ALL 16-PIN IC's, PIN 20 OF ALL 20-PIN IC's, ETC.

2. GROUND PIN LOCATIONS :

   GROUND IS APPLIED TO PIN 4 OF ALL 8-PIN IC's, PIN 7 OF ALL 14-PIN IC's, PIN 8 OF ALL 16-PIN IC's, PIN 10 OF ALL 20-PIN IC's, ETC.

3. DEVICE TYPE, PIN NUMBERS, AND REFERENCE DESIGNATOR OF GATES ARE SHOWN AS FOLLOWS :



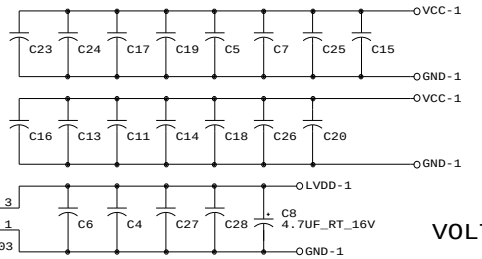
   7407 = DEVICE TYPE
   1 AND 2 = PIN NUMBERS
   U1A = REFERENCE DESIGNATORS

4. RESISTANCE VALUES ARE IN OHMS.
5. RESISTORS ARE 1/4 WATT, 5%.
6. CAPACITANCE VALUES ARE IN MICROFARADS.

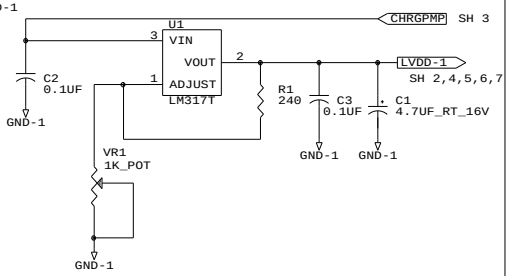
Decouple Caps for ICs as labeled.
All caps are 0.1 uF @ 50 V

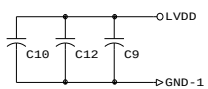
GROUND PLANE ----> GND-1

SPLIT POWER PLANE ----> VCC-1 & LVDD-1

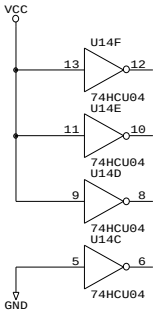


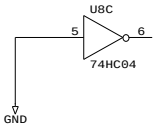
VOLTAGE REGULATOR

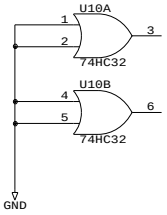


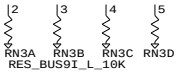


Spare Gates









ORCAD IV FLAT FILES

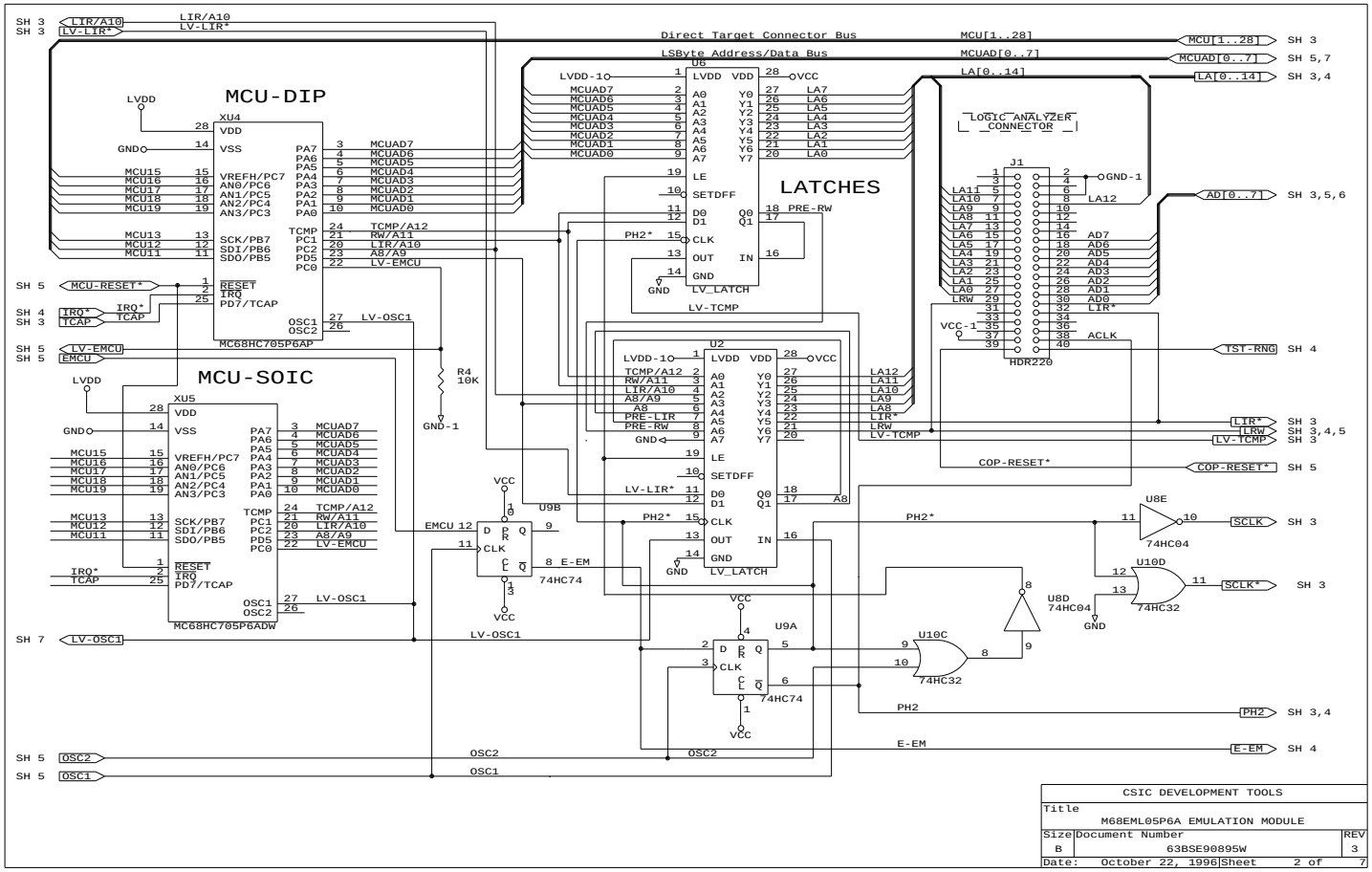
LINK
LP6AR3S2.SCH
LP6AR3S3.SCH
LP6AR3S4.SCH
LP6AR3S5.SCH
LP6AR3S6.SCH
LP6AR3S7.SCH

COMPUTER GENERATED DRAWING : DO NOT REVISE MANUALLY

CSIC DEVELOPMENT TOOLS		
Title: M68EML05P6A EMULATION MODULE		
Size: B	Document Number: 63BSE90895W	REV: 3
Date: October 22, 1996	Sheet 1 of 7	

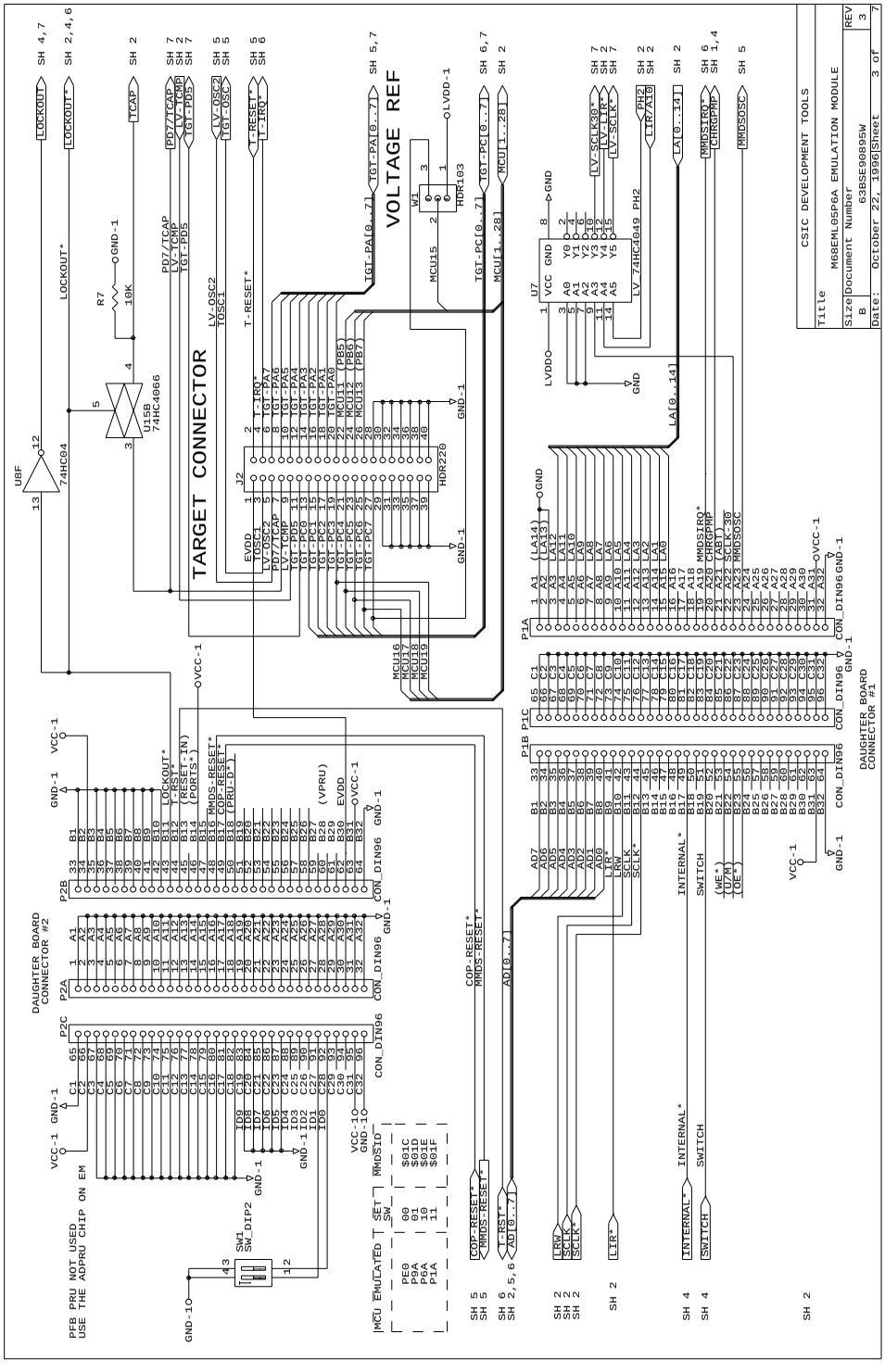
Schematics

M68EML05P6A Schematics (Sheet 2 of 7)



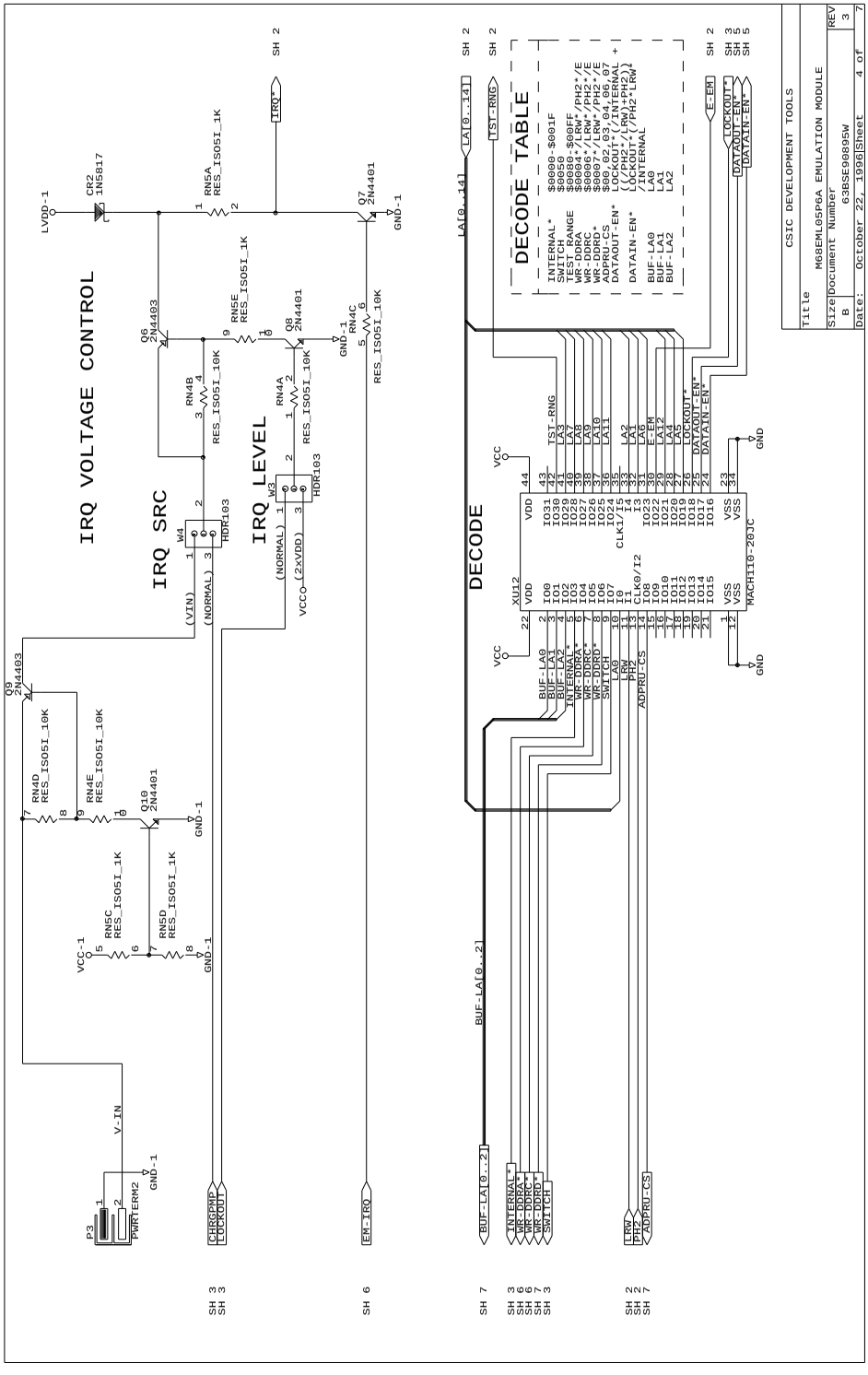
Schematics

M68EML05P6A Schematics (Sheet 3 of 7)



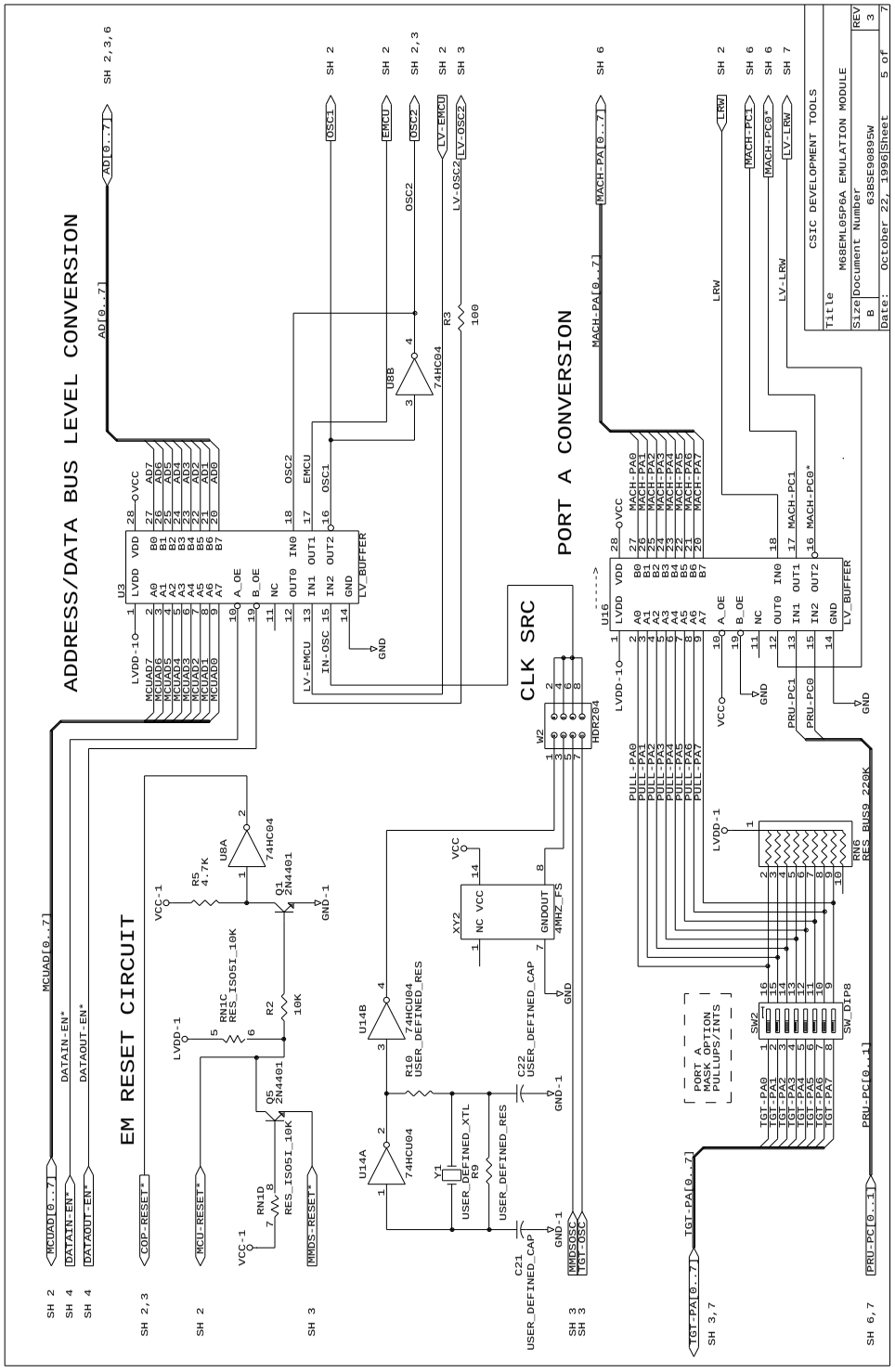
Schematics

M68EML05P6A Schematics (Sheet 4 of 7)



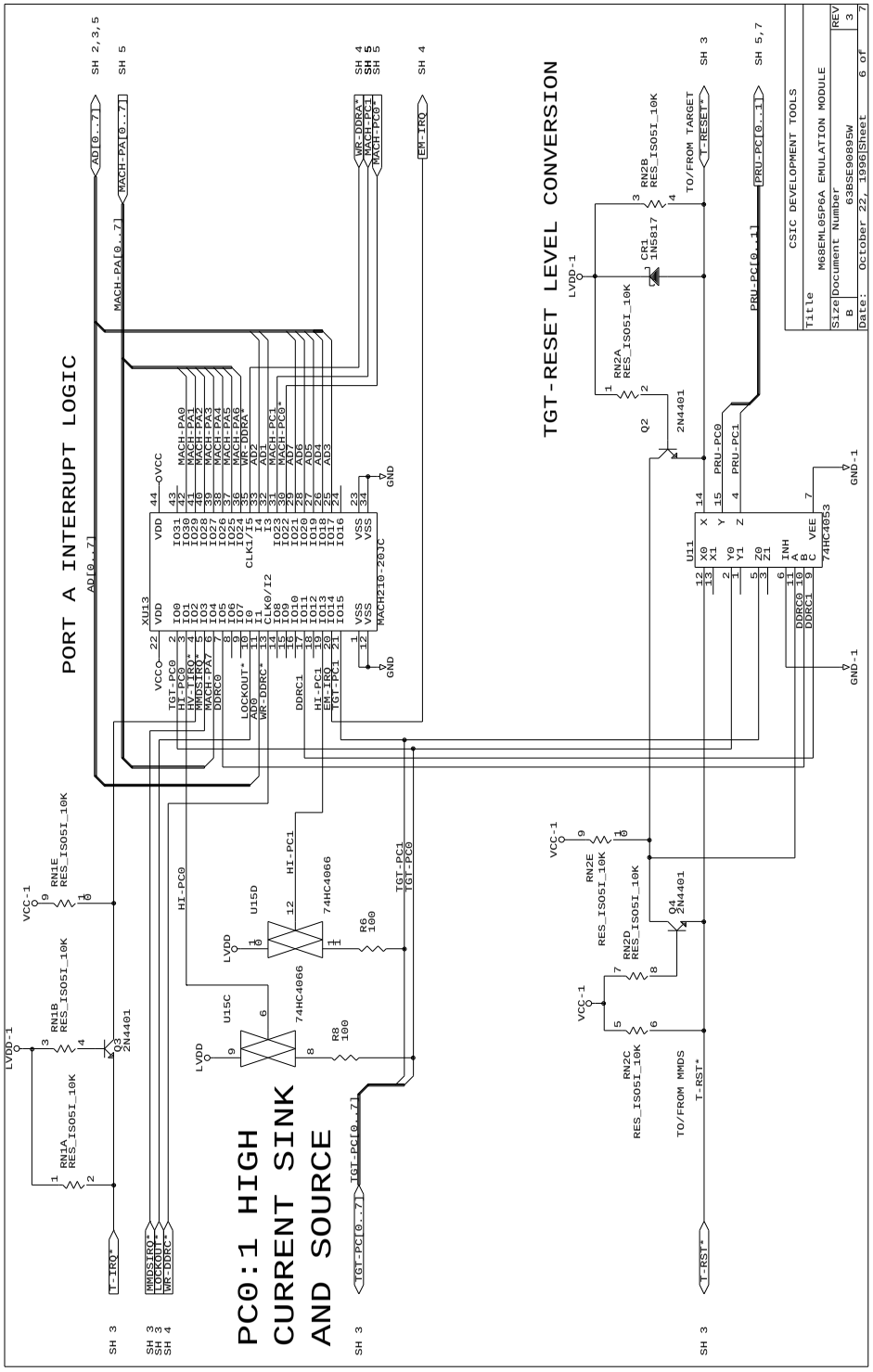
Schematics

M68EML05P6A Schematics (Sheet 5 of 7)



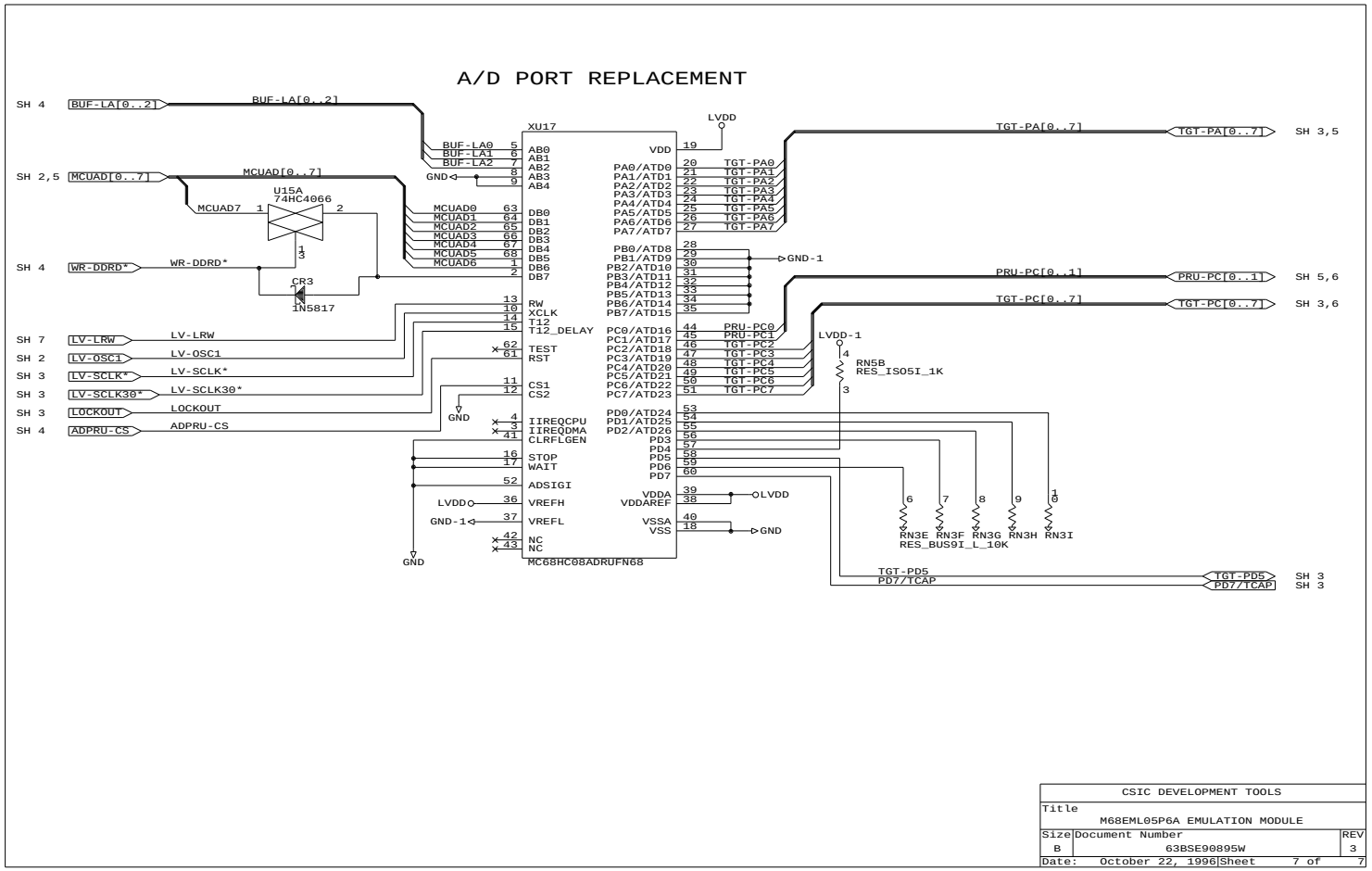
Schematics

M68EML05P6A Schematics (Sheet 6 of 7)



Schematics

M68EML05P6A Schematics (Sheet 7 of 7)



Schematics

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