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MC68F333

User's Manual Addendum
32-Bit Modular Microcontroller

1 Introduction

The MC68F333 contains two flash electrically erasable programmable read-only memory (EEPROM) modules: a 16 Kbyte module and a 48 Kbyte module.

The flash EEPROM modules serve as nonvolatile, fast-access, electrically erasable and programmable ROM-emulation memory. The modules can contain program code (e.g., operating system kernels and standard subroutines) which must execute at high speed or is frequently executed, or static data which is read frequently. The flash EEPROM supports both byte and word reads. It is capable of responding to back-to-back IMB accesses to provide two bus cycle (four system clock) access for aligned long words. It can also be programmed to insert up to three wait states to accommodate migration from slower external development memory to onboard flash EEPROM without the need for retiming the system.

The 16 Kbyte flash EEPROM array can begin on any 16 Kbyte boundary, and the 48 Kbyte array can begin on any 64 Kbyte boundary. The two arrays can be configured to appear as a single contiguous memory block, with the 16 Kbyte array immediately preceding or immediately following the 48 Kbyte array. They can be individually configured to reside in supervisor or unrestricted address space. They can also be programmed to reside in either program space or data space.

Pulling data bus pins DATA15 and DATA14 low during reset disables both the 16- and 48-Kbyte flash EEPROM modules and places them in stop mode.

The flash EEPROM and its control bits are erasable and programmable under software control. Program/erase voltage must be supplied via external V_{FPE} pins. Data is programmed in byte or word aligned fashion. Multiple word programming is not supported. The flash EEPROM modules support bulk erase only, and have a minimum program-erase life of 100 cycles.

The flash EEPROM modules have hardware interlocks which protect stored data from corruption by accidental enabling of the program/erase voltage to the flash EEPROM arrays. With the hardware interlocks, inadvertent programming or erasure is highly unlikely.

1.1 Address Map

Table 1 shows the flash EEPROM module address map.

Table 1 Flash EEPROM Address Map

Address	Register	Module
$YFF800[1]	FLASH EEPROM MODULE CONFIGURATION (FEE1MCR)	16 KBYTE FLASH EEPROM
$YFF802	FLASH EEPROM TEST REGISTER (FEE1TST)	
$YFF804	FLASH EEPROM BASE ADDRESS HIGH (FEE1BAH)	
$YFF806	FLASH EEPROM BASE ADDRESS LOW (FEE1BAL)	
$YFF808	FLASH EEPROM CONTROL REGISTER (FEE1CTL)	
$YFF80A	RESERVED	
$YFF80C	RESERVED	
$YFF80E	RESERVED	
$YFF810	FLASH EEPROM BOOTSTRAP WORD 0 (FEE1BS0)	
$YFF812	FLASH EEPROM BOOTSTRAP WORD 1 (FEE1BS1)	
$YFF814	FLASH EEPROM BOOTSTRAP WORD 2 (FEE1BS2)	
$YFF816	FLASH EEPROM BOOTSTRAP WORD 3 (FEE1BS3)	
$YFF818	RESERVED	
$YFF81A	RESERVED	
$YFF81C	RESERVED	
$YFF81E	RESERVED	
$YFF820	FLASH EEPROM MODULE CONFIGURATION (FEE2MCR)	48 KBYTE FLASH EEPROM
$YFF822	FLASH EEPROM TEST REGISTER (FEE2TST)	
$YFF824	FLASH EEPROM BASE ADDRESS HIGH (FEE2BAH)	
$YFF826	FLASH EEPROM BASE ADDRESS LOW (FEE2BAL)	
$YFF828	FLASH EEPROM CONTROL REGISTER (FEE2CTL)	
$YFF82A	RESERVED	
$YFF82C	RESERVED	
$YFF82E	RESERVED	
$YFF830	FLASH EEPROM BOOTSTRAP WORD 0 (FEE2BS0)	
$YFF832	FLASH EEPROM BOOTSTRAP WORD 1 (FEE2BS1)	
$YFF834	FLASH EEPROM BOOTSTRAP WORD 2 (FEE2BS2)	
$YFF836	FLASH EEPROM BOOTSTRAP WORD 3 (FEE2BS3)	
$YFF838	RESERVED	
$YFF83A	RESERVED	
$YFF83C	RESERVED	
$YFF83E	RESERVED	

1. Y = M111, where M is the logic state of the module mapping (MM) bit in the SCIMCR.

1.2 Flash EEPROM Control Block

Each flash EEPROM module has a 32 byte control block with five registers to control flash EEPROM operation: the flash EEPROM module configuration register (FEE1MCR, FEE2MCR), the flash EEPROM test register (FEE1TST, FEE2TST), the flash EEPROM array base address registers (FEE1BAH, FEE2BAH, and FEE1BAL, FEE2BAL), and the flash EEPROM control register (FEE1CTL, FEE2CTL). Four additional flash EEPROM words in the control block can contain bootstrap information for use during reset. Control registers are located in supervisor data space.

The control register blocks for the 16 Kbyte and 48 Kbyte flash EEPROM modules start at locations $YFF800 and $YFF820, respectively. The following register descriptions apply to the corresponding register in either control block. References to FEExMCR, for example, apply to both FEE1MCR (in the 16 Kbyte module) and FEE2MCR (in the 48 Kbyte module.)

A number of control register bits have associated bits in “shadow” registers. The values of the shadow bits determine the reset states of the control register bits. Shadow registers are programmed or erased in the same manner as a location in the array, using the address of the corresponding control registers. When a shadow register is programmed, the data is not written to the corresponding control register. The new data is not copied into the control register until the next reset. The contents of shadow registers are erased when the array is erased.

Configuration information is specified and programmed independently of the array. After reset, registers in the control block that contain writable bits can be modified. Writes to these registers do not affect the associated shadow register. Certain registers can be written only when LOCK = 0 or STOP = 1 in FEExMCR.

1.3 Flash EEPROM Array

The base address registers specify the starting address of the flash EEPROM array. The user programs the reset base address. The base address of the 16 Kbyte array must be on a 16 Kbyte boundary; the base address of the 48 Kbyte array must be on a 64 Kbyte boundary. Behavior will be indeterminate if one flash EEPROM array overlaps the other.

The base address must also be set so that an array does not overlap a flash EEPROM control block in the data space memory map. If an array does overlap a control block, accesses to the 32 bytes in the array that are overlapped are ignored, allowing the flash EEPROM control blocks to remain accessible. If the array overlaps the control block of another module, the results will be indeterminate.

1.4 Flash EEPROM Registers

In the following register diagrams, bits with reset states determined by shadow bits are shaded, and the reset state is annotated “SB”.

FEE1MCR, FEE2MCR — Flash EEPROM Module Configuration Registers **$YFF800, $YFF820**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STOP	FRZ	0	BOOT	LOCK	0	ASPC[1:0]		WAIT[1:0]		0	0	0	0	0	0
RESET:															
FEE1MCR															
$\overline{\text{DATA15}}$ + SB	0	0	SB	SB	0	SB	SB	SB	SB	0	0	0	0	0	0
FEE2MCR															
$\overline{\text{DATA14}}$ + SB	0	0	SB	SB	0	SB	SB	SB	SB	0	0	0	0	0	0

The flash EEPROM module configuration registers (FEE1MCR, FEE2MCR) control module configuration. This register can be written only when LOCK = 0. All active bits in the FEExMCR take values from the associated shadow register during reset.

STOP — Stop Mode Control

0 = Normal operation

1 = Low-power stop operation

STOP can be set either by pulling the appropriate data bus pin low during reset (DATA15 for FEE1MCR and DATA14 for FEE2MCR) or by the corresponding shadow bit. The array can be re-enabled by clearing STOP. If STOP is set during programming or erasing, the program/erase voltage is automatically turned off. However, the ENPE control bit in FEExCTL remains set. When STOP is cleared, the program/erase voltage is automatically turned back on if ENPE is set.

FRZ — Freeze Mode Control

0 = Disable program/erase voltage while FREEZE is asserted

1 = Allow ENPE bit to turn on the program/erase voltage while FREEZE is asserted

BOOT — Boot Control

0 = Flash EEPROM module responds to bootstrap addresses after reset

1 = Flash EEPROM module does not respond to bootstrap addresses after reset

On reset, BOOT takes on the value stored in its associated shadow bit. If BOOT = 0 and STOP = 0, the module responds to program space accesses to IMB addresses $000000 to $000006 following reset, and the contents of FEExBS[3:0] are used as bootstrap vectors. After address $000006 is read, the module responds normally to control block or array addresses only.

LOCK — Lock Registers

0 = Write-locking disabled

1 = Write-locked registers protected

If the reset state of LOCK is zero, it can be set once after reset to allow protection of the registers after initialization. Once the LOCK bit is set by software, it cannot be cleared again until after a reset. Execution of the CPU32 RESET instruction has no effect on the LOCK bit.

ASPC[1:0] — Flash EEPROM Array Space

ASPC[1:0] assigns the array to supervisor or user space, and to program or data space. The state of ASPC[1:0] out of reset is determined by the value stored in the associated shadow bits. The field can be written only when LOCK = 0 and STOP = 1. Refer to **Table 2**.

Table 2 Array Space Encoding

ASPC[1:0]	Type of Access
00	Unrestricted program and data space
01	Unrestricted program space
10	Supervisor program and data space
11	Supervisor program space

WAIT[1:0] — Wait States

The state of WAIT[1:0] out of reset is determined by the value stored in the associated shadow bits. WAIT[1:0] specifies the number of wait states inserted during accesses to the flash EEPROM module. A wait state has the duration of one system clock cycle. WAIT[1:0] affects both control block and array accesses, and can be written only if LOCK = 0 and STOP = 1. Refer to **Table 3**.

Table 3 Wait State Encoding

WAIT[1:0]	Wait States	Clocks Per Transfer
00	0	3
01	1	4
10	2	5
11	–1	2

The value of WAIT[1:0] is compatible with the lower two bits of the $\overline{\text{DSACK}}$ field in the SCIM chip-select option registers. An encoding of %11 in WAIT[1:0] corresponds to an encoding for fast termination.

FEE1TST, FEE2TST — Flash EEPROM Test Registers **$YFF802, $YFF822**

These registers are used for factory test only.

FEE1BAH, FEE2BAH — Flash EEPROM Base Address High Registers **$YFF804, $YFF824**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	ADDR 23	ADDR 22	ADDR 21	ADDR 20	ADDR 19	ADDR 18	ADDR 17	ADDR 16
RESET:															
0	0	0	0	0	0	0	0	SB	SB	SB	SB	SB	SB	SB	SB

FEE1BAL — Flash EEPROM Base Address Low Register **$YFF806**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR 15	ADDR 14	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESET:															
SB	SB	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FEE2BAL — Flash EEPROM Base Address Low Register **$YFF826**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The base address high registers (FEE1BAH, FEE2BAH) contain the 8 high-order bits of the array base address; the base address low registers (FEE1BAL, FEE2BAL) contain the active low-order bits of the array base address. During reset, both FEExBAH and FEExBAL take on default values programmed into associated shadow registers. After reset, if LOCK = 0 and STOP = 1, software can write to FEExBAH and FEExBAL to relocate the array.

FEE1CTL, FEE2CTL — Flash EEPROM Control Register **$YFF808, $YFF828**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	VFPE	ERAS	LAT	ENPE
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The flash EEPROM control registers (FEE1CTL, FEE2CTL) control programming and erasure of the arrays. FEExCTL is accessible in supervisor mode only.

VFPE — Verify Program/Erase

0 = Normal read cycles

1 = Invoke program verify circuit

The VFPE bit invokes a special program-verify circuit. During programming sequences (ERAS = 0), VFPE is used in conjunction with the LAT bit to determine when programming of a location is complete. If VFPE and LAT are both set, a bit-wise exclusive-OR of the latched data with the data in the location being programmed occurs when any valid FLASH location is read. If the location is completely programmed, a value of zero is read. Any other value indicates that the location is not fully programmed. When VFPE is cleared, normal reads of valid FLASH locations occur. The value of VFPE cannot be changed while ENPE = 1.

ERAS — Erase Control

0 = Flash EEPROM configured for programming

1 = Flash EEPROM configured for erasure

The ERAS bit configures the array for either programming or erasure. Setting ERAS causes all locations in the array and all control bits in the control block to be configured for erasure at the same time.

When the LAT bit is set, ERAS also determines whether a read returns the data in the addressed location (ERAS = 1) or the address itself (ERAS = 0). ERAS cannot be changed while ENPE = 1.

LAT — Latch Control

0 = Programming latches disabled

1 = Programming latches enabled

The LAT bit configures the EEPROM array for normal reads or for programming. When LAT is cleared, the FLASH module address and data buses are connected to the IMB address and data buses and the module is configured for normal reads. When LAT is set, module address and data buses are connected to parallel internal latches and the array is configured for programming or erasing.

Once LAT is set, the next write to a valid FLASH module address causes the programming circuitry to latch both address and data. Unless control register shadow bits are to be programmed, the write must be to an array address. The value of LAT cannot be changed while ENPE = 1.

ENPE — Enable Programming/Erase

0 = Disable program/erase voltage

1 = Apply program/erase voltage to flash EEPROM

Setting the ENPE bit applies the program/erase voltage to the array. ENPE can be set only after LAT has been set and a write to the data and address latches has occurred. ENPE remains cleared if these conditions are not met. While ENPE is set, the LAT, VFPE, and ERAS bits cannot be changed, and attempts to read an array location are ignored.

FEE1BS[3:0] — Flash EEPROM Bootstrap Words **$YFF810–$YFF816**
FEE2BS[3:0] — Flash EEPROM Bootstrap Words **$YFF830–$YFF836**

The flash EEPROM bootstrap words (FEE1BS[3:0], FEE2BS[3:0]) can be used as system bootstrap vectors. When BOOT = 0 in FEExMCR during reset, the flash module responds to program space accesses of IMB addresses $000000 to $000006 after reset. When BOOT = 1, the flash module responds only to normal array and register accesses. FEExBS[3:0] can be read at any time, but it can only be changed by programming the appropriate locations. **Table 4** shows bootstrap word addresses in program space.

Table 4 Bootstrap Words

Bootstrap Word	Corresponding Boot Address
FEE1BS0, FEE2BS0	$000000
FEE1BS1, FEE2BS1	$000002
FEE1BS2, FEE2BS2	$000004
FEE1BS3, FEE2BS3	$000006

1.5 Flash EEPROM Operation

The following paragraphs describe the operation of the flash EEPROM module during reset, system boot, normal operation, and while it is being programmed or erased.

1.5.1 Reset Operation

Reset initializes all registers to certain default values. Some of these reset values are programmable by the user and are contained in flash EEPROM shadow registers. If the state of the STOP shadow bit is zero, and the module's associated data bus pin is pulled high during reset (DATA15 for the 16 Kbyte array and DATA14 for the 48 Kbyte array), the STOP bit in the FEExMCR is cleared during reset. The array responds normally to the bootstrap address range and the flash EEPROM array base address. If the STOP shadow bit is one, or the module's associated data bus pin is pulled low during reset, the STOP bit in the FEExMCR is set. The flash EEPROM array is disabled until the STOP bit is cleared by software. It will not respond to the bootstrap address range, or the flash EEPROM array base address in FEExBAH and FEExBAL, allowing an external device to respond to the flash EEPROM array's address space or bootstrap information. Since the erased state of the shadow bits is one, erased flash EEPROM modules (which include the shadow registers in the control blocks) come out of reset in STOP mode.

1.5.2 Bootstrap Operation

After reset, the CPU begins bootstrap operation by fetching initial values for its internal registers from special bootstrap word addresses $000000 through $000006. If BOOT = 0 and STOP = 0 in FEExMCR, the flash EEPROM module is configured to recognize these addresses after a reset and provide this information from the FEExBS[3:0] bootstrap registers in the flash EEPROM control block. The information in these registers is programmed by the user.

1.5.3 Normal Operation

The flash EEPROM module allows a byte or aligned-word read in one bus cycle. Long-word reads require two bus cycles.

The module checks function codes to verify access privileges. All control block addresses must be in supervisor data space. Array accesses are defined by the state of ASPC[1:0] in FEExMCR. Access time is governed by the WAIT[1:0] field in FEExMCR.

Accesses to any address in the address block defined by FEExBAH and FEExBAL which does not fall within the array are ignored, allowing external devices to adjoin flash EEPROM arrays which do not entirely fill the address space specified by FEExBAH and FEExBAL.

1.5.4 Program/Erase Operation

An erased flash bit has a logic state of one. A bit must be programmed to change its state from one to zero. Erasing a bit returns it to a logic state of one. Programming and erasing the flash module requires a series of control register writes and a write to an array address. The same procedure is used to program control registers that contain flash shadow bits. Programming is restricted to a single byte or aligned word at a time. The entire array and the shadow register bits are erased at the same time.

When multiple flash modules share a single V_{FPE} pin, do not program or erase more than one flash module at a time. Normal accesses to modules that are not being programmed are not affected by programming or erasure of another flash module.

The following paragraphs give step-by-step procedures for programming and erasure of flash EEPROM arrays. Refer to **1.6 Electrical Characteristics** for information on programming and erasing specifications for the flash EEPROM module.

1.5.4.1 Programming

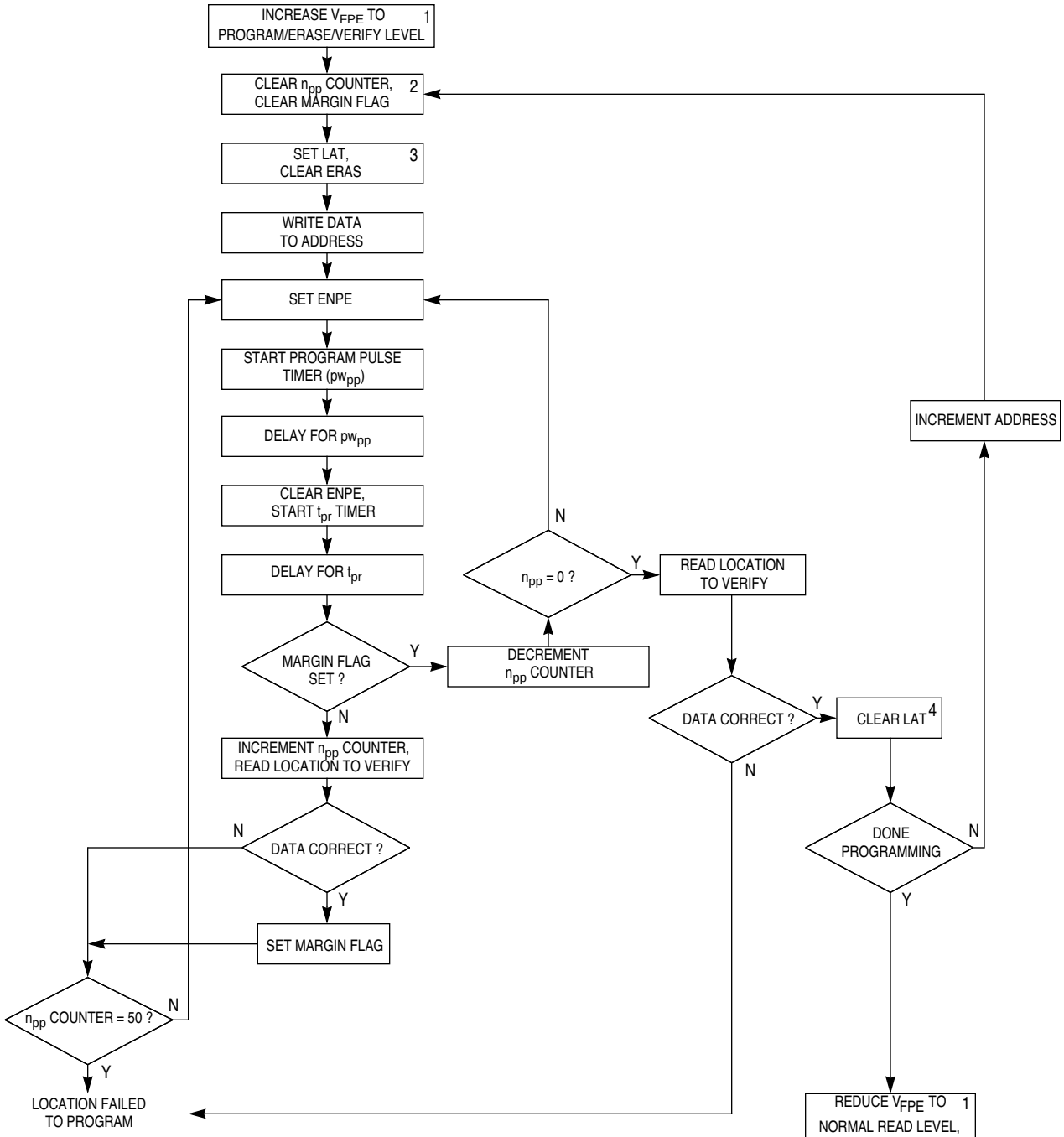
The following steps are used to program a flash EEPROM array. **Figure 1** is a flowchart of the programming operation.

1. Increase voltage applied to the V_{FPE} pin to program/erase/verify level.
2. Clear the ERAS bit and set the LAT bit in FEExCTL. This enables the programming address and data latches.
3. Write data to the address to be programmed. This latches the address to be programmed and the programming data.
4. Set the ENPE bit in FEExCTL. This starts the program pulse.
5. Delay the proper amount of time for one programming pulse to take place. Delay is specified by parameter pw_{pp}.
6. Clear the ENPE bit in FEExCTL. This stops the program pulse.
7. Delay while high voltage to array is turned off. Delay is specified by parameter t_{pr}.
8. Read the address to verify that it has been programmed.
9. If the location is not programmed, repeat steps 4 through 7 until the location is programmed, or until the specified maximum number of program pulses has been reached. Maximum number of pulses is specified by parameter n_{pp}.
10. If the location is programmed, repeat the same number of pulses as required to program the location. This provides 100% program margin.
11. Read the address to verify that it remains programmed.
12. Clear the LAT bit in FEExCTL. This disables the programming address and data latches.
13. If more locations are to be programmed, repeat steps 2 through 10.
14. Reduce voltage applied to the V_{FPE} pin to normal read level.

1.5.4.2 Erasure

The following steps are used to erase a flash EEPROM array. **Figure 2** is a flowchart of the erasure operation.

1. Increase voltage applied to the V_{FPE} pin to program/erase/verify level.
2. Set the ERAS bit and the LAT bit in FEExCTL. This configures the module for erasure.
3. Perform a write to any valid address in the control block or array. The data written does not matter.
4. Set the ENPE bit in FEExCTL. This applies the erase voltage to the array.
5. Delay the proper amount of time for one erase pulse. Delay is specified by parameter t_{epk}.
6. Clear the ENPE bit in FEExCTL. This turns off erase voltage to the array.
7. Delay while high voltage to array is turned off. Delay is specified by parameter t_{er}.
8. Read the entire array and control block to ensure all locations are erased.
9. If all locations are not erased, calculate a new value for t_{epk} ($t_{ei} \times$ pulse number) and repeat steps 3 through 10 until all locations erase, or the maximum number of pulses has been applied.
10. If all locations are erased, calculate the erase margin (e_m) and repeat steps 3 through 10 for the single margin pulse.
11. Clear the LAT and ERAS bits in FEExCTL. This allows normal access to the flash.
12. Reduce voltage applied to the V_{FPE} pin to normal read level.

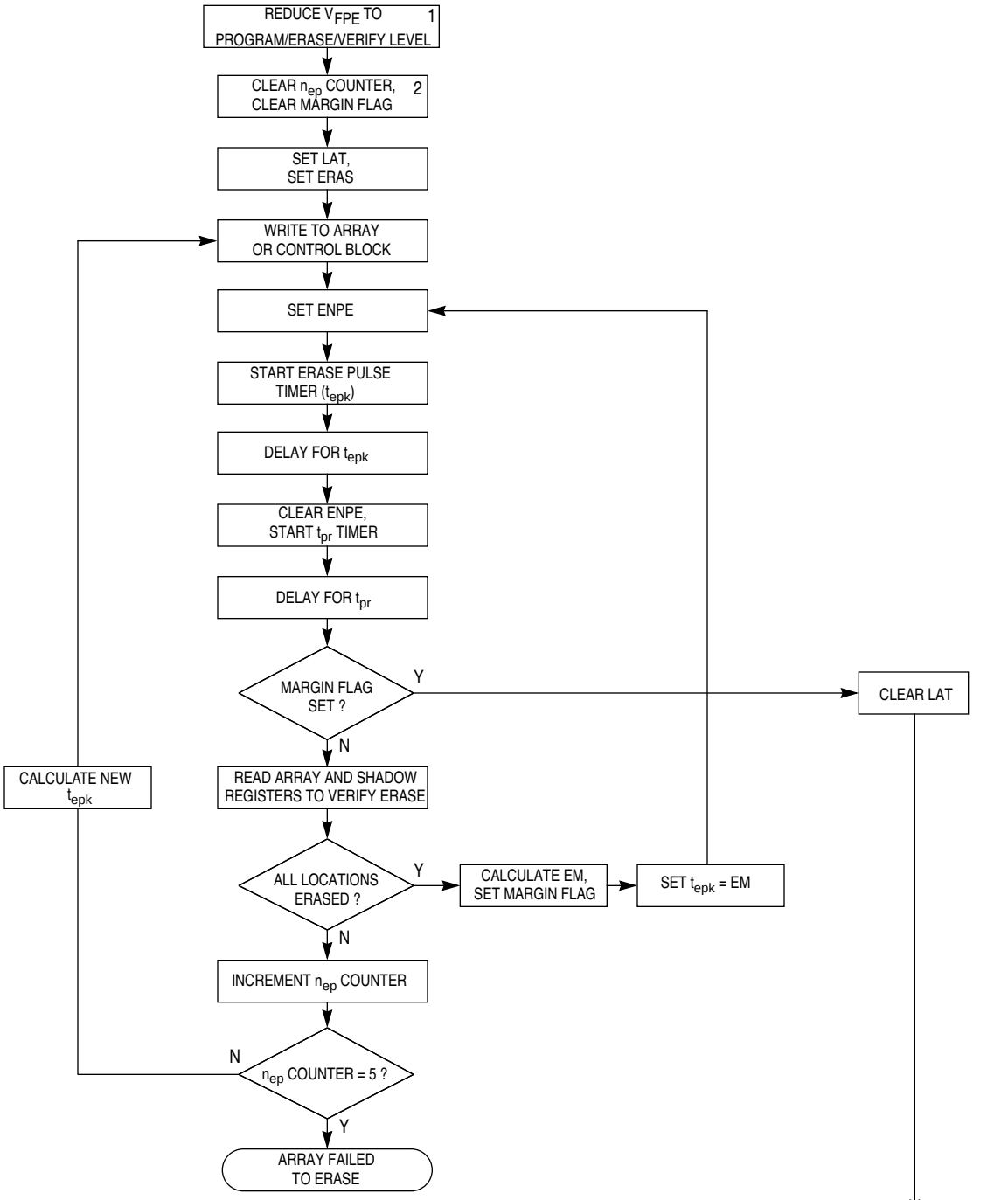


NOTES:

1. SEE ELECTRICAL CHARACTERISTICS FOR V_{FPE} PIN VOLTAGE SEQUENCING.
2. THE MARGIN FLAG IS A SOFTWARE-DEFINED FLAG THAT INDICATES WHETHER THE PROGRAM SEQUENCE IS GENERATING PROGRAM PULSES OR MARGIN PULSES.
3. TO SIMPLIFY THE PROGRAM OPERATION, THE V_{FPE} BIT IN FEExCTL CAN BE SET.
4. CLEAR V_{FPE} BIT ALSO IF ROUTINE USES THIS FUNCTION.

FEEPROM PGM FLOW1 TD

Figure 1 Programming Flow



NOTES:
1. SEE ELECTRICAL CHARACTERISTICS FOR V_{FPE} PIN VOLTAGE SEQUENCING.
2. THE MARGIN FLAG IS A SOFTWARE-DEFINED FLAG THAT INDICATES WHETHER THE PROGRAM SEQUENCE IS GENERATING ERASE PULSES OR MARGIN PULSES.

FEEPROM PGM FLOW2 TD

Figure 2 Erasure Flow

1.6 Electrical Characteristics

The following electrical specifications supersede those that appear in the *MC68F333 User's Manual* (MC68F333UM/AD). **Figures 3** and **4** show V_{FPE} pin voltage characteristics.

Table 5 Flash EEPROM Module Specifications

Num	Characteristic	Symbol	Min	Max	Unit
1	Program/Erase Supply Voltage[1] Read Operation Program/Erase/Verify Operation	V_{FPE}	$V_{DD} - 0.5$ 11.4	5.5 12.6	V
2	Program/Erase Supply Current[2] Read Operation Program/Erase/Verify Operation Verify (ENPE = 0) Program Byte (ENPE = 1) Program Word (ENPE = 1) Erase (ENPE = 1)	I_{FPE}	— — — — —	15 50 15 30 4	µA µA mA mA mA
3	Program Recovery Time	t_{pr}	—	3	cycles
4	Program Pulse Width	pw_{pp}	20	25	µA
5	Number of Program Pulses[3]	n_{pp}	—	50	—
6	Program Margin[4]	p_m	100	—	%
7	Number of Erase Pulses	n_{ep}	—	5	—
8	Erase Pulse Time	t_{epk}	—	$t_{ei} \times k$	ms
9	Amount to Increment t_{ep}	t_{ei}	90	110	ms
10	Erase Margin	e_m	—	$\sum_{k=1}^{n_{ep}} t_{ei} \times k$	ms
11	Erase Recovery Time	t_{er}	1	—	ms
12	Low-Power Stop Recovery Time[5]	t_{sb}	1	—	µA

1. V_{FPE} must not be raised to programming voltage while V_{DD} is below specified minimum value. V_{FPE} must not be reduced below minimum specified value while V_{DD} is applied.
2. Current parameters apply to each individual EEPROM module.
3. Without margin.
4. At 100% margin, the number of margin pulses required is the same as the number of pulses used to program the byte or word.
5. Parameter measured from end of write cycle that clears STOP bit in FEEMCR.

Table 6 Flash EEPROM Module Life

Num	Parameter	Symbol	Value	Unit
1	Program-Erase Endurance[1]	e_{pe}	100	cyc
2	Data Retention[2]	r_d	10	yr

1. Number of program-erase cycles (1 to 0, 0 to 1) per bit.
2. Parameter based on accelerated-life testing with standard test pattern.

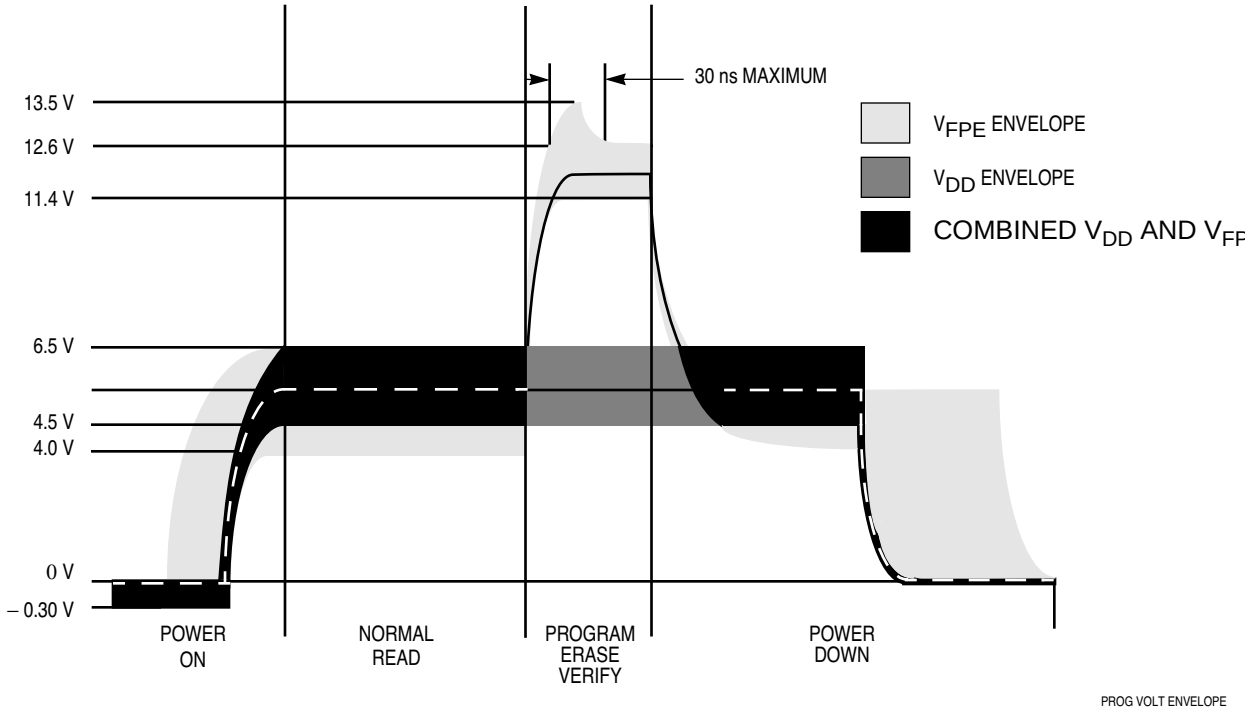


Figure 3 Programming Voltage Envelope

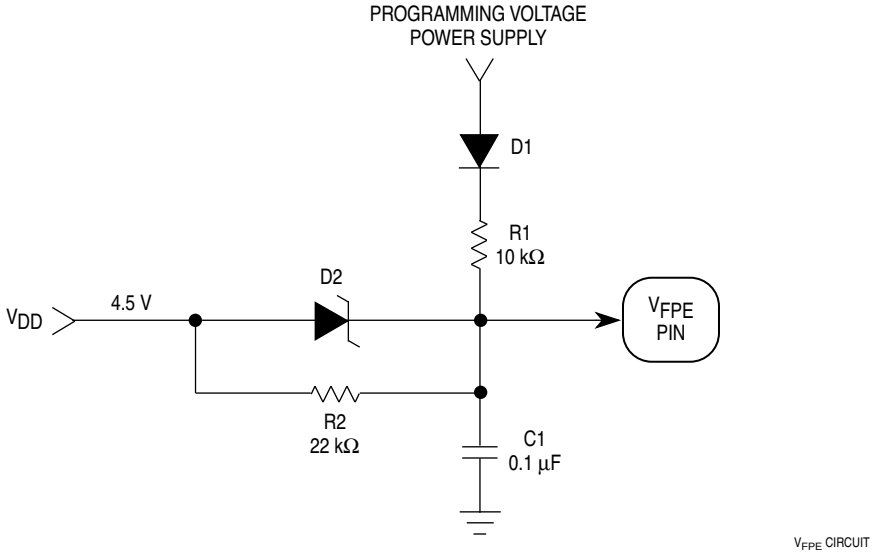


Figure 4 V_{FPE} Conditioning Circuit

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How to reach us:
USA/EUROPE: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447
MFAX: RMFAX0@email.sps.mot.com - TOUCHTONE (602) 244-6609
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HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298