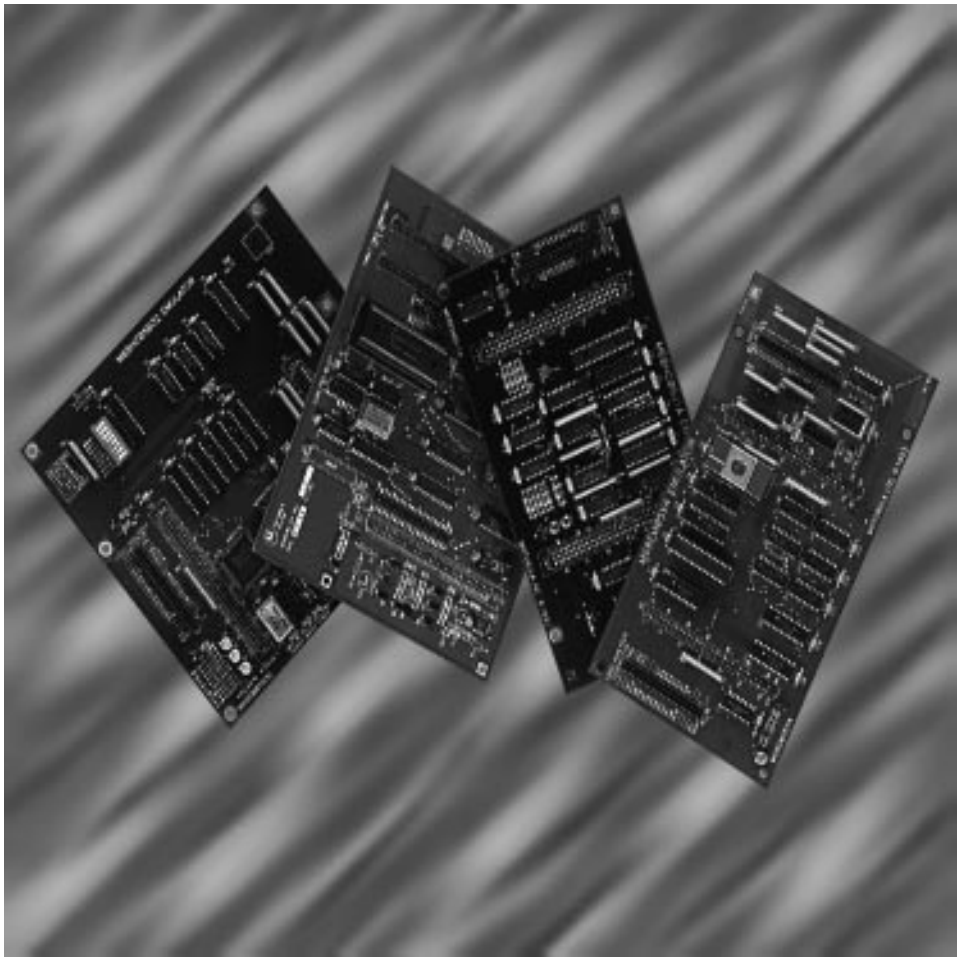
M68EML08LN56UM/D
Rev. 1.0

M68EML08LN56

EMULATION MODULE
USER'S MANUAL



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M68EML08LN56

Emulation Module
User's Manual

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Revision History

This table summarizes differences between this revision and the previous revision of this emulation module user's manual.

Previous Revision	0.0
Current Revision	Original Release
Date	09/96

Revision History

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General Description

Contents

Introduction

The M68EML08LN56 gives your Motorola development tool the ability to emulate target systems based on MC68HC708LN56 microcontroller units (MCUs). The M68EML08LN56 is designed to be a low-voltage emulator, operating in the 3.0 Vdc to 5.0 Vdc range at maximum rated frequencies per the general release specification.

By substituting a different emulation module (EM), the Motorola development tool can be enabled to emulate other MCUs. Refer to *Motorola's Development Tool Selector Guide*, order number SG173/D, for a complete list of available EMs.

This hardware user's manual explains connection, configuration, and operation information specific to the M68EML08LN56 emulation module. The module can be installed in two Motorola development systems. To configure your M68EML08LN56 for either an MMDS or an MMEVS, follow the instructions given in **Configuration and Operation** on page 21.

In this manual, MMDS0508 and MMEVS0508 are referred to as MMDS.

Emulation Components

Motorola’s complete emulation system consists of the emulation module described in this manual as well as other separately purchased options described in the following paragraphs.

The following items are included with the M68EML08LN56 emulation module:

- **An M68EML08LN56 emulation module (EM)** — The printed circuit board that enables system functionality for MC68HC708LN56 MCUs. The female connectors, on the bottom of the module, mate with male connectors on a development system platform board. The EM also has a connector for the target cable assembly.
- **Configuration software** — 3.5-inch diskette containing personality files for this module.

Separately purchased Motorola modular development tool options include:

- **An MMEVS0508 platform board (M68MMPFB0508)** — The MMEVS is an economical development tool that provides real-time in-circuit emulation. The unit's integrated design environment includes an editor, an assembler, a user interface, and a source-level debugging program.
- **An MMDS05 modular development system (MMDS05)** — The MMDS is a high-performance development tool that has all the capabilities of the MMEVS. In addition, it also has a bus state analyzer and real-time memory windows.
- **Flex cable target assembly** — Refer to **Target Cable Assemblies** on page 12 for more information.

User-supplied components include:

- **Host computer** — See the appropriate development tool user’s manual for minimum requirements.
- **Power supply** — +5 Vdc is required for the MMEVS.

Emulation Module Layout

Figure 1 on page 12 shows the layout of the M68EML08LN56. Jumper header W1 selects whether the V_{RH} voltage is supplied through the target cable assembly or from the variable resistor divider (VR1). Jumper header W2 lets you select the source of the MCU's oscillator.

Connector J1 connects to a logic analyzer. J2 provides a probe point for all input/output ports and other miscellaneous signals. Target connectors J3 and J4 provide the interface to a target system; this connector uses a separately purchased target cable assembly. When you install the M68EML08LN56 on the MMDS05, the target cable passes through the slit in the station module enclosure.

Variable resistor VR1 is used as a voltage divider to supply the V_{RH}, A/D reference voltage high to the MCU. VR2 controls a voltage regulator for supplying the MCU operating voltage between 3.0 V and 5.0 V. Test point header TP1 is the monitor point for MCU operating voltage adjustment. The MC68HC708LN56 MCU is at location XU2.

DIN connectors P1 and P2 connect the EM and a development system platform board. Connectors P3–P8 allow the user to connect a customer-supplied LCD target PCB. These connectors provide all frontplane and backplane signals.

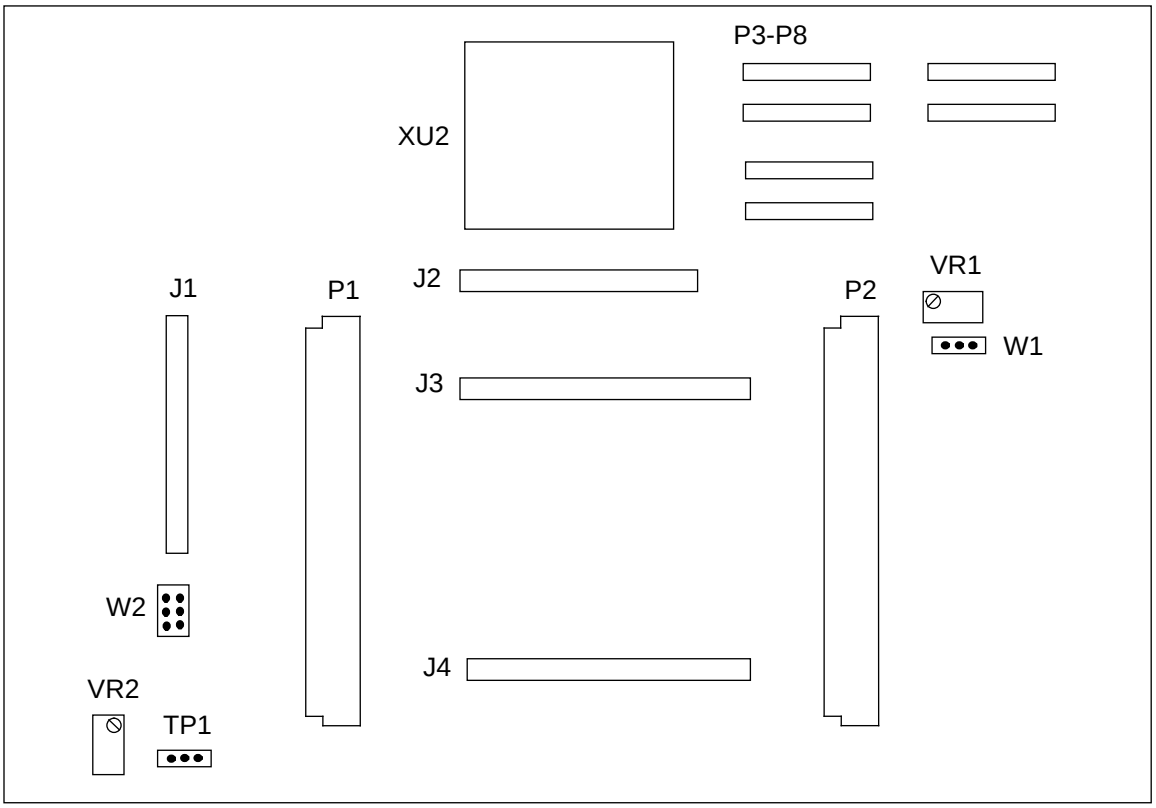


Figure 1. M68EML08LN56 Emulation Module

Target Cable Assemblies

To connect the M68EML08LN56 to a target system, you need a separately purchased target cable assembly. Cable assemblies are available for the 144-pin TQFP MCU package.

The target cable connects to the emulator via connectors J3 and J4 on the M68EML08LN56 emulation module. Pin assignments and signal descriptions for connectors J3 and J4 can be found in **Target Cable Connector Pin Assignments** on page 17.

Figure 2 on page 13 represents a target cable assembly. An assembly for a 144–pin TQFP package consists of a rigid flex cable with built-in target head adapter. One end of the rigid flex cable plugs onto M68EML08LN56 connectors J3 and J4 with orientation shown in **Figure**

2. The other end of the rigid flex cable contains the target head adapter which plugs into the user's target system.

The MCU package in the target system determines the target cable assembly components required:

- For the 144-pin TQFP package, use rigid flex cable M68CBL08LN56. A TQSOCKET with guides (M68TQS144SDG1) and a TQPACK (M68TQP144SD1) are included with the rigid flex cable assembly.

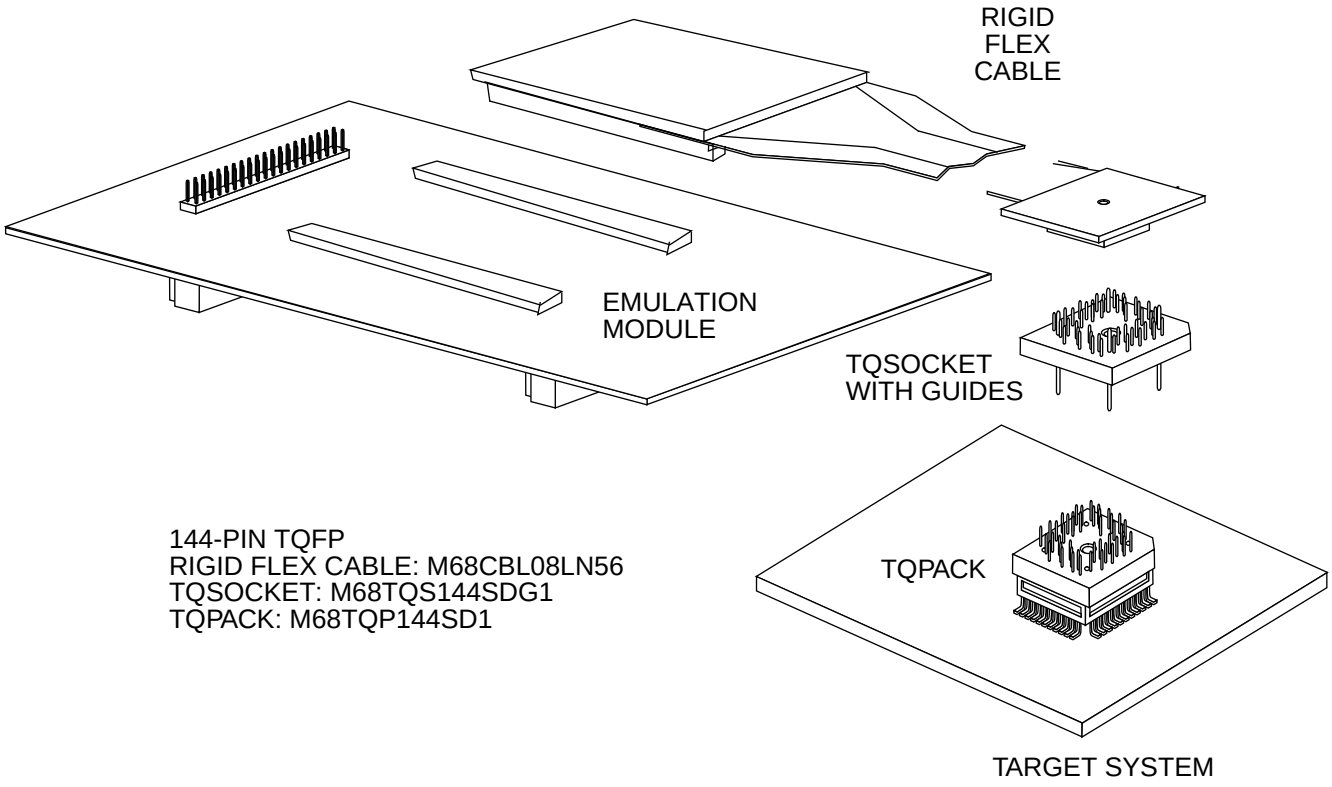


Figure 2. Target Cable Assembly

Connector Information

The connectors on the M68EML08LN56 module provide access to the user mode emulation signals (J2, J3, and J4) as well as select internal signals (J1). Connector J1 is used to connect to a logic analyzer. Connector J2 is used as a probe point for all MCU I/O signals. Connectors J3 and J4 are used for a cable interface to a user's target system.

Logic Analyzer Connector Pin Assignments

Figure 3 shows the pin assignments for logic analyzer connector J1. This connector provides the emulator easy access to many of the signals used internally. **Table 1** lists signal descriptions for this connector.

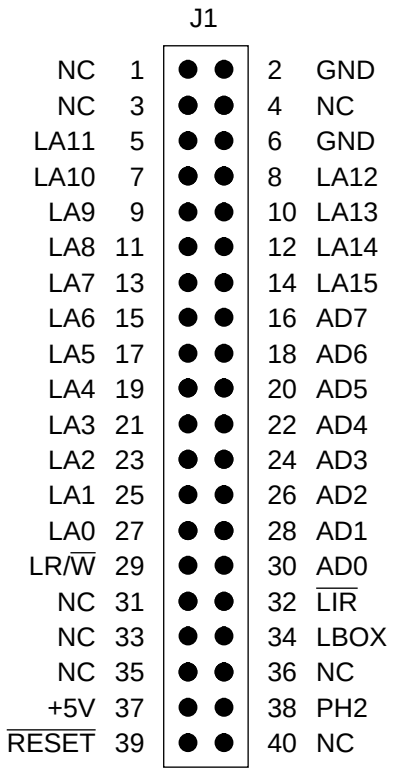


Figure 3. Connector J1 Pin Assignments

Table 1. Logic Analyzer Connector J1 Signal Descriptions

Pin	Mnemonic	Signal
1, 3, 4, 10, 12, 14, 31, 33, 35, 36, 40	NC	No Connection
2, 6	GND	GROUND
8, 10, 12, 14	LA12–LA15	LATCHED ADDRESS (Bits 12–15) — MCU latched address bus
5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27	LA11–LA0	LATCHED ADDRESSES (Bits 11–0) — MCU latched address bus
16, 18, 20, 22, 24, 26, 28, 30	AD7–AD0	DATA BUS (Bits 7–0) — MCU multiplexed I/O bus
29	LR/$\overline{W}$	LATCHED READ/WRITE — The MCU's write signal is latched and used on the emulator to control emulator memory accesses.
32	$\overline{LIR}$	LOAD INSTRUCTION REGISTER — Signal indicating an opcode fetch cycle is in process
34	$\overline{LBOX}$	LAST BOX — Active-high signal indicating last cycle of current instruction.
37	5V	+5 Vdc POWER — Connection to the system voltage V_{CC}
38	PH2	ANALYZER CLOCK — The latched addresses are valid on the latched address bus at the falling edge of PH2. Also, data is valid on the AD BUS at PH2 falling edge.
39	$\overline{RESET}$	RESET — Active-low signal; will be asserted during internally or externally caused resets

Figure 4 shows the pin assignments for connector J2. For pin descriptions, see signal name under **Table 2** on page 19 or **Table 3** on page 20.

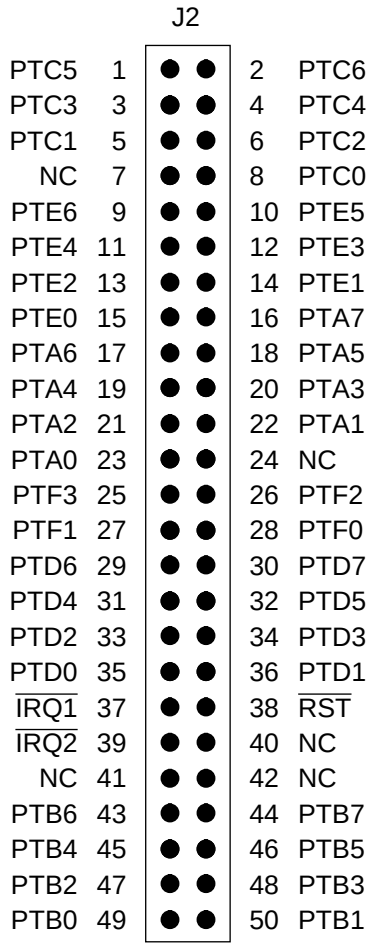


Figure 4. MCU I/O Probe Connector Pin Assignments

Target Cable Connector Pin Assignments

Figure 5 shows the pin assignments for connector J3. **Table 2** on page 19 lists signal descriptions for connector J3.

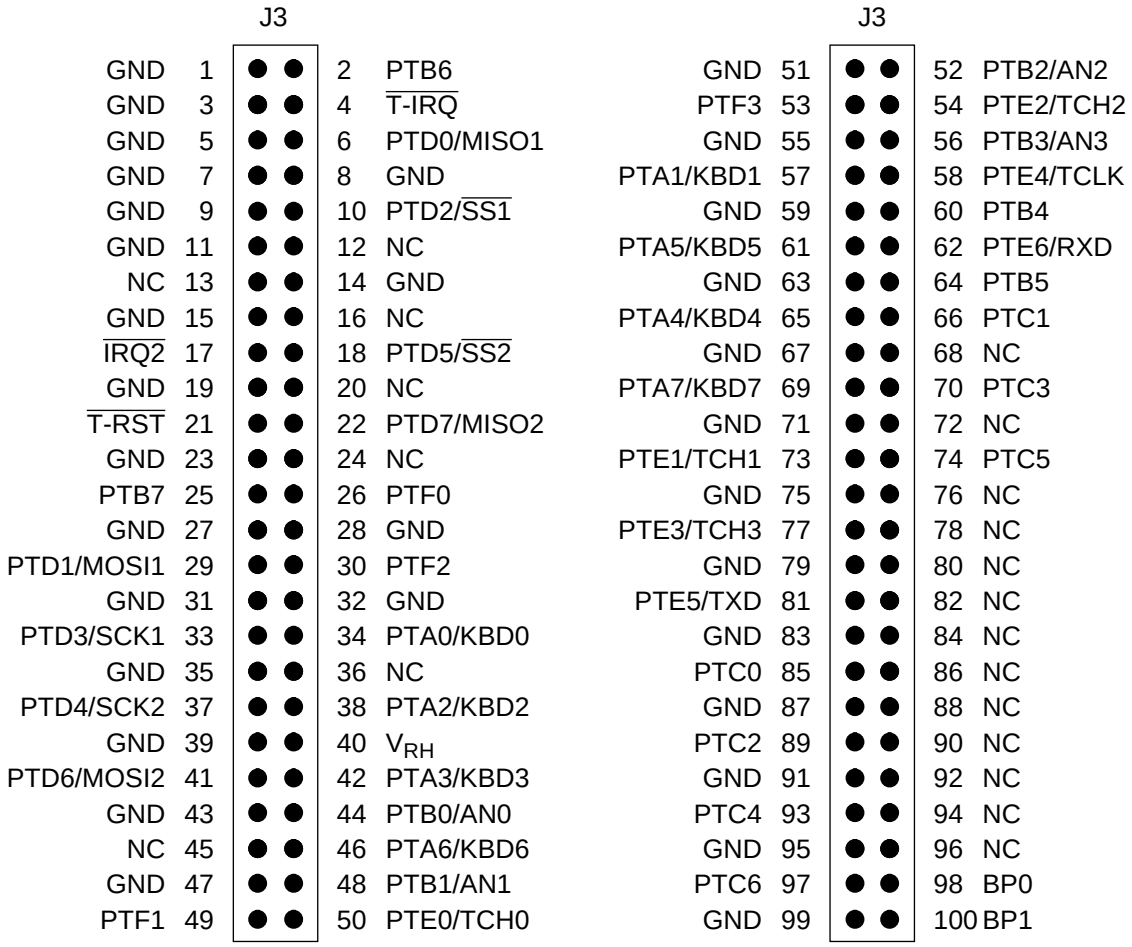


Figure 5. Target Connector Pin Assignments

Figure 6 shows the pin assignments for connector J3. **Table 3** on page 20 lists signal descriptions for connector J4.

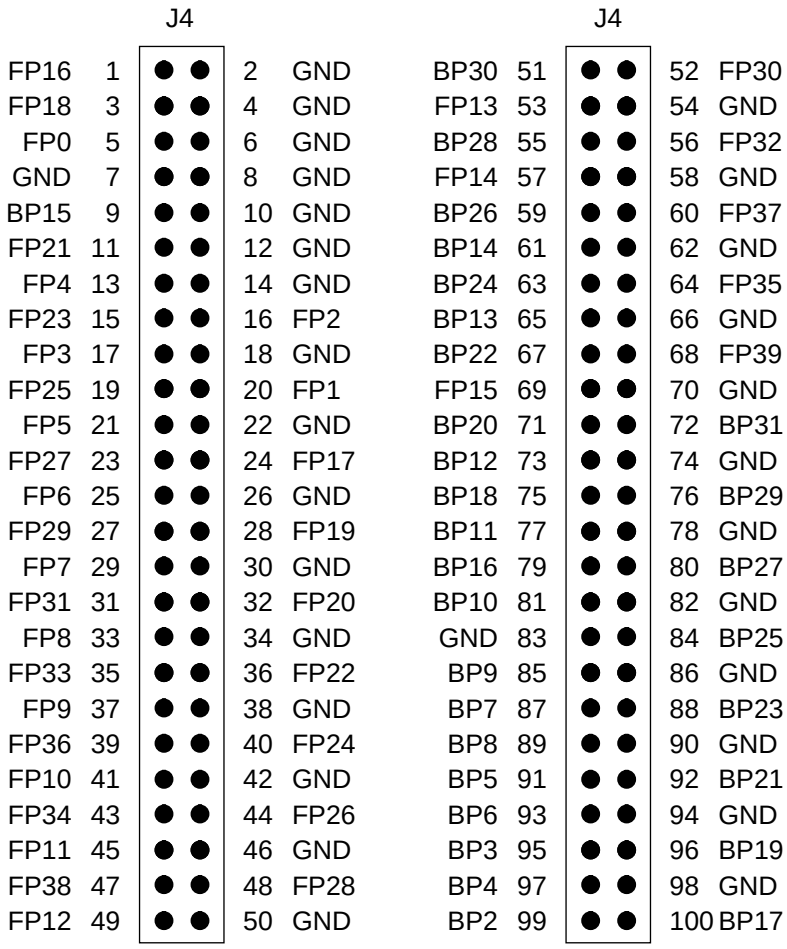


Figure 6. Target Connector Pin Assignments

Table 2. Connector J3 Signal Descriptions

Pin	Mnemonic	Signal
1, 3, 5, 7–9, 11, 14, 15, 19, 23, 27, 28, 31, 32, 35, 39, 43, 47, 51, 55, 59, 63, 67, 71, 75, 79, 83, 87, 91, 95, 99	GND	GROUND
2, 25, 44, 48, 52, 56, 60, 64	PTB6, PTB7 PTB0/AN0 PTB1/AN1 PTB2/AN2 PTB3/AN3 PTB4, PTB5	PORT B (Bits 0–7) – General-purpose I/O lines controlled by software via data direction and data registers Bits 0–3 are shared with the analog-to-digital converter module.
4	$\overline{\text{T-IRQ}}$	TARGET INTERRUPT REQUEST — Active-low input signal from the target that asynchronously applies an MCU interrupt
6, 10, 18, 22, 29, 33, 37, 41	PTD0/MISO1 PTD2/$\overline{\text{SS1}}$ PTD5/$\overline{\text{SS2}}$ PTD7/MISO2 PTD1/MOSI1 PTD3/SCK1 PTD4/SCK2 $\overline{\text{PTD6/MOSI2}}$	PORT D (Bits 0–7) – General-purpose I/O lines controlled by software via data direction and data registers Bits 0–7 are shared with the two SPI modules. NOTE: Silkscreen on Rev. 0 PCB is incorrect for PTD4 through PTD7. See **Figure 5** for correct pinout.
13, 20, 24, 36, 45, 68, 72, 76, 78, 80, 82, 84, 86, 88, 90, 92, 94, 96	NC	No Connection
17	$\overline{\text{IRQ2}}$	INTERRUPT REQUEST 2 – Active-low input signal from target that asynchronously applies an MCU interrupt 2
21	$\overline{\text{T–RESET}}$	Active-low bidirectional signal to/from the target system driven low to pull the MCU into reset
26, 30, 49, 53	PTF0, PTF2, PTF1, PTF3	PORT F (Bits 0–3) – General-purpose I/O lines controlled by software via data direction and data registers. These are high-current pins.
34, 38, 42, 46, 57, 61, 65, 69	PTA0/KBD0 PTA2/KBD2 PTA3/KBD3 PTA6/KBD6 PTA1/KBD1 PTA5/KBD5 PTA4/KBD4 PTA7/KBD7	PORT A (Bits 0–7) – General-purpose I/O lines controlled by software via data direction and data registers Bits 0–7 are shared with the keyboard input module.

Table 2. Connector J3 Signal Descriptions

Pin	Mnemonic	Signal
66, 70, 74, 85, 89, 93, 97	PTC1, PTC3, PTC5, PTC0, PTC2, PTC4, PTC6	PORT 6 (Bits 0–6) – General-purpose I/O lines controlled by software via data direction and data registers
50, 54, 58, 62, 73, 77, 81	PTE0/TCH0 PTE2/TCH2 PTE4/TCLK PTE6/RXD PTE1/TCH1 PTE3/TCH3 PTE5/TXD	PORT E (Bits 0–6) – General-purpose I/O lines controlled by software via data direction and data registers. Bits 0–4 are shared with the timer module. Bits 5 and 6 are shared with the SCI module. NOTE: Silkscreen on Rev. 0 PCB is incorrect for PTE5 and PTE6 on Rev. 0 PCB. See **Figure 5** for correct pinout.
98, 100	BP0, BP1	LCD Backplanes
12	OSC1	No Connection
16	OSC2	No Connection
40	V_{RH}	Voltage reference high for A/D converter

Table 3. Connector J4 Signal Descriptions

Pin	Mnemonic	Signal
1, 3, 5, 11, 13, 15–17, 19–21, 23–25, 27–29, 31–33, 35–37, 39–41, 43–45, 47–49, 52, 53, 56, 57, 60, 64, 68, 69	FP16, 18, 0, 21, 4, 23, 2, 3, 25, 1, 5, 27, 17, 6, 29, 19, 7, 31, 20, 8, 33, 22, 9, 36, 24, 10, 34, 26, 11, 38, 28, 12, 30, 13, 32, 14, 37, 35, 39, 15	LCD Frontplanes
2, 4, 6 – 8, 10, 12, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62, 66, 70, 74, 78, 82, 83, 86, 90, 94, 98	GND	GROUND
9, 51, 55, 59, 61, 63, 65, 67, 71–73, 75–77, 79–81, 84, 85, 87–89, 91–93, 95–97, 99, 100	BP15, 30, 28, 26, 14, 24, 13, 22, 20, 31, 12, 18, 29, 11, 16, 27, 10, 25, 9, 7, 23, 8, 5, 21, 6, 3, 19, 4, 2, 17	LCD Backplanes

Configuration and Operation

Contents

Introduction

The following paragraphs explain how to configure and use your M68EML08LN56 as part of an MMDS or MMEVS system. For other parts of system installation and configuration, see either the *MMDS05 Operations Manual* (MMDS0508OM/D) or *MMEVS0508 Operations Manual* (MMEVS0508OM/D).

The topics covered in this chapter are:

- **Setting M68EML08LN56 Jumper Headers** on page 23 explains how to set the M68EML08LN56 jumper headers.
- **Remaining System Installation** on page 25 covers the final steps to system installation.
- **Setting Emulation Voltage** on page 26 explains how to adjust the MC68HC708LN56 MCU operating voltage.
- **Setting the On-Board VRH Voltage** on page 27 explains how to adjust the variable voltage for the A/D using the on-board supply.
- **Personality File Usage** on page 27 discusses the personality file used on the M68EML08LN56 board.
- **MC68HC(7)08LN56 Emulation** on page 28 explains special considerations for emulating with this module.

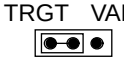
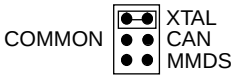
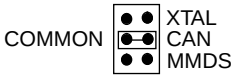
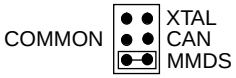
NOTE: *You can configure an M68EML08LN56 already installed in the system platform board. To do so, remove system power and then follow the guidance of this chapter.*

CAUTION: *Be sure to switch off power before you reconfigure an installed EM. Reconfiguring EM jumper headers with the power on can damage emulation circuits.*

Setting M68EML08LN56 Jumper Headers

Your M68EML08LN56 has two jumper headers – W1 and W2. **Table 4** provides a quick reference for configuration options. Refer to the paragraphs that follow for a more detailed explanation.

Table 4. Jumper Headers for MMDS/MMEVS

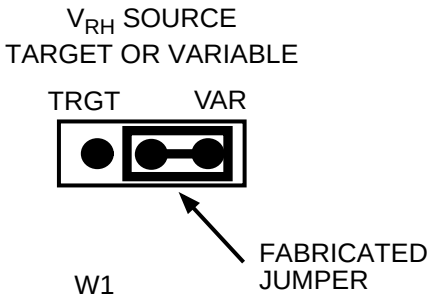
Jumper/ Switch	Position	Description	Factory Setting
V_{RH} Select- W1		Selects a variable voltage divider, controlled by VR1, as the source of the analog-to-digital voltage reference high supply.	X
		Selects a user-supplied voltage, through the target cable, as the source of the analog-to-digital voltage reference high supply.	
Clock Source Select- W2		Selects a user-supplied crystal oscillator circuit as the MCU clock source.	
		Selects the 32.768-kHz canned oscillator located on the EM board at XY2.	X
		Selects the clock originating from the development system platform board. The frequency is controlled by the OSC command and is 4 MHz on power-up.	

V_{RH} Select Header – W1

Jumper header W1 controls the source of the analog-to-digital voltage reference high supply. The diagram below shows the factory configuration wherein the fabricated jumper in the VAR position enables the V_{RH} voltage source to be supplied by the variable resistor VR1.

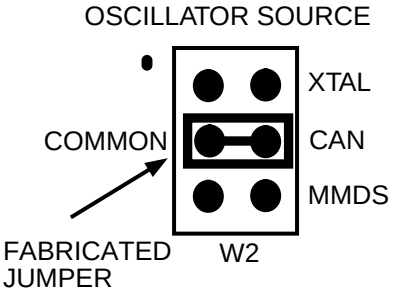
NOTE: *The variable resistor VR1 uses the emulation voltage as its supply. Therefore, adjust the MCU emulation first (see* ***Setting the On-Board VRH Voltage*** on page 27*) first, then set the V_{RH} voltage.*

For a target supplied source, the user should configure the jumper to the TRGT position.



Clock Source Select Header – W2

Jumper header W2 determines the clock-signal source. The diagram below illustrates the jumper header where the pin marked COMMON is always connected to one of the three clock source pins via the fabricated jumper. The default configuration, between CAN and COMMON, selects the 32.768-kHz canned oscillator clock source at board location XY2.



There are two other possible clock sources. To use the one originating from the development system platform, reposition the W2 jumper header

between the MMDS05 and COMMON pins. Then use the system's OSC command to select a frequency.

For a user-supplied crystal source, the user must install components Y1, R13, R14, C37, and C38, and reposition the W2 jumper header between the XTAL and COMMON pins. Consult the schematics sheet 4 for actual component connection.

Remaining System Installation

When headers W1 and W2 have been configured, the M68EML08LN56 configuration is complete.

- Ensure that the power to the development tool is off.
- If installing the M68EML08LN56 in an MMDS station module, remove the panel from the station module top.
- Fit together EM connectors P1 and P2 on the bottom of the board and platform board DIN connectors. Snap the corners of the EM onto the plastic standoffs.
- Connect the target cable, if appropriate.
- If installing in an MMDS, replace the panel.

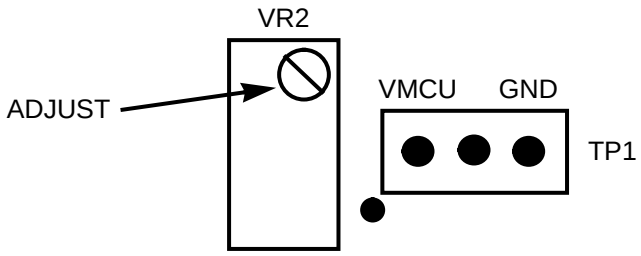
At this point, you are ready to make remaining cable connections, as necessary, and restore power.

For instructions, consult either the *MMEVS05/MMEVS08 Operations Manual* (MMEVS0508OM/D) or the *MMDS05 Operations Manual* (MMDS05OM/D).

Setting Emulation Voltage

The M68EML08LN56 module has an on-board voltage regulator that can be adjusted to provide low-voltage emulation in the 3.0 V to 5.0 V range. The adjustment for that variable voltage is variable resistor VR2. Test point TP1 is used for connection to a voltmeter during voltage adjustment.

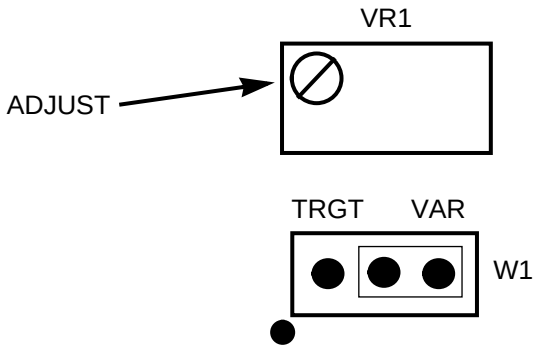
To adjust the MCU operating voltage, first ensure that no target cable is connected to target cable connectors J3 and J4. Then connect a voltmeter across the GND and VMCU pins of test point header TP1 and adjust variable resistor VR2 to the desired voltage level. Make sure that the target system operating voltage is at the newly adjusted level before connecting target signals through the J3 and J4 connectors.



Setting the On-Board V_{RH} Voltage

The M68EML08LN56 module has an on-board variable supply for the analog-to-digital converter. The adjustment for the voltage divider is done by adjusting the variable resistor VR1. The supply for the resistor is the emulation MCU voltage. The valid voltage for the V_{RH} is from VMCU to 1.5 V. Pin 2 (center pin) of jumper W1 can be used as a connection to a voltmeter during voltage adjustment.

NOTE: *The variable resistor VR1 uses the emulation voltage as its supply. Therefore, adjust the MCU emulation voltage first, then set the V_{RH} voltage.*



Personality File Usage

Your development system uses a specific personality file for the MCU type being emulated. For example, to emulate an MC68HC(7)08LN56 MCU, the system uses the personality file 0041BVxx.MEM. Debugger software loads this personality file upon power-up.

NOTE: *Note that personality file names follow the pattern 00ZZZVxx.MEM, where ZZZ is the EM identifier or MCU name and xx is the version of the file.*

MC68HC(7)08LN56 Emulation

NOTE: *Be aware that if the computer operating properly disable bit (COPD) option in the configuration register $1F is enabled out of reset, your code must clear the COP watchdog timer counter to avoid a COP reset. The counter is cleared by writing any value at location $FFFF. This should be the first check when code is not operating as expected.*

The MC68HC08LN56 MCU is emulated on the M68EML08LN56 emulation module. The resident MCU (socket XU2) can be either a ROM device, an MC68HC08LN56, or an EPROM device, an MC68HC708LN56. Because emulation flexibility is optimum when using the EPROM device, the M68EML08LN56 is shipped with an MC68HC708LN56 as the resident MCU.

There are no known differences between the performance of an MC68HC(7)08LN56 MCU run in single-chip operation versus the way certain features perform during emulation.

Schematics

Contents

M68EML08LN56 Schematics

Refer to the following pages for the 10 sheets of schematics for the M68EML08LN56 emulation module.

Schematics

M68EML08LN56 Schematics (Sheet 1 of 10)

NOTES, UNLESS OTHERWISE SPECIFIED

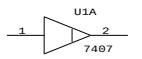
1. VCC PIN LOCATIONS :

   VCC IS APPLIED TO PIN 8 OF ALL 8-PIN IC's, PIN 14 OF ALL 14-PIN IC's, PIN 16 OF ALL 16-PIN IC's, PIN 20 OF ALL 20-PIN IC's, ETC.

2. GROUND PIN LOCATIONS :

   GROUND IS APPLIED TO PIN 4 OF ALL 8-PIN IC's, PIN 7 OF ALL 14-PIN IC's, PIN 8 OF ALL 16-PIN IC's, PIN 10 OF ALL 20-PIN IC's, ETC.

3. DEVICE TYPE, PIN NUMBERS, AND REFERENCE DESIGNATOR OF GATES ARE SHOWN AS FOLLOWS :



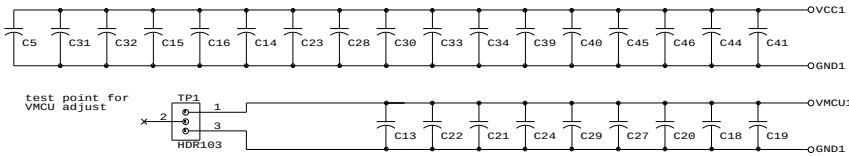
7407 = DEVICE TYPE
1 AND 2 = PIN NUMBERS
U1A = REFERENCE DESIGNATORS

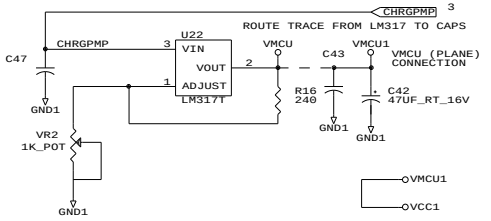
4. RESISTANCE VALUES ARE IN OHMS.
5. RESISTORS ARE 1/4 WATT, 5%.
6. CAPACITANCE VALUES ARE IN MICROFARADS.

M68EML08LN56 EMULATION MODULE

REVISIONS		
REV	DESCRIPTION	DATE
2	required changes to make PCB rev 0 functional	5/12/96
3	target connector had 4 wrong connections on PORT D, rev 3 corrects this	6/7/96

All caps are 0.1 uF @ 50 V



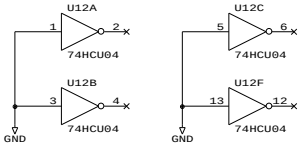


VCC1 = 5V (plance)
VMCU1 = Vreg (plane)

NOTE: make isolated plane for VMCU1 and VCC1 on PCB layout!

GND1 = GROUND (plane)

Spare Gates



ORCAD IV FLAT FILES

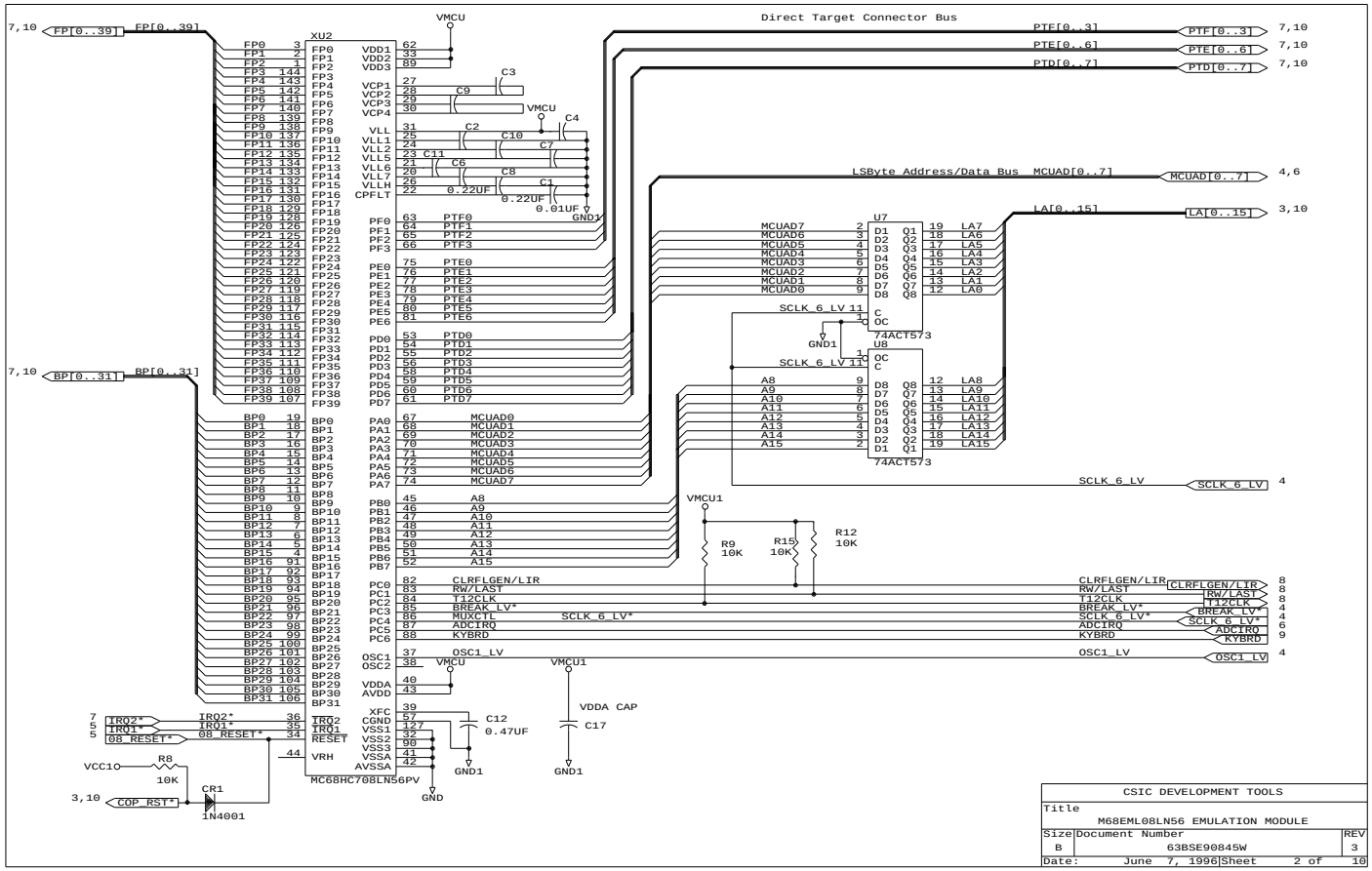
LINK
LN56R3S2.SCH
LN56R3S3.SCH
LN56R3S4.SCH
LN56R3S5.SCH
LN56R3S6.SCH
LN56R3S7.SCH
LN56R3S8.SCH
LN56R3S9.SCH
LN56R3SA.SCH

COMPUTER GENERATED DRAWING : DO NOT REVISE MANUALLY

CSIC DEVELOPMENT TOOLS		
Title	M68EML08LN56 EMULATION MODULE	
Size: B	Document Number: 63BSE90845W	REV: 3
Date: June 7, 1996	Sheet 1 of 10	

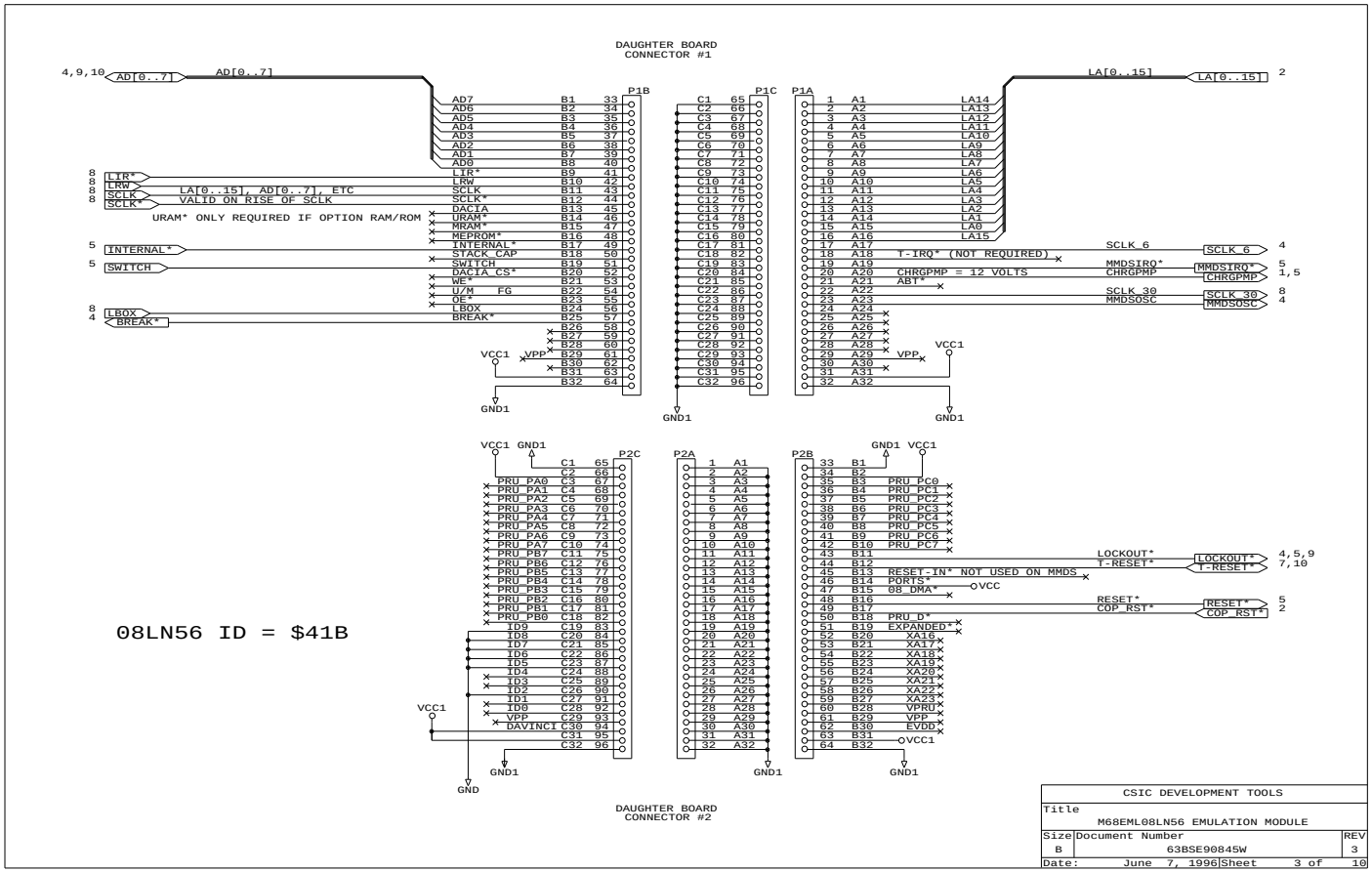
Schematics

M68EML08LN56 Schematics (Sheet 2 of 10)



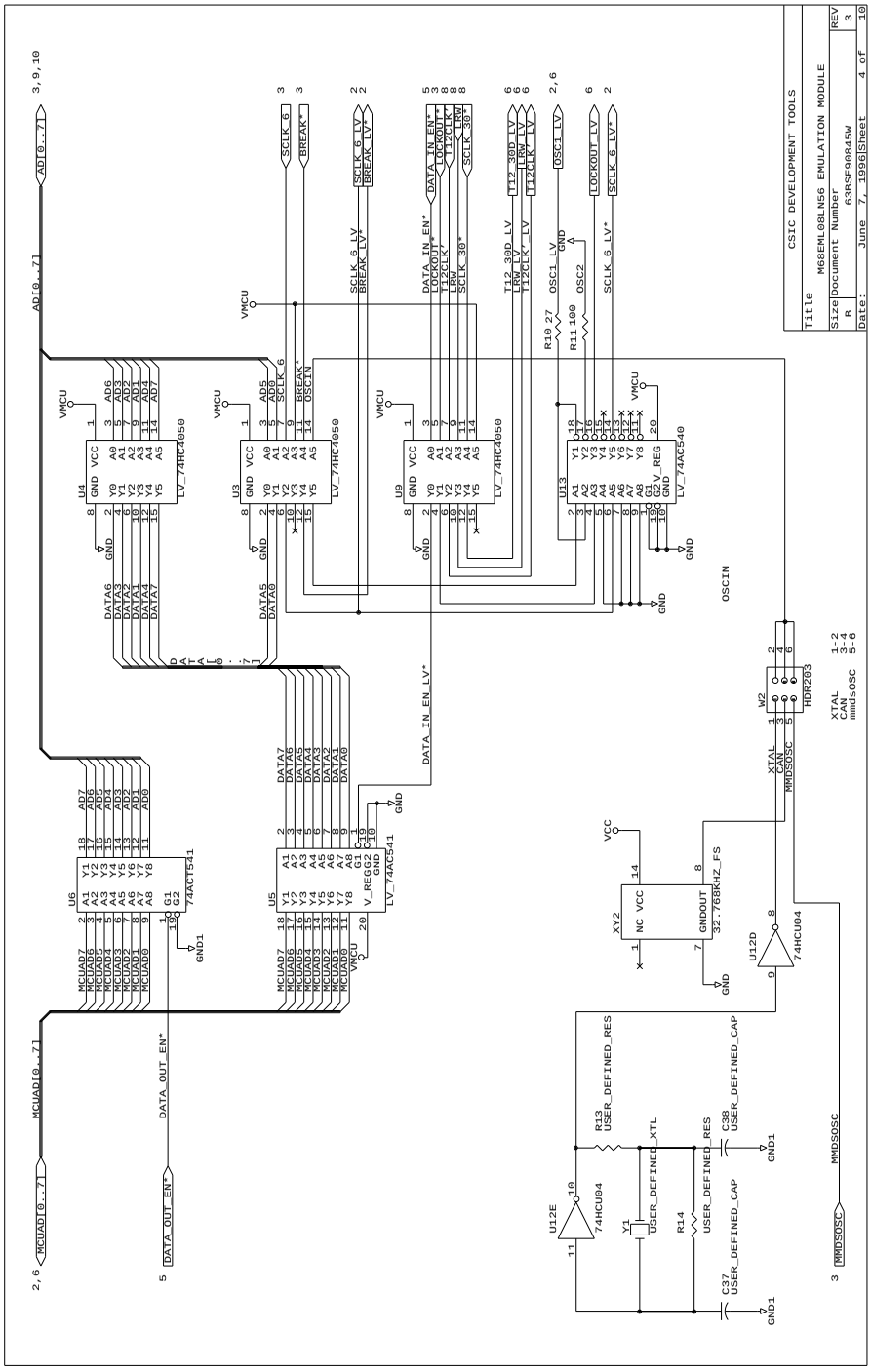
Schematics

M68EML08LN56 Schematics (Sheet 3 of 10)



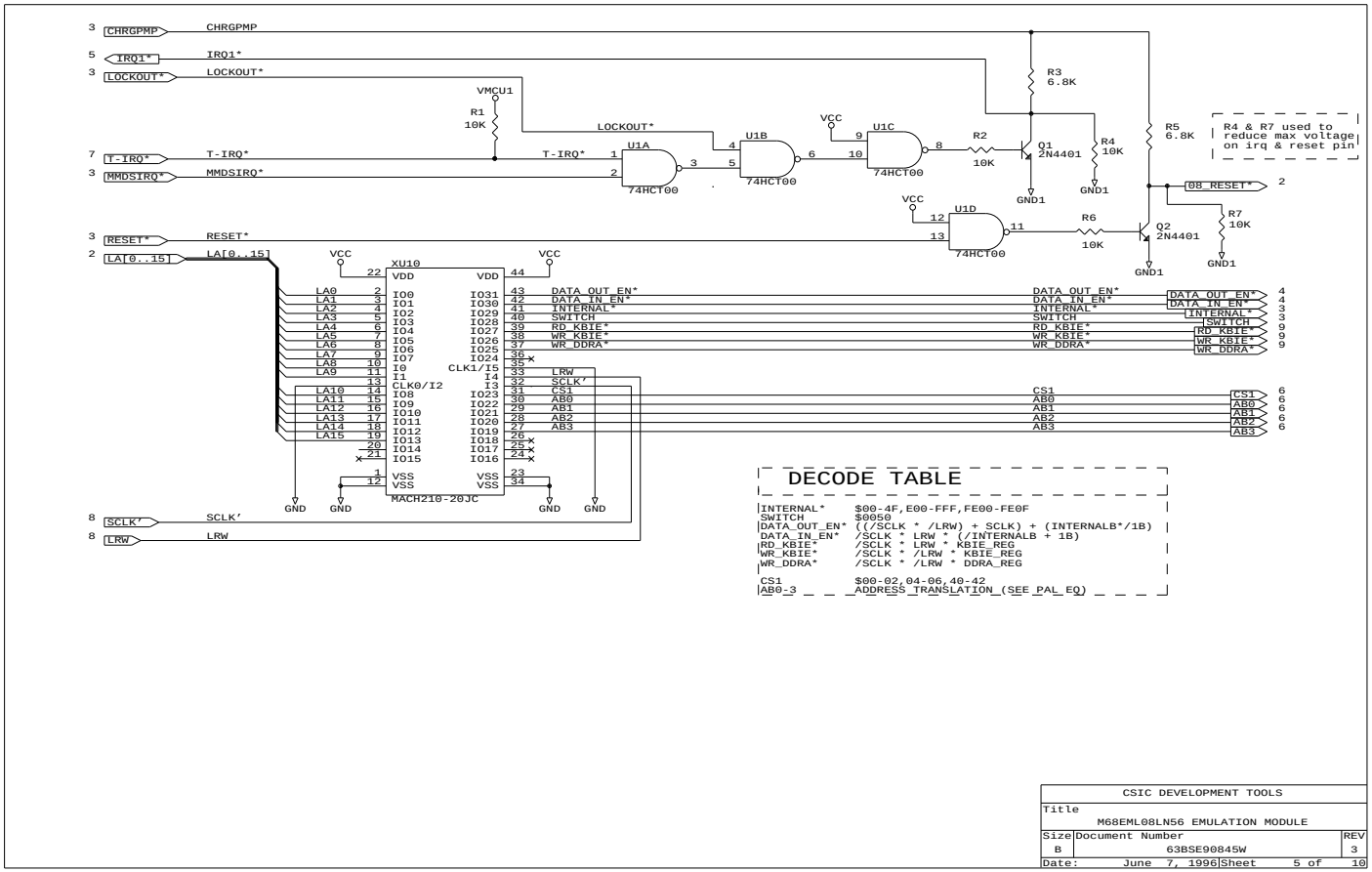
Schematics

M68EML08LN56 Schematics (Sheet 4 of 10)



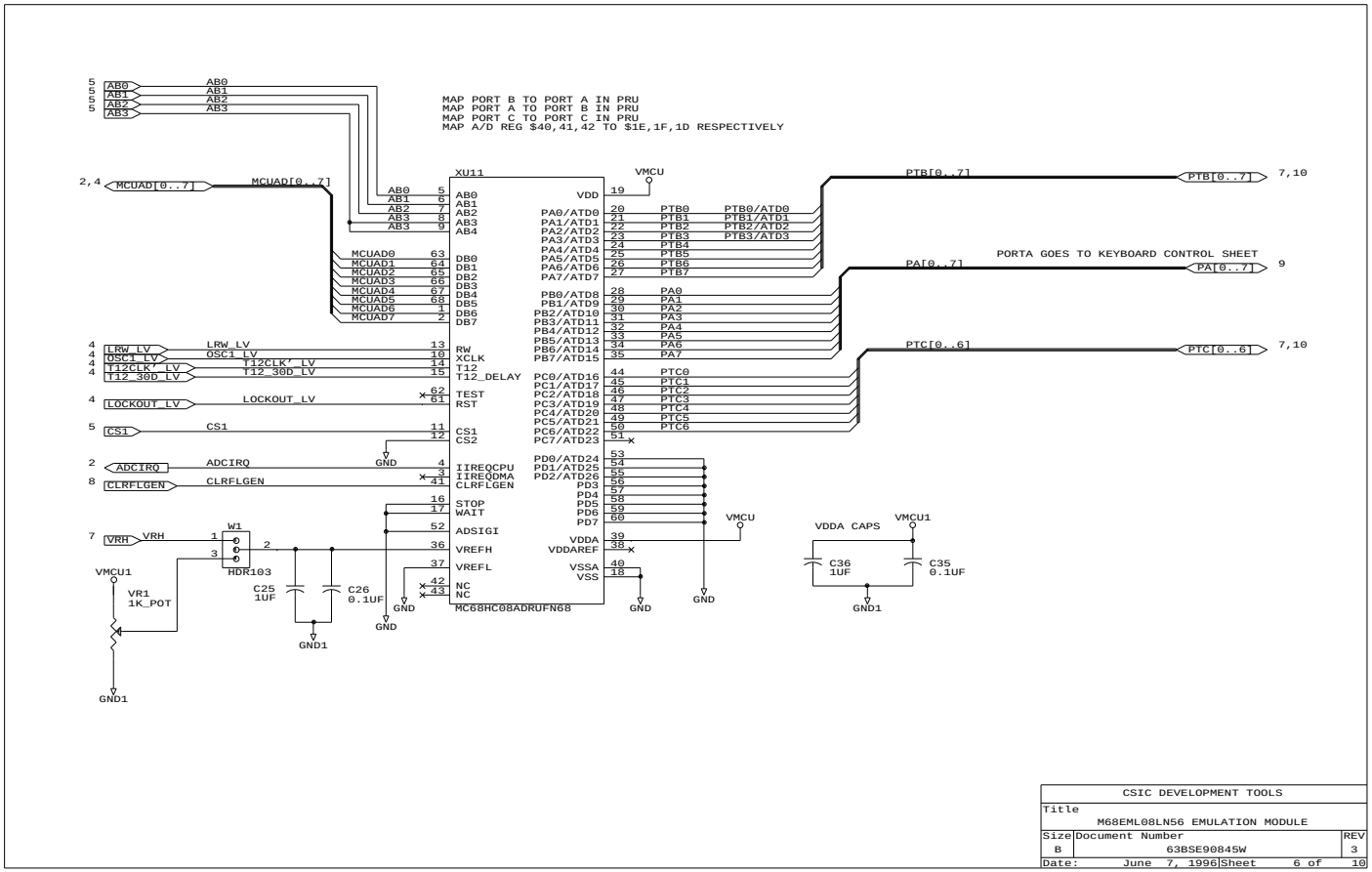
Schematics

M68EML08LN56 Schematics (Sheet 5 of 10)



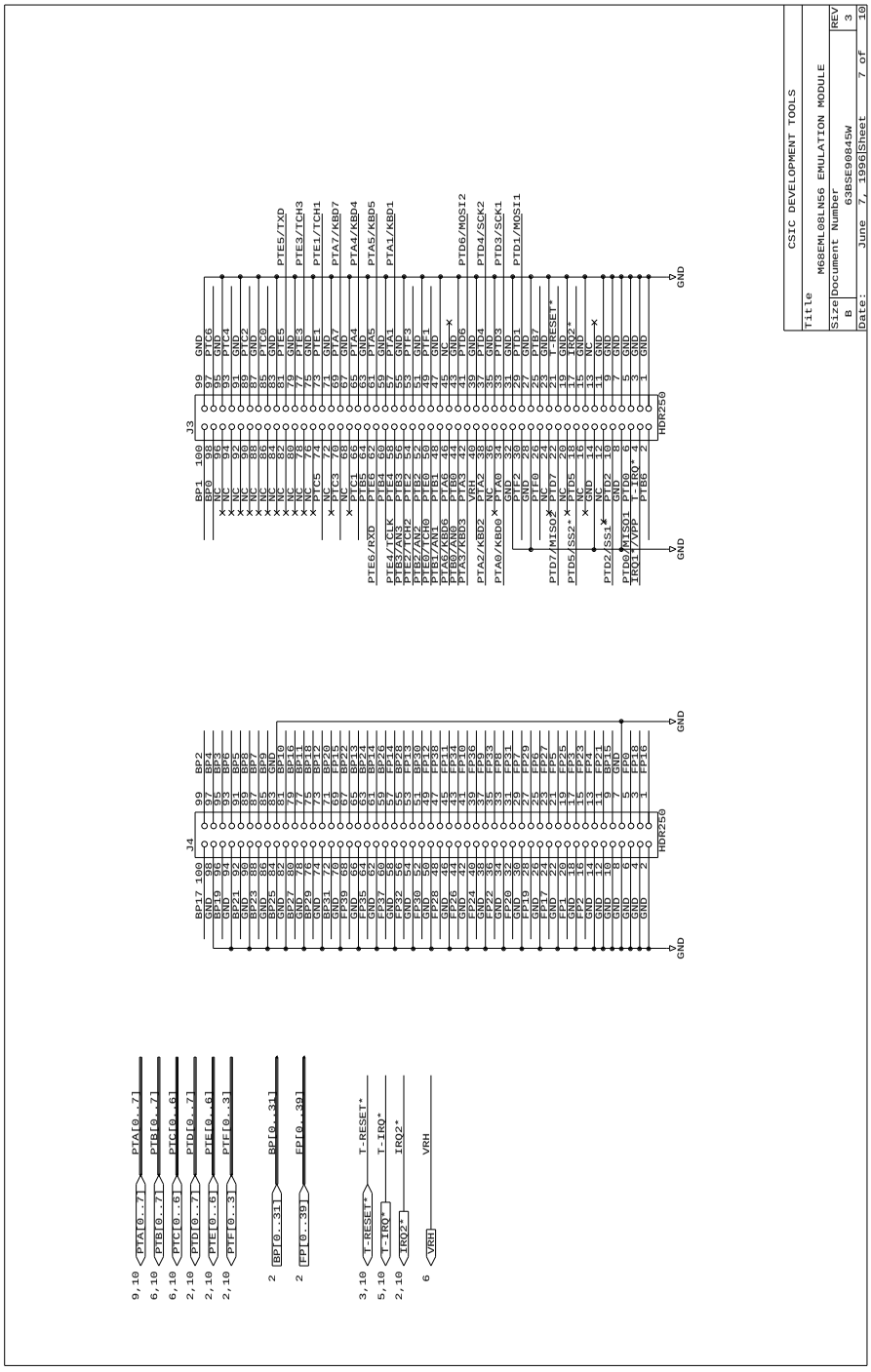
Schematics

M68EML08LN56 Schematics (Sheet 6 of 10)



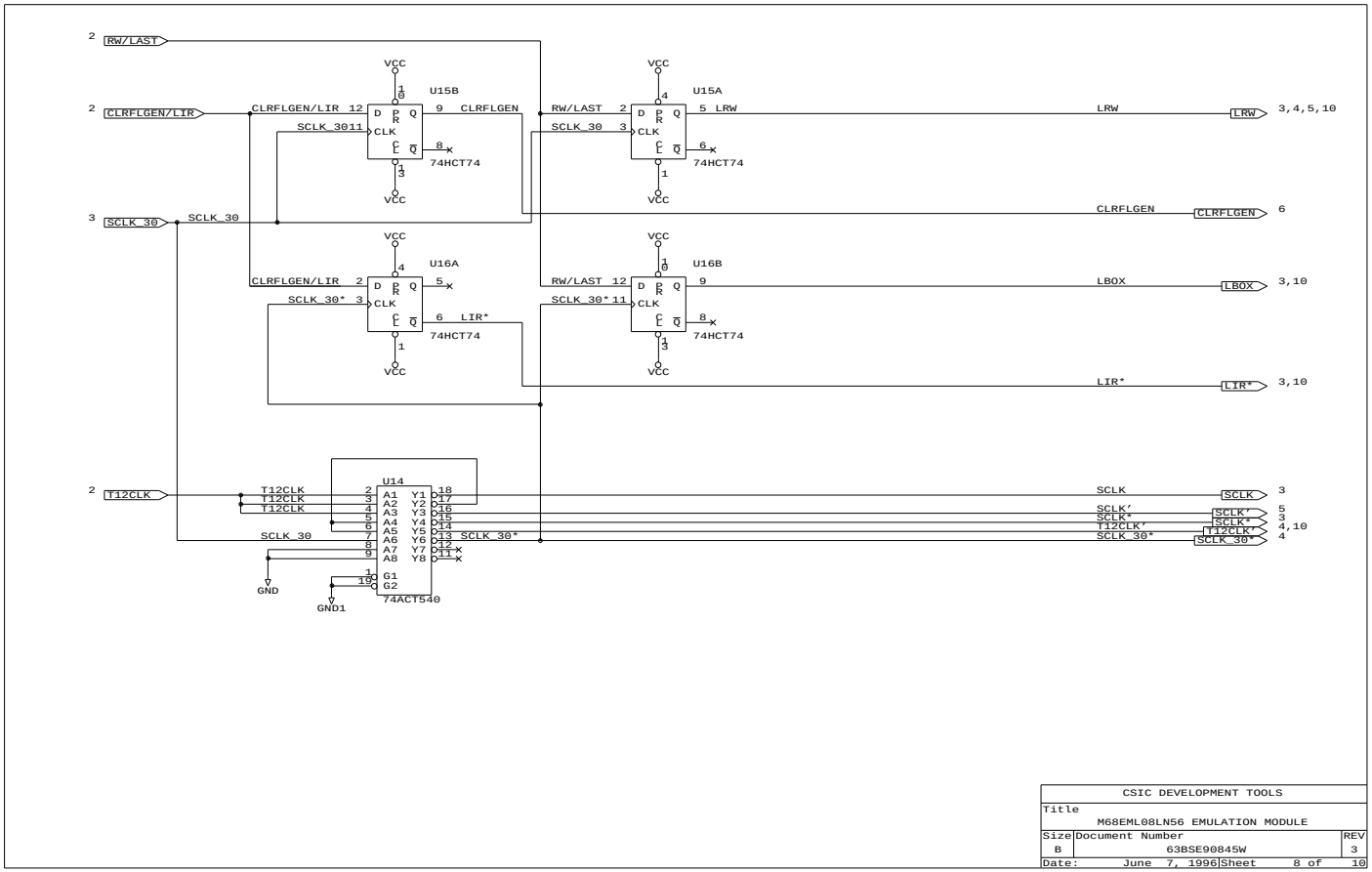
Schematics

M68EML08LN56 Schematics (Sheet 7 of 10)



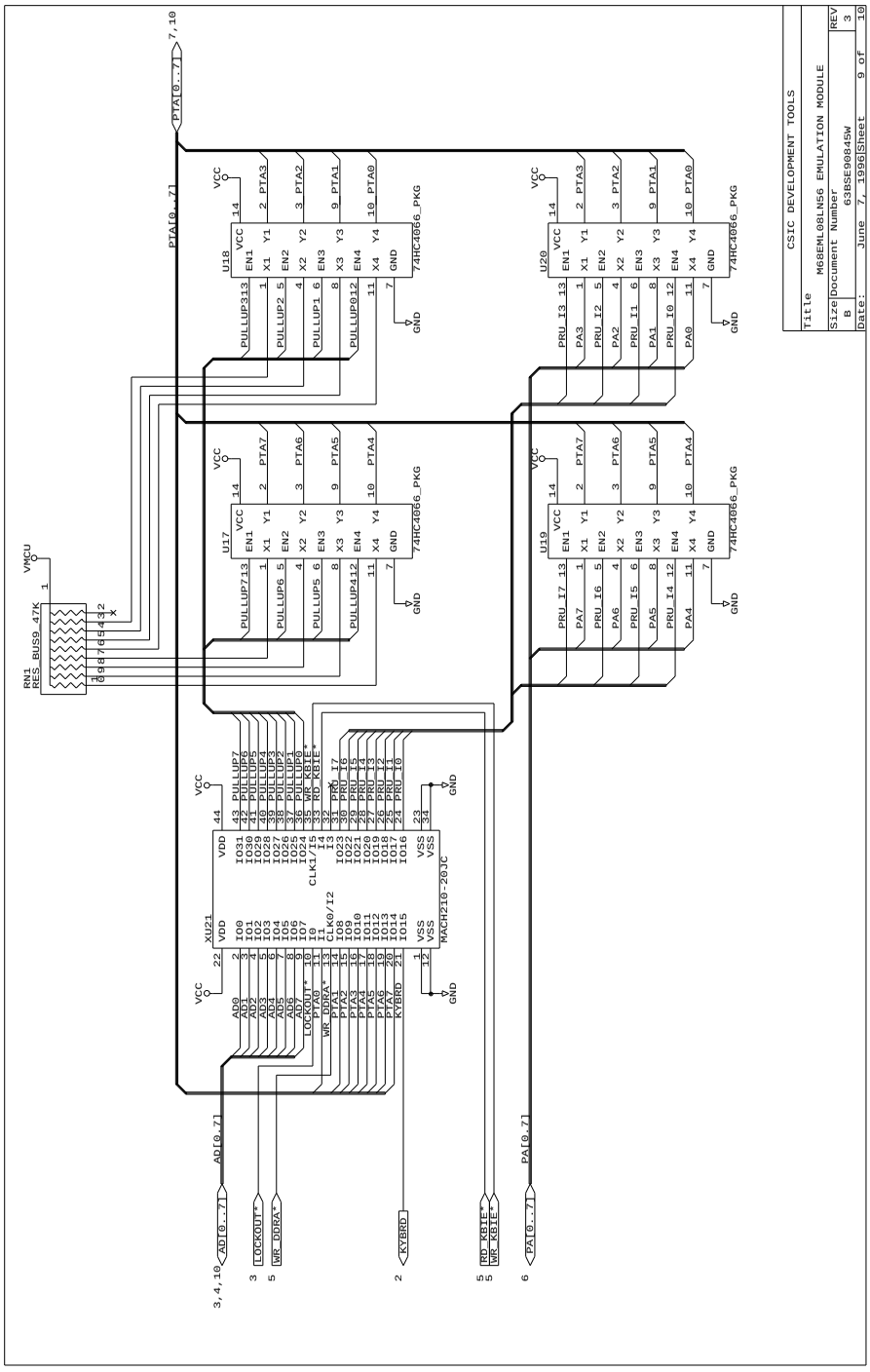
Schematics

M68EML08LN56 Schematics (Sheet 8 of 10)



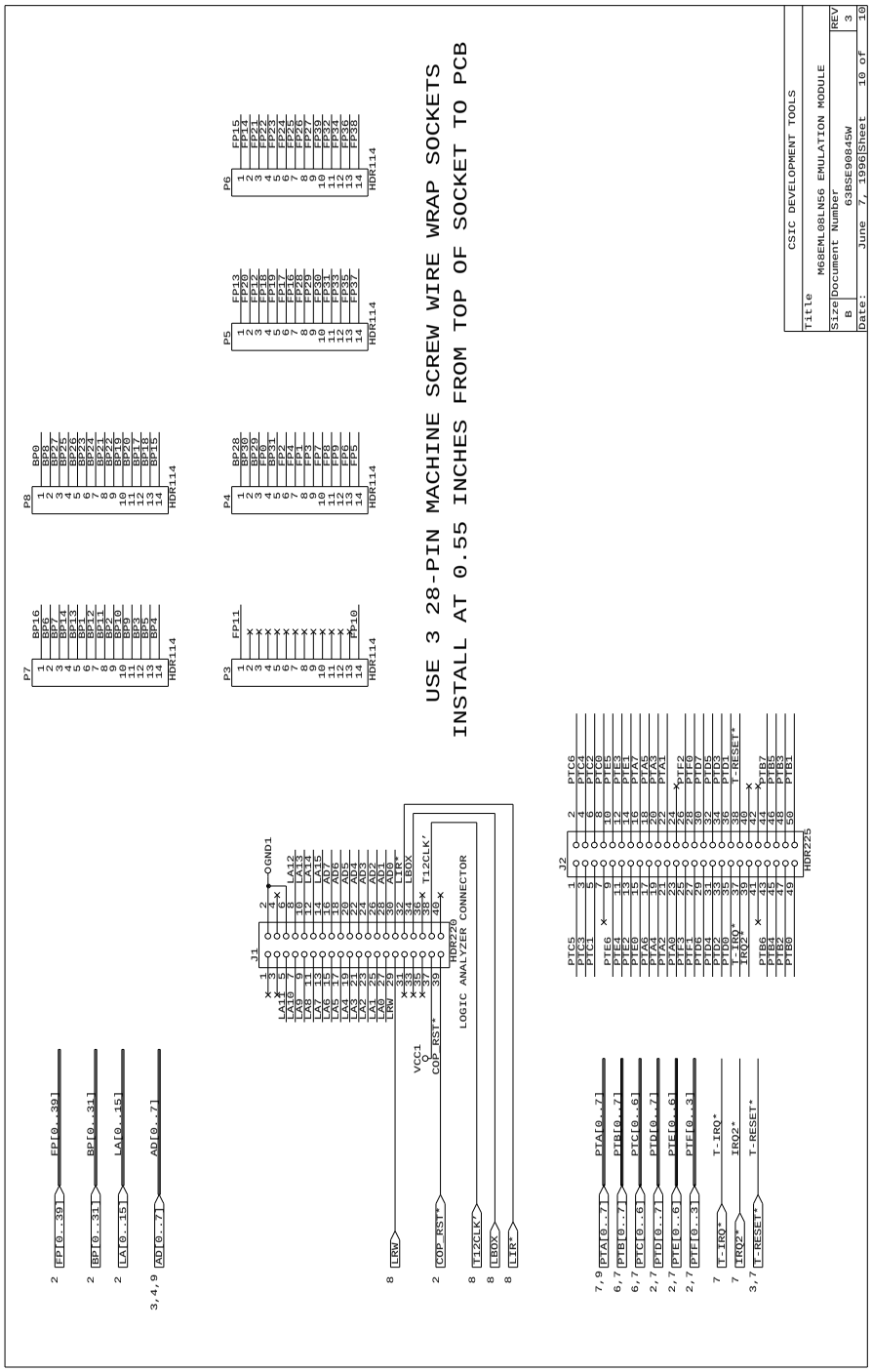
Schematics

M68EML08LN56 Schematics (Sheet 9 of 10)



Schematics

M68EML08LN56 Schematics (Sheet 10 of 10)



Schematics

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