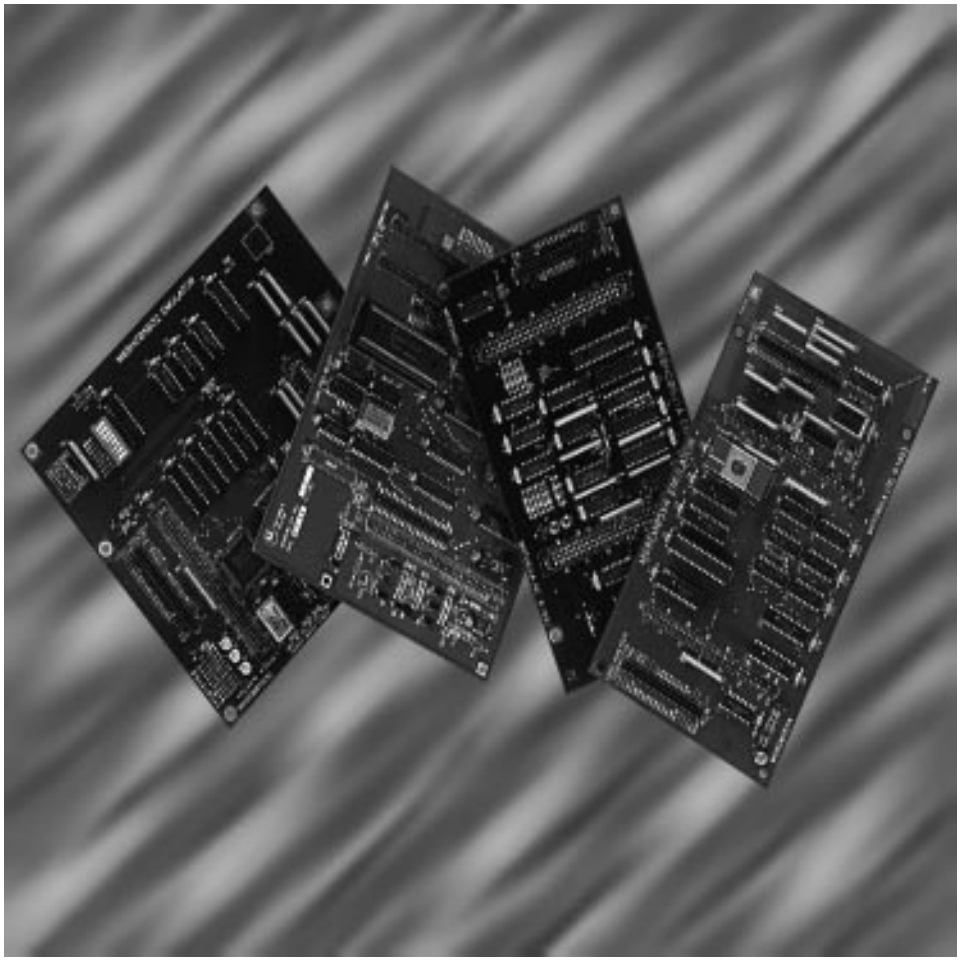
M68EML08XL36

EMULATION MODULE
USER'S MANUAL



MOTOROLA

M68EML08XL36

Emulation Module
User's Manual

Revision History

This table summarizes differences between this revision and the previous revision of this emulation module user's manual.

Previous Revision	None
Current Revision	Original release
Date	06/96

Revision History

Table of Contents

Table of Contents

General Description

Contents

Introduction

Your M68EML08XL36 gives your Motorola development tool the ability to emulate target systems based on MC68HC708XL36 microcontroller units (MCUs). The M68EML08XL36 is designed to be a low-voltage emulator, operating in the 3.0 Vdc to 5.0 Vdc range at maximum rated frequencies per the general release specification.

By substituting a different emulation module (EM), you can enable your Motorola development tool to emulate other MCUs. Refer to *Motorola's Development Tool Selector Guide*, Motorola order number SG173/D, for a complete list of available EMs.

This hardware user's manual explains connection, configuration, and operation information specific to the M68EML08XL36 emulation module. The module can be installed in two Motorola development systems. To configure your M68EML08XL36 for either an MMDS or an MMEVS, follow the instructions given in **MMDS/MMEVS Configuration and Operation** on page 19.

Emulation Components

Motorola’s complete emulation system consists of the emulation module described in this manual as well as other separately purchased options described in the following paragraphs.

The following items are included with the M68EML08XL36 emulation module:

- **An M68EML08XL36 emulation module (EM)** — the printed circuit board that enables system functionality for MC68HC708XL36 MCUs. The female connectors, on the bottom of the module, mate with male connectors on a development system platform board. The EM also has a connector for the target cable assembly.
- **Configuration software** — 3 1/2-inch diskette containing personality files for this module.

Separately purchased Motorola modular development tool options include:

- **An MMEVS platform board (M68MMPFB0508)** — The MMEVS is an economical development tool that provides real-time in-circuit emulation. The unit's integrated design environment includes an editor, an assembler, a user interface, and a source-level debugging program.
- **An MMDS0508 modular development system (MMDS0508)** — The MMDS is a high-performance development tool that has all the capabilities of the MMEVS. In addition, it also has a bus state analyzer and real-time memory windows.
- **Flex cable target assembly** — Refer to **Target Cable Assemblies** on page 12 for more information.

User supplied components include:

- **Host computer** — see the appropriate development tool user’s manual for minimum requirements.
- **Power supply** — +5 Vdc @ 1.0 amp required for the MMEVS.

Emulation Module Layout

Figure 1 shows the layout of the M68EML08XL36. Jumper header W1 lets you select the source of the MCU's oscillator.

Connector J1 connects to a logic analyzer. Target connectors J2 and J3 provide the interface to a target system. These connectors use a separately purchased target cable assembly. When you install the M68EML08XL36 on the MMDS05, the target cable passes through the slit in the station module enclosure.

Variable resistor, VR1, controls MCU operating voltage between 3.0 V and 5.0 V. Test point header TP1 is the monitor point for MCU operating voltage. The MC68HC708XL36 MCU is at location XU1.

DIN connectors P1 and P2 connect the EM and a development system platform board.

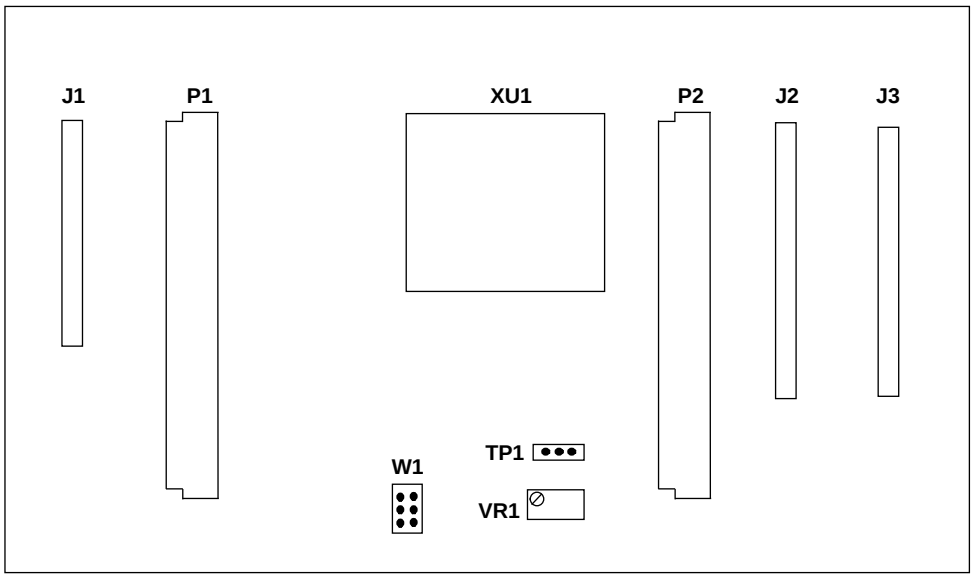


Figure 1. M68EML08XL36 Emulation Module

Target Cable Assemblies

To connect your M68EML08XL36 to a target system, you need a separately purchased target cable assembly. Cable assemblies are available for the 64-pin QFP and 56-pin SDIP MCU packages.

The target cable connects to the emulator via connector J2 and J3 on the M68EML08XL36 emulation module. Pin assignments and signal descriptions for connectors J2 and J3 can be found in **Target Cable Connector Pin Assignments** on page 16.

Figure 2 represents a target cable assembly. An assembly for 64-pin QFP package consists of a flex cable and a QFP target head adapter. The assembly for 56-pin SDIP consists of a flex cable and a SDIP target head adapter. One end of the flex cable plugs onto M68EML08XL36 connector J2 and J3 with orientation shown in **Figure 2**. The other end of the flex cable plugs into the target head adapter. The 64-pin QFP target head adapter then inserts into a TQSOCKET and then a TQPACK installed on the users target system. The 56-pin SDIP target head adapter inserts into a SDIP footprint in a target system.

The MCU package in your target system determines the target cable assembly components required:

- For a 64-pin QFP package, use flex cable M68CBL05C and target head adapter M68TC08XL36FU64. A TQSOCKET w/guides (M68TQS064SAG1) and a TQPACK (M68TQP064SAM01) are included with the target head adapter.
- For a 56-pin SDIP package, use flex cable M68CBL05B and target head adapter M68TB08XL36B56.

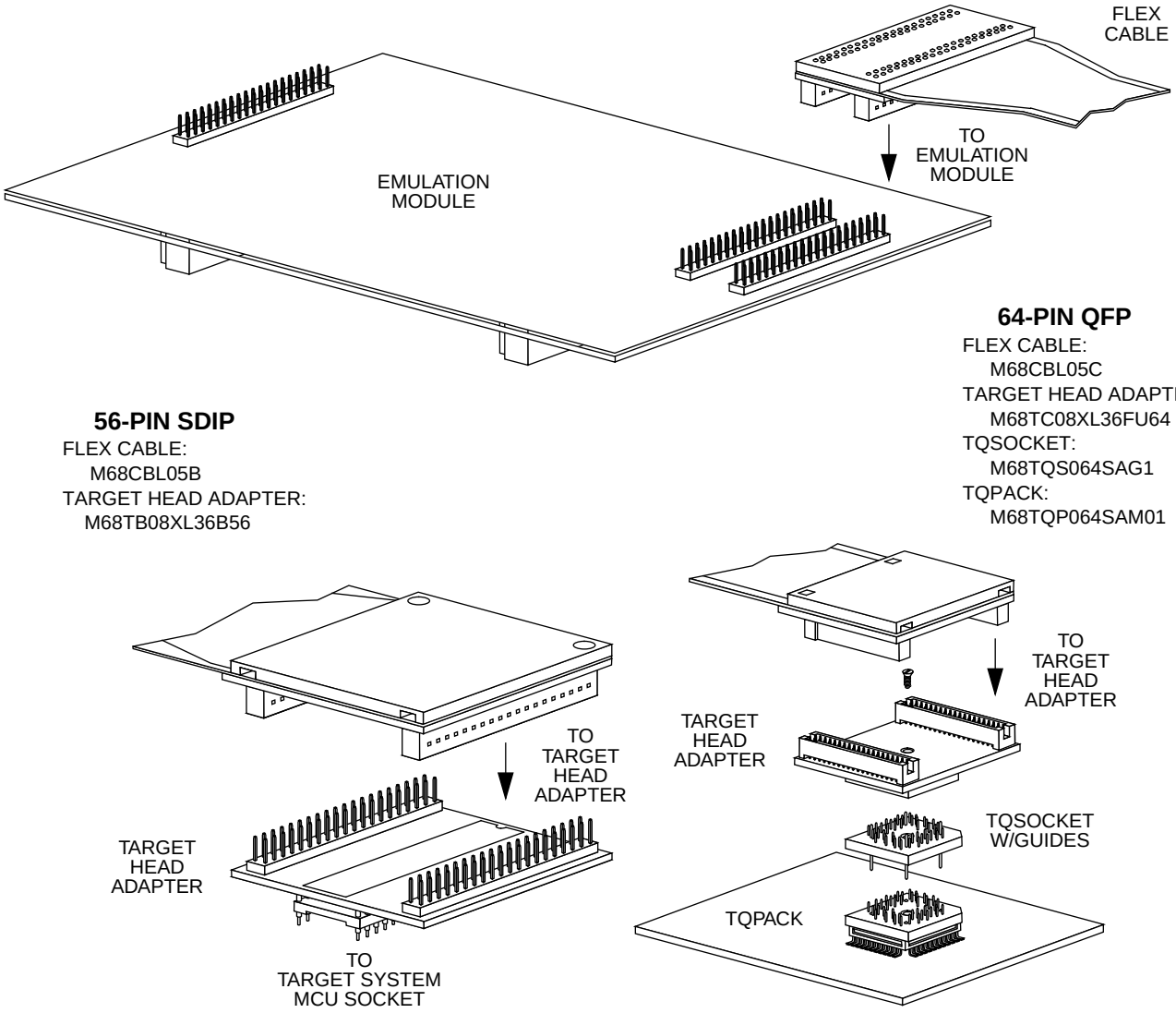


Figure 2. Target Cable Assembly

Connector Information

The connectors on the M68EML08XL36 module provide access to the user mode emulation signals (J2 and J3) as well as select internal signals (J1). Connector J1 is used to connect to a logic analyzer. Connectors J2 and J3 is used for a cable interface to a user's target system.

Logic Analyzer Connector Pin Assignments

Figure 3 shows the pin assignments for logic analyzer connector J1. This connector provides the emulator easy access to many of the signals used internally. **Table 1** lists signal descriptions for this connector.

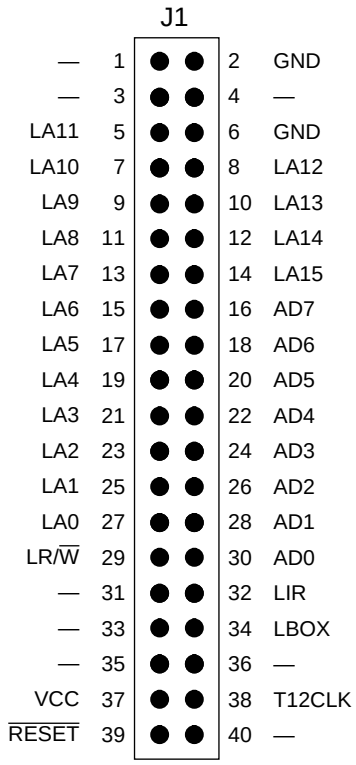


Figure 3. Connector J1 Pin Assignments

Table 1. Logic Analyzer Connector J1 Signal Descriptions

Pin	Mnemonic	Signal
1, 3, 4, 31, 33, 35, 36, 40	NC	NO CONNECTS.
2, 6	GND	GROUND.
8, 10, 12, 14	LA12–LA15	LATCHED ADDRESS (bits 12–15) — MCU latched address bus.
5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27	LA11–LA0	LATCHED ADDRESSES (bits 11–0) — MCU latched address bus.
16, 18, 20, 22, 24, 26, 28, 30	AD7–AD0	DATA BUS (bits 7–0) — MCU multiplexed I/O bus.
29	LR/$\overline{W}$	LATCHED READ/WRITE — The MCU's write signal is latched and used on the emulator to control emulator memory accesses.
32	$\overline{LIR}$	LOAD INSTRUCTION REGISTER — Active low signal indicating an opcode fetch cycle is in process.
34	$\overline{LBOX}$	LAST BOX — Active high signal indicating last cycle of current instruction.
37	V_{CC}	+5 Vdc POWER — Connection to the system voltage V_{CC}.
38	T12CLK	ANALYZER CLOCK — The latched addresses are valid on the latched address bus at the falling edge of T12CLK. Also, data is valid on the AD BUS at T12CLK falling edge.
39	$\overline{RESET}$	RESET — Active-low signal; will be asserted during internally or externally caused resets.

Target Cable Connector Pin Assignments

Figure 4 shows the pin assignments for connector J2 and J3. **Table 2** lists signal descriptions for connector J2. **Table 3** lists signal descriptions for connector J3.

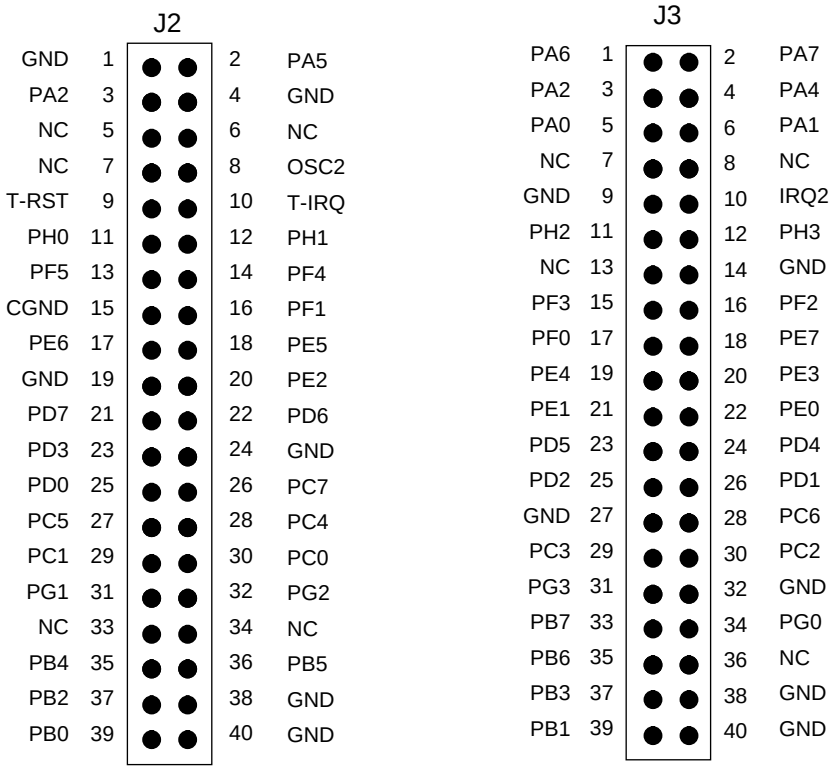


Figure 4. Target Connector Pin Assignments

Table 2. Connector J2 Signal Descriptions

Pin	Mnemonic	Signal
1, 4, 19, 24, 38, 40	GND	GROUND.
2, 3	PA5, PA2	PORT A (bits 5, 2) — General-purpose I/O lines controlled by software via data direction and data registers.
5–7, 33, 34	NC	NO CONNECTS.
8	OSC2	OSCILLATOR 2 — Output from em board to be used by target as sync to osc clock.
9	T-RST	TARGET RESET — Active-low bidirectional signal to/from the target system driven low to pull the MCU into reset.
10	T-IRQ	TARGET INTERRUPT REQUEST — Active-low input signal from the target that asynchronously applies an MCU interrupt.
11, 12	PH0, PH1	PORT H (bits 0, 1) — General-purpose I/O lines controlled by software via data direction and data registers.
13, 14, 16	PF5 ,PF4, PF1/SPSCK	PORT F (bits 5, 4, 1) — General-purpose I/O lines controlled by software via data direction and data registers. PF1 shares its pin with the SPI's clock..
15	CGND	Clock Ground Pin
17, 18, 20	PE6/TCH2, PE5/TCH1, PE2/TXD	PORT E (bits 6, 5, 2) — General-purpose I/O lines controlled by software via data direction and data registers. Bits 6, 5 are shared with the timer module. Bit 2 is shared with the SCI module.
21–23, 25	PD7/KBD7, PD6/KBD6, PD3/KBD3, PD0/KBD0	PORT D (bits 7, 6, 3, 0) — General-purpose I/O lines controlled by software via data direction and data registers. Port D is shared with the keyboard module.
26–30	PC7, PC5, PC4, PC1, PC0	PORT C (bits 7, 5, 4, 1, 0) — General-purpose I/O lines controlled by software via data direction and data registers.
31, 32	PG1, PG2	PORT G (bits 1, 2) — General-purpose I/O lines controlled by software via data direction and data registers.
35–37, 39	PB4, PB5, PB2, PB0	PORT B (bits 4, 5, 2, 0) — General-purpose I/O lines controlled by software via data direction and data registers.

Table 3. Connector J3 Signal Descriptions

Pin	Mnemonic	Signal
1–6	PA6, PA7, PA3, PA4, PA0, PA1	PORT A (bits 6, 7, 3, 4, 0, 1) — General-purpose I/O lines controlled by software via data direction and data registers.
7, 8, 13, 36	NC	NO CONNECTS.
9, 14, 27, 32, 38, 40	GND	GROUND.
10	IRQ2	External Interrupt 2 — Active-low input signal that asynchronously applies an MCU interrupt.
11–12	PH2, PH3	PORT H (bits 2, 3) — General-purpose I/O lines controlled by software via data direction and data registers.
15–17	PF3/MISO, PF2/MOSI, PF0/$\overline{SS}$	PORT F (bits 3, 2, 0) — General-purpose I/O lines controlled by software via data direction and data registers. PF3, PF2, PF0 shares its pin with the SPI module.
18–22	PE7/TCH3, PE4/TCH0, PE3/TCLK, PE1/RXD, PE0	PORT E (bits 7, 4, 3, 1, 0) — General-purpose I/O lines controlled by software via data direction and data registers. Bits 7, 4, 3 are shared with the timer module. Bit 1 is shared with the SCI module.
23–26	PD5/KBD5, PD4/KBD4, PD2/KBD2, PD1/KBD1	PORT D (bits 5, 4, 2, 1) — General-purpose I/O lines controlled by software via data direction and data registers. Port D is shared with the keyboard module.
28–30	PC6, PC3, PC2	PORT C (bits 6, 3, 2) — General-purpose I/O lines controlled by software via data direction and data registers.
31, 34	PG3, PG0	PORT G (bits 3, 0) — General-purpose I/O lines controlled by software via data direction and data registers.
33, 35, 37, 39	PB7, PB6, PB3, PB1	PORT B (bits 7, 6, 3, 1) — General-purpose I/O lines controlled by software via data direction and data registers.

MMDS/MMEVS Configuration and Operation

Contents

Introduction

The following paragraphs explain how to configure and use your M68EML08XL36 as part of an MMDS or MMEVS system. For other parts of system installation and configuration, see either the *MMDS0508 Operations Manual* (MMDS05OM/D) or *MMEVS05/MMEVS08 Operations Manual* (MMEVS0508OM/D).

The topics covered in this chapter are:

- **Setting M68EML08XL36 Jumper Header** on page 21 explains how to set the M68EML08XL36 jumper headers.
- **Remaining System Installation** on page 23 covers the final steps to system installation.
- **Setting Emulation Voltage** on page 24 explains how to adjust the MC68HC708XL36 MCU operating voltage.
- **Personality File Usage** on page 25 discusses the personality file used on the M68EML08XL36 board.
- **MC68HC(7)08XL36 Emulation** on page 25 explains special considerations for emulating with this module.

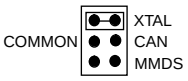
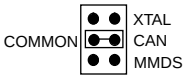
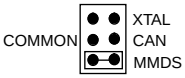
NOTE: *You can configure an M68EML08XL36 already installed in the system platform board. To do so, remove system power and then follow the guidance of this chapter.*

CAUTION: *Be sure to switch off power before you reconfigure an installed EM. Reconfigure EM jumper headers with the power on can damage emulation circuits.*

Setting M68EML08XL36 Jumper Header

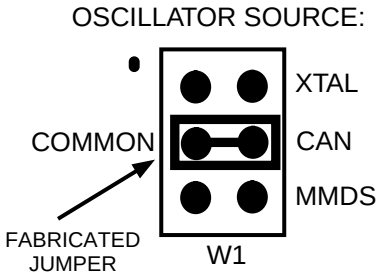
Your M68EML08XL36 has one jumper header — W1. The following table provides a quick reference for configuration options. Refer to the paragraphs that follow for a more detailed explanation.

Table 1. Jumper Header Positions for MMDS/MMEVS

Jumper	Position	Description	Factory Setting
Clock Source Select, W1		Selects a user supplied crystal oscillator circuit as the MCU clock source.	
		Select the 4.9152 MHz canned oscillator located on the EM board at XY1.	X
		Select the clock originating from the development system platform board. The frequency is controlled by the OSC command and is 4 MHz on power up.	

Clock Source Select Header, W1

Jumper header W1 determines the clock-signal source. The diagram below illustrates the jumper header where the pin marked COMMON is always connected to one of the three clock source pins via the fabricated jumper. The default configuration, between CAN and COMMON, selects the 4.9152 MHz canned oscillator clock source (at board location XY1).



There are two other possible clock sources. To use the one originating from the development system platform, reposition the W1 jumper header between the MMDS05 and COMMON pins. Then use the system's OSC command to select a frequency.

For a user supplied crystal source, the user must install components Y1, R15, R16, C21, and C22, reposition the W1 jumper header between the XTAL and COMMON pins. Consult the schematics sheet 5 for actual component connection.

Remaining System Installation

When you have configured headers W1, M68EML08XL36 configuration is complete:

- Ensure that the power to the development tool is off.
- If installing the M68EML08XL36 in an MMDS station module, remove the panel from the station module top.
- Fit together EM connectors P1 and P2 (on the bottom of the board) and platform board DIN connectors. Snap the corners of the EM onto the plastic standoffs.
- Connect the target cable, if appropriate.
- If installing in an MMDS05, replace the panel.

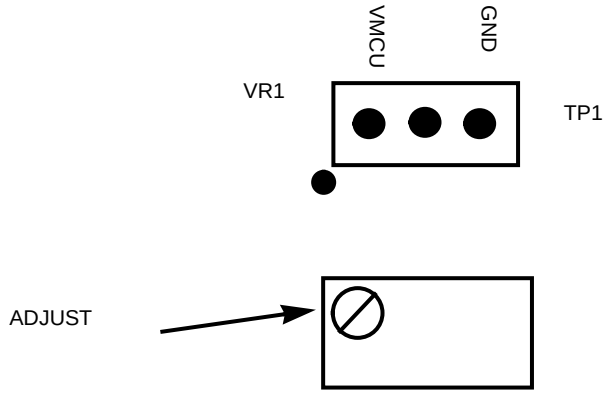
At this point, you are ready to make remaining cable connections, as necessary, and restore power.

For instructions, consult either the *MMEVS05/MMEVS08 Operations Manual* (MMEVS0508OM/D) or the *MMDS0508 Operations Manual* (MMDS0508OM/D).

Setting Emulation Voltage

The M68EML08XL36 module has an on-board voltage regulator that can be adjusted to provide low voltage emulation in the 3.0 V to 5.0 V range. The adjustment for that variable voltage is variable resistor VR1. Test point TP1 is used for connection to a voltmeter during voltage adjustment. (See illustration below.)

To adjust the MCU operating voltage, first ensure that no target cable is connected to target cable connectors J2 and J3. Second, connect a voltmeter across the GND and VMCU pins of test point header TP1. Finally, adjust variable resistor VR1 to the desired voltage level. Make sure that the target systems operating voltage is at the newly adjusted level before connecting target signals through the J2 and J3 connectors.



Personality File Usage

Your development system uses a specific personality file for the MCU type being emulated. For example, to emulate an MC68HC(7)08XL36 MCU, the system uses the personality file 00411Vxx.MEM. Debugger software loads this personality file upon power up.

NOTE: *Personality file names follow the pattern 00ZZZVxx.MEM, where ZZZ is the EM identifier or MCU name and xx is the version of the file*

MC68HC(7)08XL36 Emulation

NOTE: *Be aware that if the computer operating properly disable bit (COPD) option in the configuration register $1F is enabled out of reset, your code must clear the COP watchdog timer counter to avoid a COP reset. The counter is cleared by writing any value at location $FFFF. This should be the first check when code is not operating as expected.*

The MC68HC08XL36 MCU is emulated on the M68EML08XL36 emulation module. The resident MCU (socket XU1) can be either a ROM device, a MC68HC08XL36, or an EPROM device, a MC68HC708XL36. Because emulation flexibility is optimum when using the EPROM device, the M68EML08XL36 is shipped with an MC68HC708XL36 as the resident MCU.

The following paragraphs detail known differences between the performance of an MC68HC(7)08XL36 MCU running in single-chip mode versus the way certain features will perform during emulation mode.

Pullup on $\overline{\text{IRQ}}$

In single-chip mode operation:

There is no pullup on the $\overline{\text{IRQ}}$ pin. Your application must pull the $\overline{\text{IRQ}}$ pin to V_{DD} level to prevent interrupts.

In emulation:

The $\overline{\text{IRQ}}$ pin is pulled up on the module. Be aware that an application without the $\overline{\text{IRQ}}$ pin pulled high will emulate correctly but will fail in the application because of a floating IRQ line. The $\overline{\text{IRQ}}$ pin pulled high on the module causes these results.

Schematics

Contents

M68EML08XL36 Schematics

Refer to the following pages for the five sheets of schematics for the M68EML08XL36 emulation module.

M68EML08XL36 Schematics

M68EML08XL36 Schematics (Sheet 1 of 5)

NOTES, UNLESS OTHERWISE SPECIFIED

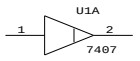
1. VCC PIN LOCATIONS :

   VCC IS APPLIED TO PIN 8 OF ALL 8-PIN IC's, PIN 14 OF ALL 14-PIN IC's, PIN 16 OF ALL 16-PIN IC's, PIN 20 OF ALL 20-PIN IC's, ETC.

2. GROUND PIN LOCATIONS :

   GROUND IS APPLIED TO PIN 4 OF ALL 8-PIN IC's, PIN 7 OF ALL 14-PIN IC's, PIN 8 OF ALL 16-PIN IC's, PIN 10 OF ALL 20-PIN IC's, ETC.

3. DEVICE TYPE, PIN NUMBERS, AND REFERENCE DESIGNATOR OF GATES ARE SHOWN AS FOLLOWS :



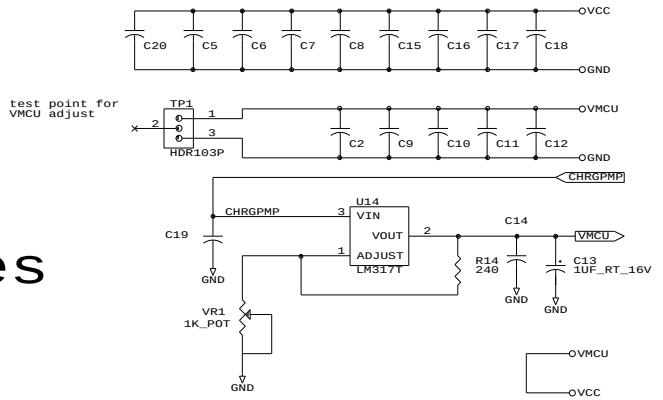
7407 = DEVICE TYPE
1 AND 2 = PIN NUMBERS
U1A = REFERENCE DESIGNATORS

4. RESISTANCE VALUES ARE IN OHMS.
5. RESISTORS ARE 1/4 WATT, 5%.
6. CAPACITANCE VALUES ARE IN MICROFARADS.

M68EML08XL36 CPU BOARD

REVISIONS		
REV	DESCRIPTION	DATE
2	added R100 (10K) pullup to T12CLK. T12CLK floating out of reset, causing reset problems at 3.0V	12/11/95
3	chged R10,R12 to 4.7K, cop being enabled in bg, chged U12,U13 to 74HCT74 due to glitch on LR/W on bnksw pal on MMEVS	2/8/96

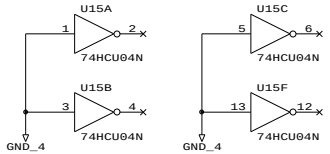
All caps are 0.1 uF @ 50 V



VCC = 5V (plance)
VMCU = Vreg (plane)

NOTE: make isolated plane for VMCU on PCB layout!

Spare Gates



0RCAD IV FLAT FILES

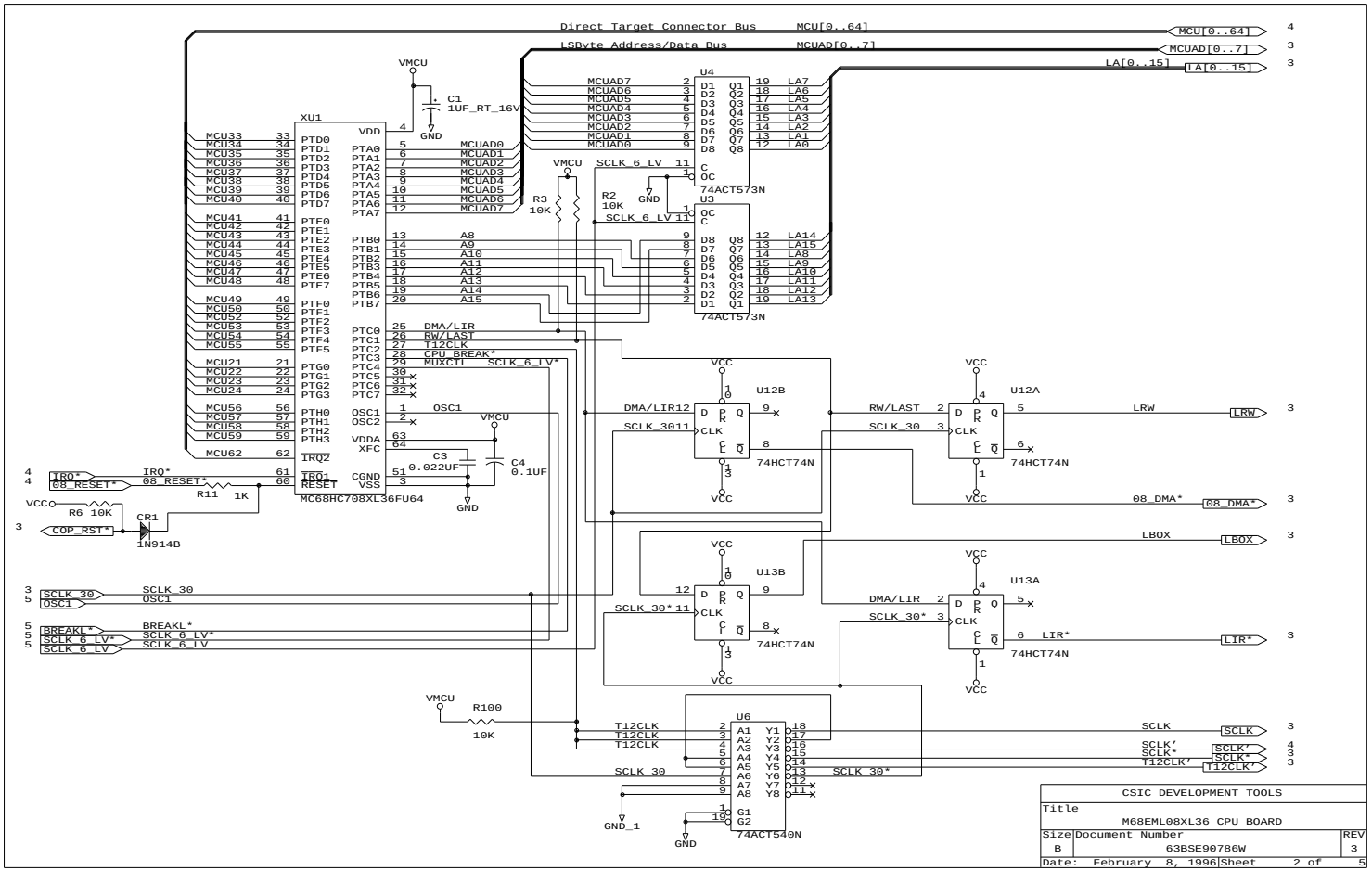
LINK
LVXLR3S2.SCH
LVXLR3S3.SCH
LVXLR3S4.SCH
LVXLR3S5.SCH

COMPUTER GENERATED DRAWING : DO NOT REVISE MANUALLY

CSIC DEVELOPMENT TOOLS		
Title: M68EML08XL36 CPU BOARD		
Size: B	Document Number: 63BSE90786W	REV: 3
Date: February 8, 1996	Sheet 1 of 5	

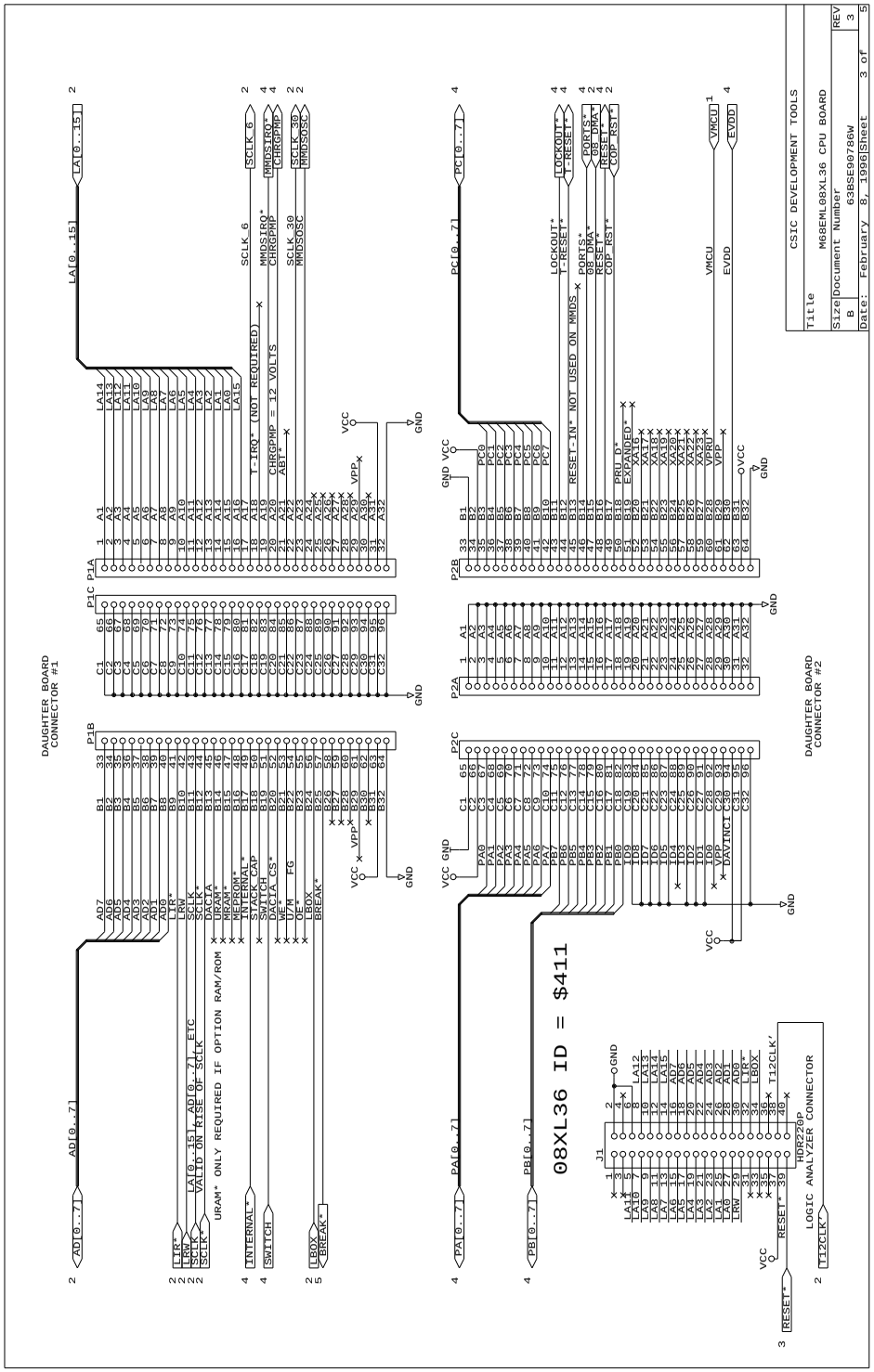
M68EML08XL36 Schematics

M68EML08XL36 Schematics (Sheet 2 of 5)



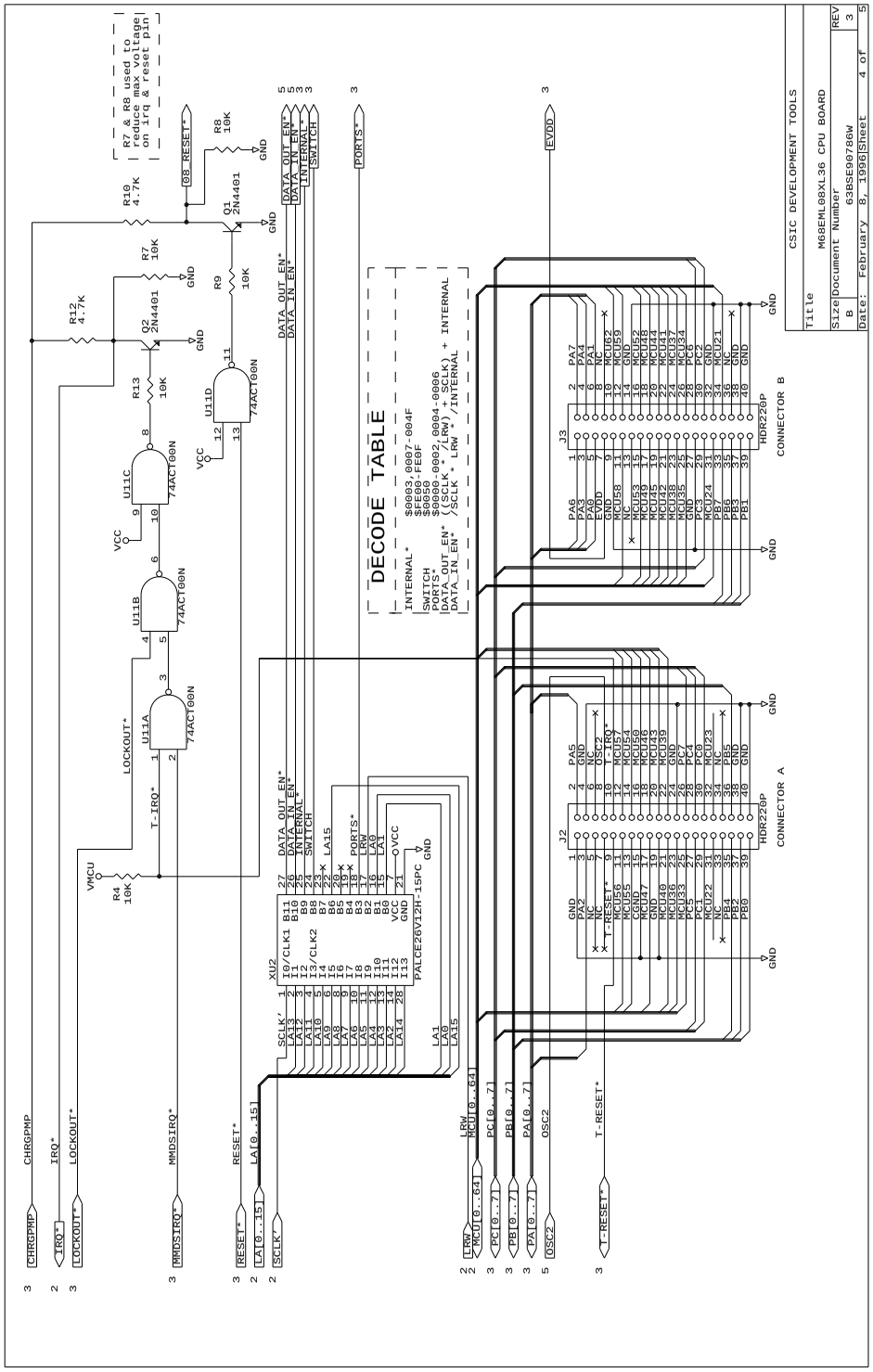
M68EML08XL36 Schematics

M68EML08XL36 Schematics (Sheet 3 of 5)



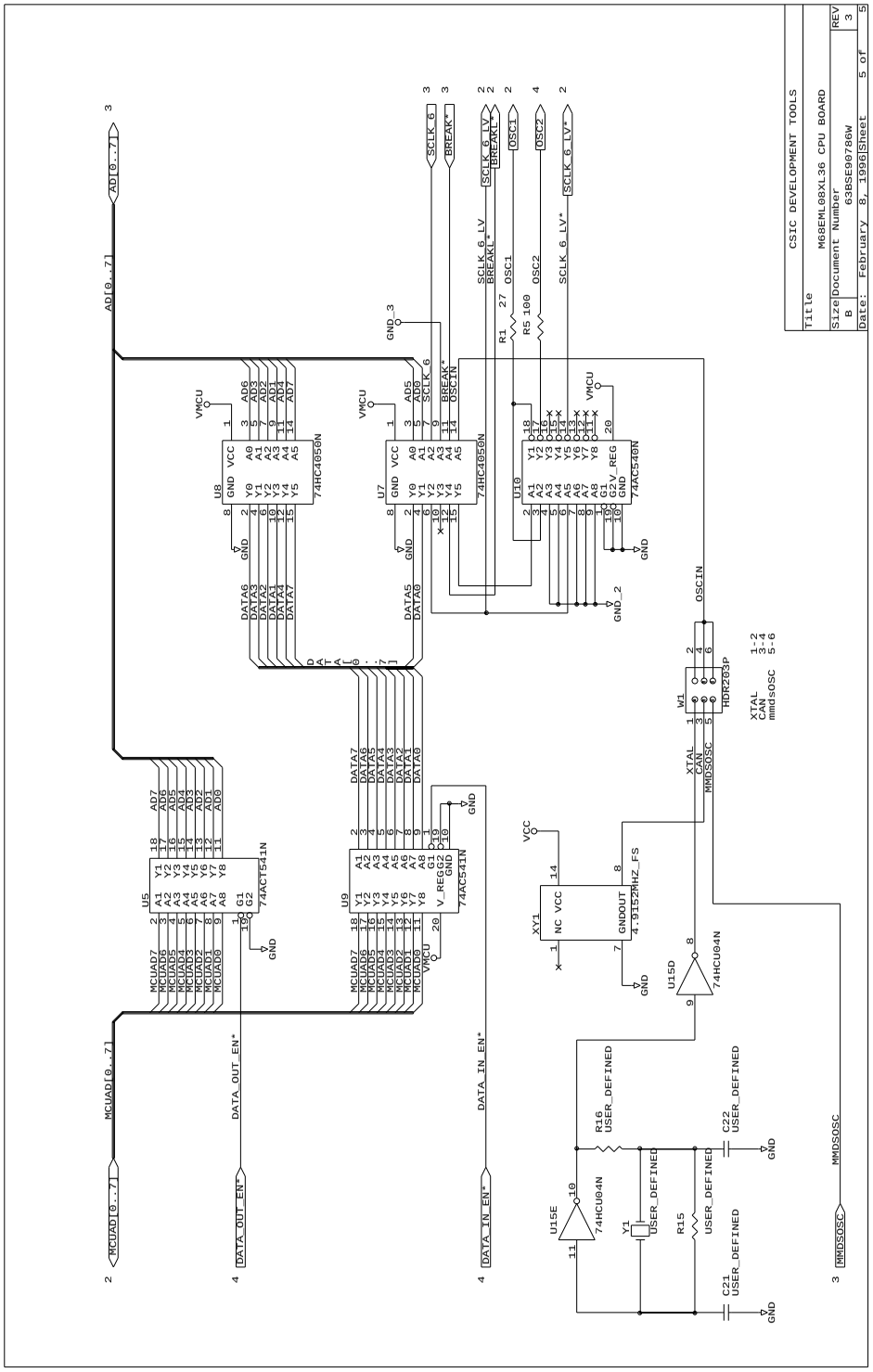
M68EML08XL36 Schematics

M68EML08XL36 Schematics (Sheet 4 of 5)



M68EML08XL36 Schematics

M68EML08XL36 Schematics (Sheet 5 of 5)



M68EML08XL36 Schematics

How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.1-800-441-2447 or 602-303-5454

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE 602-244-6609

INTERNET: http://Design-NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-81-3521-8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298