SG184/D
Rev 1

MOTOROLA

Wireless Infrastructure Systems Division

DSP Products

4th Quarter 1998

Motorola DSP563xx Advantages

A Balanced Architecture

Compatibility

Compatible with 56000 family; preserves code investment

On-chip Memory

Up to 64K words today

Low Voltage

2.5/3.3 volt; functional down to 1.8v

Low Power

0.9 mA/MIPS at 2.5v, 1.3mA/MIPS at 3.3v

Ease of Programming

24-bit wide, highly orthogonal instruction set, transparent pipeline, position-independent code, hardware stack extension, fully nested hardware do loops and interrupts, auto return interrupts, VSL instruction for efficient software Viterbi decoding

Mixed Precision

Selectable precision (24 or 16), on a per application basis

DMA

Six independent general-purpose channels, concurrent to the core, MIPS savings, power and pointers

Instruction Cache

1K word internal cache minimizes effect of external memory

Powerful Peripherals

Reduce need for external logic; each is able to trigger DMAs

Co-processors

Very cost effective application-specific acceleration

Contents

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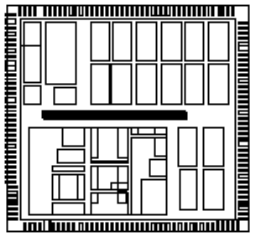
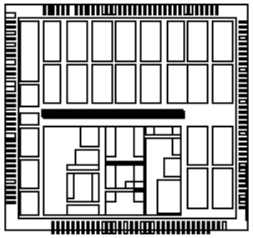
Design Focus



56301



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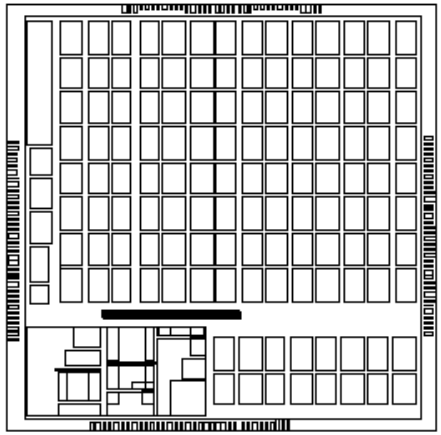

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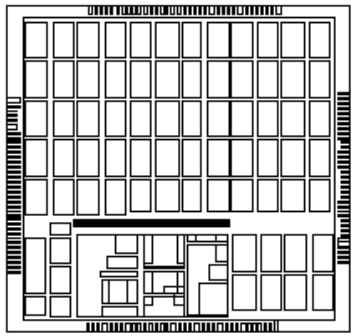


56309

DSP	Performance	Voltage	On-chip Memory	Peripherals	Package	Applications
56301	24-bit program 24-bit data 66/80 MIPS 66/80 MHz	3.3v core 3.3v I/O	8K 2 - 4K Program RAM 4 - 6K Data RAM	2 ESSI 1 SCI Triple Timer Module GPIO 32-bit PCI Host (HI32)	208-pin TQFP 252-pin PBGA	General-purpose digital signal processing, particularly useful in multimedia and telecommunication applications, such as video-conferencing and base transceiver stations
56303	24-bit program 24-bit data 66/80 MIPS 66/80 MHz	3.3v core 3.3v I/O	8K 2 - 4K Program RAM 4 - 6K Data RAM	2 ESSI 1 SCI Triple Timer Module GPIO 8-bit Host (HI08)	144-pin TQFP 196-pin PBGA	Telecommunication applications, such as multi-line voice/data/fax processing, video-conferencing, audio applications, control, and general digital signal processing
56307	24-bit program 24-bit data 100 MIPS 100 MHz	2.5v core 3.3v I/O	64K 16 - 48K Program RAM 16 - 48K Data RAM	2 ESSI 1 SCI Triple Timer Module GPIO 8-bit Host (HI08) EFCOP	196-pin PBGA	Wireless infrastructure applications with general filtering operations
56309	24-bit program 24-bit data 80 MIPS 80 MHz	3.3v core 3.3v I/O	34K 20 - 24K Program RAM 10 -14K Data RAM	2 ESSI 1 SCI Triple Timer Module GPIO 8-bit Host (HI08)	144-pin TQFP 196-pin PBGA	Applications requiring large internal memory, mainly in wireless, wireline local loop, and wireline infrastructure

DSP Products

Technical Documentation and chip errata (if applicable) are available at the Motorola DSP Web site:
http://www.mot.com/SPS/WIRELESS/documentation/dspdocs.html

Part Number	MOQ*	Package	Voltage	Speed	Program ROM/RAM	Data ROM/RAM	Peripherals	Comments
DSP56000 Family General Purpose 24-Bit Fixed Point								
DSP56002FC40	36	132-pin PQFP	5.0v core 5.0v I/O	40 MHz	64/512	2x256/2x256	Host,SSI,SCI,Timer	OnCE and PLL
DSP56002FC66	36	132-pin PQFP	5.0v core 5.0v I/O	66 MHz	64/512	2x256/2x256	Host,SSI,SCI,Timer	OnCE and PLL
DSP56002PV40	36	144-pin TQFP	5.0v core 5.v0 I/O	40 MHz	64/512	2x256/2x256	Host,SSI,SCI,Timer	OnCE and PLL
DSP56002PV66	36	144-pin TQFP	5.0v core 5.0v I/O	66 MHz	64/512	2x256/2x256	Host,SSI,SCI,Timer	OnCE and PLL
DSP56002PV80	36	144-pin TQFP	5.0v core 5.0v I/O	80 MHz	64/512	2x256/2x256	Host,SSI,SCI,Timer	OnCE and PLL
Order 2-unit sample packs by adding the prefix SPAK to the part numbers above.								
DSP56300 Family High Performance 24-Bit Fixed Point								
XC56301PW66	84	208-pin TQFP	3.3v core 3.3v I/O	66 MHz	__/4096	__/4096	32-bit Host, ESSI, SCI, Triple Timer	Single clock-cycle per instruction, barrel shifter, instruction cache, DMA
SPAKXC56301PW66	2	208-pin TQFP	3.3v core 3.3v I/O	66 MHz	__/4096	__/4096	32-bit Host, ESSI, SCI, Triple Timer	Single clock-cycle per instruction, barrel shifter, instruction cache, DMA
XC56301PW80	84	208-pin TQFP	3.3v core 3.3v I/O	80 MHz	__/4096	__/4096	32-bit Host, ESSI, SCI, Triple Timer	Single clock-cycle per instruction, barrel shifter, instruction cache, DMA
SPAKXC56301PW80	2	208-pin TQFP	3.3v core 3.3v I/O	80 MHz	__/4096	__/4096	32-bit Host, ESSI, SCI, Triple Timer	Single clock-cycle per instruction, barrel shifter, instruction cache, DMA
XC56301GC66	126	252-pin PBGA	3.3v core 3.3v I/O	66 MHz	__/4096	__/4096	32-bit Host, ESSI, SCI, Triple Timer	Single clock-cycle per instruction, barrel shifter, instruction cache, DMA
SPAKXC56301GC66	2	252-pin PBGA	3.3v core 3.3v I/O	66 MHz	__/4096	__/4096	32-bit Host, ESSI, SCI, Triple Timer	Single clock-cycle per instruction, barrel shifter, instruction cache, DMA
XC56301GC80	126	252-pin PBGA	3.3v core 3.3v I/O	80 MHz	__/4096	__/4096	32-bit Host, ESSI, SCI, Triple Timer	Single clock-cycle per instruction, barrel shifter, instruction cache, DMA
SPAKXC56301GC80	2	252-pin PBGA	3.3v core 3.3v I/O	80 MHz	__/4096	__/4096	32-bit Host, ESSI, SCI, Triple Timer	Single clock-cycle per instruction, barrel shifter, instruction cache, DMA
XC56303PV66	36	144-pin TQFP	3.3v core 3.3v I/O	66 MHz	__/4096	__/4096	8-bit Host, ESSI, SCI, Triple Timer	Single clock-cycle per instruction, barrel shifter, instruction cache, DMA
SPAKXC56303PV66	2	144-pin TQFP	3.3v core 3.3v I/O	66 MHz	__/4096	__/4096	8-bit Host, ESSI, SCI, Triple Timer	Single clock-cycle per instruction, barrel shifter, instruction cache, DMA
XC56303PV80	36	144-pin TQFP	3.3v core 3.3v I/O	80 MHz	__/4096	__/4096	8-bit Host, ESSI, SCI, Triple Timer	Single clock-cycle per instruction, barrel shifter, instruction cache, DMA
SPAKXC56303PV80	2	144-pin TQFP	3.3v core 3.3v I/O	80 MHz	__/4096	__/4096	8-bit Host, ESSI, SCI, Triple Timer	Single clock-cycle per instruction, barrel shifter, instruction cache, DMA
XC56303GC66	126	196-pin PBGA	3.3v core 3.3v I/O	66 MHz	__/4096	__/4096	8-bit Host, ESSI, SCI, Triple Timer	Single clock-cycle per instruction, barrel shifter, instruction cache, DMA
SPAKXC56303GC66	2	196-pin PBGA	3.3v core 3.3v I/O	66 MHz	__/4096	__/4096	8-bit Host, ESSI, SCI, Triple Timer	Single clock-cycle per instruction, barrel shifter, instruction cache, DMA
XC56303GC80	126	196-pin PBGA	3.3v core 3.3v I/O	80 MHz	__/4096	__/4096	8-bit Host, ESSI, SCI, Triple Timer	Single clock-cycle per instruction, barrel shifter, instruction cache, DMA
SPAKXC56303GC80	2	196-pin PBGA	3.3v core 3.3v I/O	80 MHz	__/4096	__/4096	8-bit Host, ESSI, SCI, Triple Timer	Single clock-cycle per instruction, barrel shifter, instruction cache, DMA
XC56307GC100C	126	196-pin PBGA	2.5v core 3.3v I/O	100 MHz	__/16384	__/49152	8-bit Host, ESSI, SCI, Triple Timer, EFCOP	Single clock-cycle per instruction, barrel shifter, instruction cache, DMA
SPAKXC307GC100C	2	196-pin PBGA	2.5v core 3.3v I/O	100 MHz	__/16384	__/49152	8-bit Host, ESSI, SCI, Triple Timer, EFCOP	Single clock-cycle per instruction, barrel shifter, instruction cache, DMA

MOQ = Minimum Order Quantity
OnCE = On-chip Emulation Module

PLL = Phase Lock Loop
PBGA = Plastic Ball Grid Array

TQFP = Thin Quad Flat Package PQFP = Plastic Quad Flat Package
*Contact your local Motorola sales office or authorized Motorola distributor for availability.

DSP Products (Continued)

Part Number	MOQ*	Package	Voltage	Speed	Program ROM/RAM	Data ROM/RAM	Peripherals	Comments
XC56309PV80	36	144-pin TQFP 196-pin PBGA	3.3v core 3.3v I/O	80 MHz	__/20480	__/14336	8-bit Host, ESSI, SCI, Triple Timer	Single clock-cycle per instruction, barrel shifter, instruction cache, DMA
SPAKXC56309PV80	2	144-pin TQFP 196-pin PBGA	3.3v core 3.3v I/O	80 MHz	__/20480	__/14336	8-bit Host, ESSI, SCI, Triple Timer	Single clock-cycle per instruction, barrel shifter, instruction cache, DMA
MOQ = Minimum Order Quantity OnCE = On-chip Emulation Module		PLL = Phase Lock Loop PBGA = Plastic Ball Grid Array			TQFP = Thin Quad Flat Package PQFP = Plastic Quad Flat Package *Contact your local Motorola sales office or authorized Motorola distributor for availability.			

DSP Development Tools

Part Number	Description	Version
DSP56000 Software		
DSPTOOLSCD	DSP56000 Family Simulator/Assembler/Linker/Librarian/C Compiler for IBM® PC, SUN-4, and Hewlett-Packard Series 700	6.2
DSP56300 Software		
DSPTOOLSCD	DSP56300 Family Simulator/Assembler/Linker/Librarian/C Compiler for IBM PC, SUN-4, and Hewlett-Packard Series 700	6.2
CDWISD/D	*Using the Motorola DSP56307*, Multimedia Training CD-ROM for Windows 95/NT	
DSP56000 Hardware		
DSP56002EVM	DSP56002 Low-Cost Evaluation Module Including Software	
DSP56300 Hardware		
DSP56301ADSA	DSP56301 Development System for IBM PC	
DSP56301ADSF	DSP56301 Development System for SUN-4	
DSP56303EVM	DSP56303 Evaluation Module Including Software	2.2
DSP56307EVM	DSP56307 Evaluation Module Including Software	
DSP56309EVM	DSP56309 Evaluation Module Including Software	
Universal Hardware		
DSPPCHOST	PC Compatible Host Board and Interface Software	2.0
DSPSUN4HOST	SUN-4 Host Board and Interface Software	2.0
DSPCOMMAND	16-, 24-, 32-Bit Command Converter Board	6.1

Chip Errata

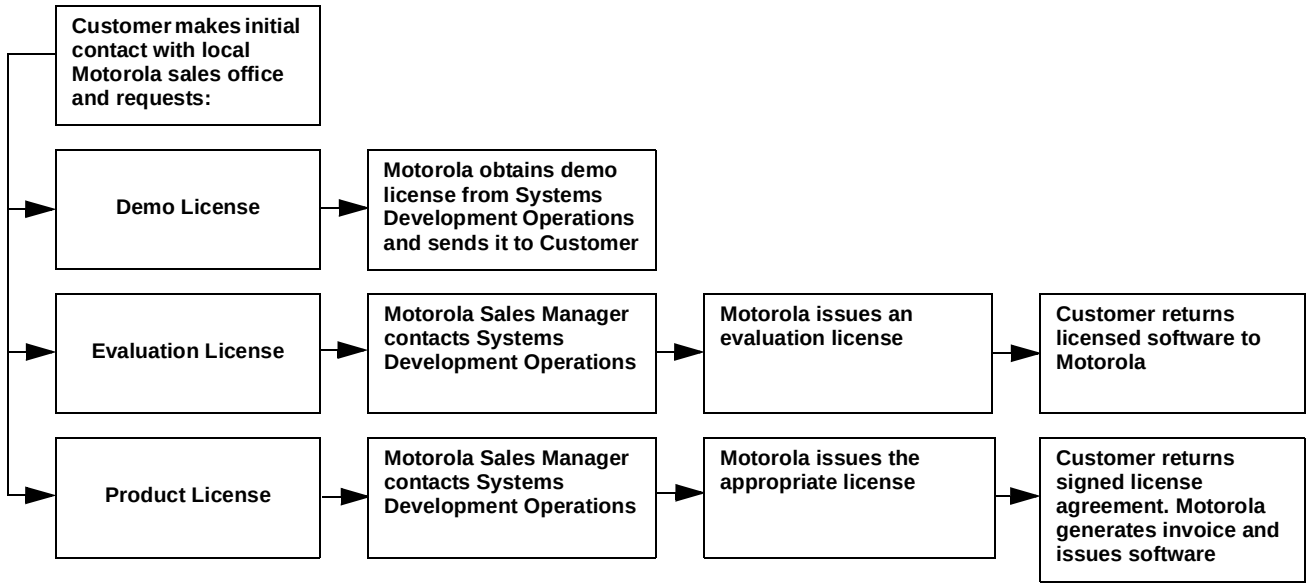
Chip errata are available for the following DSPs and masks at the Motorola DSP Web site:
http://www.mot.com/SPS/WIRELESS/documentation/dspdocs.html

DSP	Mask Number
DSP56002	D41G
DSP56301	0F92R (Revision 3.7); 1F92R (Revision 2.9); 0F48S (Revision 3.1); 1F48S (Revision 2.4); 2F48S; 3F48S (Revision 1.5)
DSP56303	0F88S; 0F94R; 1F94R; 0H826; 0J22A; 2J22A; 3J22A; 4J22A
DSP56307	2H83G
DSP56309	4H80G; 5H80G (Revision 1.1); 6H74G (Revision 1.1)

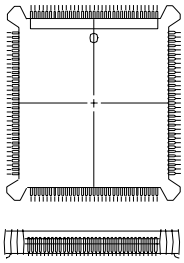
DSP563xx Application Software

Part No.	Description For Availability, Contact Motorola Sales
IS-95 CDMA Voice Codec SW Products	
MSW1D101AAF	8kbps QCELP (IS-96A)
MSW1D102AAF	13kbps QCELP (CDG-27)
MSW1D103AAF	EVRC (IS-127)
MSW1D100AAF	IS-95 CDMA Voice Codec Suite (all 3 codecs)
GSM Voice Codec SW Products	
MSW1D201AAF	GSM Half Rate (HR) VSELP, 5.6kbps
MSW1D202AAF	GSM Full Rate (FR) RPE-LTP, 13kbps
MSW1D203AAF	GSM Enhanced Full Rate (EFR) ACELP, 12.2kbps
MSW1D200AAF	GSM Voice Codec Suite (all 3 codecs)
Audio Codec SW Products	
MSW1D001AAF	G.711 codec 48, 56 and 64kbps
MSW1D002AAF	G.722 codec 48, 56 and 64kbps
MSW1D003AAF	G.728 codec 16kbps
MSW1Y001AAF	G.711/G.722/G.728 (set of 3 codecs)
MSW1D004AAF	G.723.1 codec xmit at 5.3 and 6.4kbps
MSW1Y003AAF	G.711/G.722/G.728/G.723.1 (set of 4 codecs)
MSW1D007AAF	G.726 codec 16, 24, 32 and 40kbps
MSW1D005AAF	G.729a codec
MSW1D006AAF	G.729 codec
Echo Cancellation SW Products	
MSW1A001AAF	Hybrid Echo Cancellation (HEC)
MSW1A003AAF	Acoustic Echo Cancellation (AEC)
General Communication SW Products	
MSW1A002AAF	Dual Tone Multi-frequency (DTMF)
Fax/Data Modem SW Products	
MSW1B001AAF	V.21, V.27ter, V.29 Fax Modem Pumps
MSW1B002AAF	V.17 Fax Modem Pump
MSW1B003AAF	V.32/V.32 bis Data Modem
MSW1B000AAF	V.32 Data/Fax Modem Suite (all above)
ISDN SW Products	
MSW1C201AAF	Passive Integrated Services Data Network (ISDN)

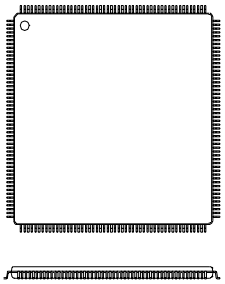
Ordering Application Software



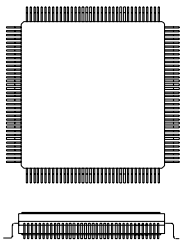
Packages



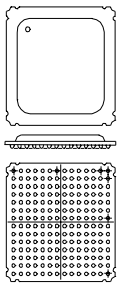
Plastic Quad Flat Package
FC Suffix
132-Pin
Pin Pitch .635 mm
Case No. 831A
1.1 X 1.1 X .19 inches



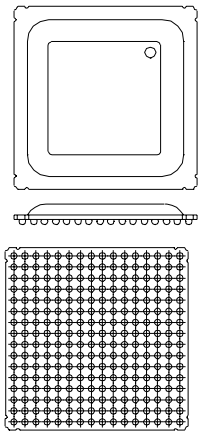
Thin Quad Flat Package
PW Suffix
208-Pin
Pin Pitch .5 mm
Case No. 998
28 X 28 X 1.6 mm



Thin Quad Flat Package
PV Suffix
144-Pin
Pin Pitch .5 mm
Case No. 918
20 X 20 X 1.5 mm



Plastic Ball Grid Array Package
GC Suffix
196-Pin
Ball Pitch 1 mm
Case No. 1128-01
15 X 15 X 1.5 mm



Plastic Ball Grid Array Package
GC Suffix
252-Pin
Ball Pitch 1.27 mm
Case No. 1205-1
21 X 21 X 2.85 mm

WISD Contacts

Support	Contact
Application Questions	dsphelp@dsp.sps.mot.com
Fax	(512) 895-7282
Technical Support	(800) 521-6274
Technical Support World Wide Web Site	http://www.mot.com/SPS/DSP/helpline/
Motorola DSP Tools World Wide Web Site	http://www.mot.com/SPS/WIRELESS/dsptools/
Motorola Wireless World Wide Web Site	http://www.mot.com/SPS/WIRELESS/
Motorola DSP World Wide Web Site	http://www.mot.com/SPS/DSP

DSP563xx Training Schedule

Date	Location
October 20 - 23	Indianapolis, IN
December 1 - 4	Indianapolis, IN
To register, call DSP Systems at (317) 274-4559, or visit the Motorola Technical Training Web site at: http://mot-sps.com/training	

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