M68MPB916Y3UM/D

March 1998

M68MPB916Y3

MCU PERSONALITY BOARD

USER’S MANUAL

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CHAPTER 1

GENERAL INFORMATION

1.1 INTRODUCTION

This manual provides general information, hardware preparation, installation instructions, a quick start guide, and support information for the M68MPB916Y3 MCU Personality Board (MPB). The MPB is one component of Motorola's modular approach to MC68HC16Y3 and MC68HC916Y3 Microcontroller Unit-based product development. This modular approach lets you easily configure our development systems to fit your requirements.

The MPB may be used in either the M68MMDS1632 Motorola Modular Development System (MMDS) or the M68MEVB1632 Modular Evaluation Board (MEVB). Alternately, you may install the MPB directly in your target system if the target system includes an modular active probe interconnect (MAPI) interface. The MCU device on the MPB defines which MCU is emulated/evaluated by the MMDS or MEVB. Both systems are invaluable tools for designing, debugging, and evaluating MCU operation of the M68HC16 and M68300 MCU Families. By providing the essential MCU timing and I/O circuitry, these systems simplify user evaluation of prototype hardware/software products.

MPB product includes:

- M68MPB916Y3 MCU Personality Board (MPB)
- Plastic overlay for use with the MEVB – pin outs for the logic analyzer connectors on the MPFB (specifically for the MC68HC916Y3 MCU)
- Documentation

1.2 SPECIFICATIONS

Table 1-1 lists MPB specifications.

Table 1-1. MPB Specifications

Characteristic	Specifications
On-Board Clock	Case style: 14 or 8-pin hybrid crystal clock oscillator (frequency as required by MCU).
External Clock	dc – 20.97 MHz (or maximum MCU allows).
MCU I/O ports	HCMOS compatible
Temperature Operating Storage	 0° to +40° C -40° to +85° C
Relative humidity	0 to 90% (non-condensing)
Power requirements	+5 Vdc ± 5% @ 500 mA (max.)
Dimensions MCU Personality Board	 3.25 x 3.25 in. (82.6 x 82.6 mm)

1.3 EQUIPMENT REQUIRED

The external requirements for MPB operation are either an MEVB or MMDS system. MMDS operation requirements are described in the M68MMDS1632 Motorola Modular Development System User’s Manual, M68MMDS1632/D. Operation requirements for the MEVB are described in this manual and the M68MPFB1632 Modular Platform Board User’s Manual, M68MPFB1632/D.

1.4 CUSTOMER SUPPORT

For information about a Motorola distributor or sales office near you call:

AUSTRALIA, Melbourne – (61-3)887-0711 Sydney – 61(2)906-3855 BRAZIL, Sao Paulo – 55(11)815-4200 CANADA, B. C., Vancouver – (604)606-8502 ONTARIO, Toronto – (416)497-8181 ONTARIO, Ottawa – (613)226-3491 QUEBEC, Montreal – (514)333-3300 CHINA, Beijing – 86-10-68437222 DENMARK – (45)43488393 FINLAND, Helsinki – 358-9-6824-400 FRANCE, Paris – 33134 635900 GERMANY, Langenhagen/Hannover – 49(511)786880 Munich – 49 89 92103-0 Nuremberg – 49 911 96-3190 Sindelfingen – 49 7031 79 710 Wiesbaden – 49 611 973050 HONG KONG, Kwai Fong – 852-6106888 Tai Po – 852-6668333 INDIA, Bangalore – (91-80)5598615 ISRAEL, Herzlia – 972-9-590222 ITALY, Milan – 39(2)82201	JAPAN, Fukuoka – 81-92-725-7583 Gotanda – 81-3-5487-8311 Nagoya – 81-52-232-3500 Osaka – 81-6-305-1802 Sendai – 81-22-268-4333 Takamatsu – 81-878-37-9972 Tokyo – 81-3-3440-3311 KOREA, Pusan – 82(51)4635-035 Seoul – 82(2)554-5118 MALAYSIA, Penang – 60(4)2282514 MEXICO, Mexico City – 52(5)282-0230 Guadalajara – 52(36)21-8977 PUERTO RICO, San Juan – (809)282-2300 SINGAPORE – (65)4818188 SPAIN, Madrid – 34(1)457-8204 SWEDEN, Solna – 46(8)734-8800 SWITZERLAND, Geneva – 41(22)799 11 11 Zurich – 41(1)730-4074 TAIWAN, Taipei – 886(2)717-7089 THAILAND, Bangkok – 66(2)254-4910 UNITED KINGDOM, Aylesbury – 441(296)395-252 UNITED STATES, Phoenix, AZ – 1-800-441-2447

For a list of the Motorola sales offices and distributors:

http://www.mcu.motsps.com/sale_off.html

CHAPTER 2

HARDWARE PREPARATION AND INSTALLATION

2.1 INTRODUCTION

This chapter provides unpacking instructions, hardware preparation information, and installation instructions for the MPB.

When you unpack the MPB from its shipping carton, verify that all items are in good condition. Save packing material for storing and shipping the MPB.

NOTE

Should the MPB arrive damaged, save all packing material, and contact the carrier's agent.

2.2 HARDWARE PREPARATION

This portion of the manual explains how to prepare the MPB before use, as well as how to configure the MPB for system operation. MPB installation in the MMDS and MEVB are also described.

The MPB has been factory tested and is shipped with installed jumpers. A jumper installed on a jumper header provides a connection between two points in the MPB circuit. There are two types of jumper headers on the MPB: three-pin and two-pin with a cut-trace short. A cut-trace short has a copper trace between the feed-through holes (bottom or solder side of the MPB). Table 2-1 describes each type of jumper header.

There are five jumper headers on the MPB (Table 2-2 is a quick reference guide for the jumper headers). These jumper headers may be re-configured to customize MPB functionality. The following paragraphs are a detailed description of each jumper header function. There is also an insertion point (E1) for connecting an external ground. Figure 2-1 shows the location of the MPB jumper headers and the insertion point.

NOTE

Verify that all socketed parts are seated in their sockets.

CAUTION

Depending on the application, it may be necessary to cut the wiring trace short (cut-trace short) on W2. Be careful not to cut adjacent PCB wiring traces or too deep on the multi-layer circuit board.

NOTE

If the cut-trace short on a jumper header is cut, a user-supplied fabricated jumper must be installed on the jumper header to return the MPB to its default setting.

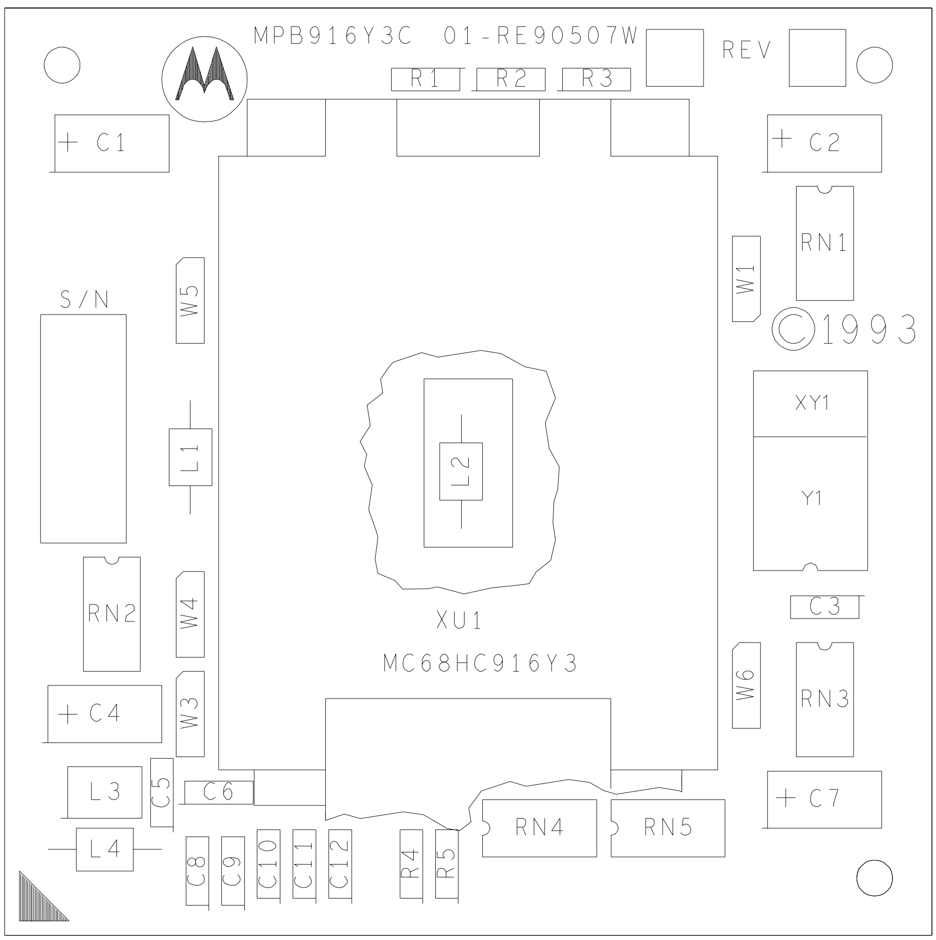


Figure 2-1. MPB Jumper Headers and Insertion Point Location Diagram (top view)

Table 2-1. Jumper Header Types

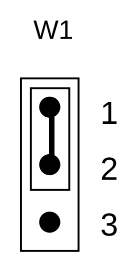
Jumper Header Type	Symbol	Description
two-pin with cut-trace short		Two-pin jumper header with cut-trace short, designated as WX (X = the jumper header number). After removing the cut-trace short, use a fabricated jumper to return the jumper header to its factory default state.
three-pin		Three-pin jumper header, designated as WX (X = the jumper header number). Use a fabricated jumper to create a short between two of the three pins of the jumper header.

Table 2-2. MPB Jumper Header Descriptions

Jumper Header	Type	Description
W1	1 2 3	Jumper between pins 1 and 2 (factory default); selects the MPB on-board crystal clock source. Jumper between pins 2 and 3; selects an external clock source as the MCU EXTAL input signal.
W2	1 2	Jumper installed or cut-trace short intact (factory default); selects the on-board VDDA power source. No jumper or cut-trace short; use an external power source by connecting an external power source to W2 pin 2. **NOTE** Jumper header W2 is not populated by the factory.
W3	1 2 3	Jumper installed on pins 1 and 2 (factory default); selects the MPB on-board VRH power source. Jumper installed on pins 2 and 3; selects external VRH power source.
W4	1 2 3	Jumper installed on pins 1 and 2 (factory default); selects the MPB on-board VRL power source. Jumper installed on pins 2 and 3; selects external VRL power source.
W5	1 2 3	Jumper installed on pins 1 and 2 (factory default); selects the MCU-internal phase-lock-loop frequency synthesizer as the system clock. Jumper installed on pins 2 and 3; selects the EXTAL input as the system clock. The MCU-internal phase-lock-loop frequency synthesizer is disabled.
W6	1 2 3	Jumper installed on pins 1 and 2 (factory default); selects an MC68HC916Y3 MCU as the MCU type for this MPB. Jumper installed on pins 2 and 3; selects an MC68HC16Y3 MCU as the MCU type for this MPB.

2.2.1 Clock Select Header (W1)

Jumper header W1 connects the MCU external clock (EXTAL) pin to either an on-board or external (target system) clock source. The drawing below shows the factory configuration: fabricated jumper on pins 1 and 2. This configuration selects the MPB on-board clock source; crystal oscillator in socket at located Y1. (This crystal provides for operation at the maximum rate the MCU allows via the internal phase-locked loop or direct clock input.) When the MPB is installed in the active probe or directly on a target system and the target system clock is used as the MPB clock, move the fabricated jumper to W1 pins 2 and 3. This connects the MCU EXTAL pin to the MAPI bus input pin. The frequency of the external clock signal can be from dc to 20.97 MHz (or to the maximum the MCU allows).

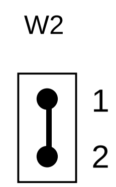


NOTE

You can not drive the MPB clock circuit from an external source (target system) with a discrete crystal. If a target system clock source is used to drive the MPB clock circuit, always use a logic driven clock such as a hybrid oscillator.

2.2.2 VDDA Select Header (W2)

Jumper header W2 selects the MPB VDDA power source; either MPB power (VDDI) or an external source. The drawing below shows the factory configuration: cut-trace short on pins 1 and 2. This configuration connects filtered VDDI to VDDA. To use an external power source, remove the cut-trace short from W2 pins 1 and 2. Then connect the external power source to W2 pin 2. Removal of the cut-trace short isolates the MCU VDDA pin from the other MPB circuitry. Isolation lets you connect a precision VDDA source for accurate 10-bit analog/digital (A/D) generation. When connecting an external VDDA power supply to the MPB connect the power supply ground to insertion point E1. For more information on A/D generation refer to the Analog-To-Digital Converter Reference Manual, ADCRM/AD.



NOTES

If the cut-trace short has been cut, a fabricated jumper must be installed on W2 to return it to the factory configuration.

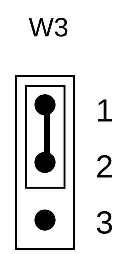
Jumper header W2 is not populated by the factory.

2.2.3 Voltage Reference High Select Header (W3)

Jumper header W3 selects the voltage reference high (VRH) source; either MPB power (VDDA) or an external VRH source. The drawing below shows the factory configuration: fabricated jumper on pins 1 and 2. This configuration selects VDDA as the VRH source. To use an external VRH source, first place the fabricated jumper on W3 pins 2 and 3. Then connect the MCU VRH pin to the external VRH source. Each configuration defines which method is best when connecting the MCU VRH pin to the external VRH source:

- •**MPB/MPFB –** connect via the MPFB logic analyzer connector (refer to Chapter 4 for the appropriate logic analyzer pin)
- •**MPB/MMDS1632 –** connect via the VRH pin of the target MCU socket
- •**MPB/Target System –** connect via the VRH pin of the target system MAPI bus

Alternately, you may remove the jumper and wire-wrap directly to W3 pin 2. Connecting directly to pin 2 is an option regardless of the configuration.

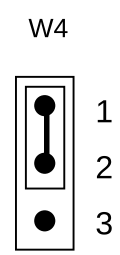


2.2.4 Voltage Reference Low Select Header (W4)

Jumper header W4 selects the voltage reference low (VRL) source; either MPB power (VSSA) or an external VRL source. The drawing below shows the factory configuration: fabricated jumper on pins 1 and 2. This configuration selects VSSA as the VRL source. To use an external VRL source, first place the fabricated jumper on W4 pins 2 and 3. Then connect the MCU VRL pin to the external VRL source. Each configuration defines which method is best when connecting the MCU VRL pin to the external VRL source:

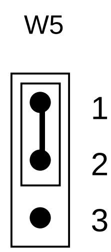
- •**MPB/MPFB –** connect via the MPFB logic analyzer connector (refer to Chapter 4 for the appropriate logic analyzer pin)
- •**MPB/MMDS1632 –** connect via the VRL pin of the target MCU socket
- •**MPB/Target System –** connect via the VRL pin of the target system MAPI bus

Alternately, you may remove the jumper and wire-wrap directly to W4 pin 2. Connecting directly to pin 2 is an option regardless of the configuration.



2.2.5 MCU Clock Source Select Header (W5)

Jumper header W5 selects the MCU clock; either the MCU-internal phase-lock-loop frequency synthesizer or the EXTAL input. The drawing below shows the factory configuration: fabricated jumper on pins 1 and 2. This configuration selects the MCU-internal phase-lock-loop frequency synthesizer as the clock. To use the EXTAL input as the clock, place the fabricated jumper on 2 and 3.



NOTE

J14 pin-4 and W16 on the MPFB are marked MODCLK, but this signal, when using an M68HC916Y3, is FASTREF. The M68HC916Y3 MEVB overlay is correct and marked FASTREF. Use W16 on the MPFB to select the MCU PLL clock input speed.

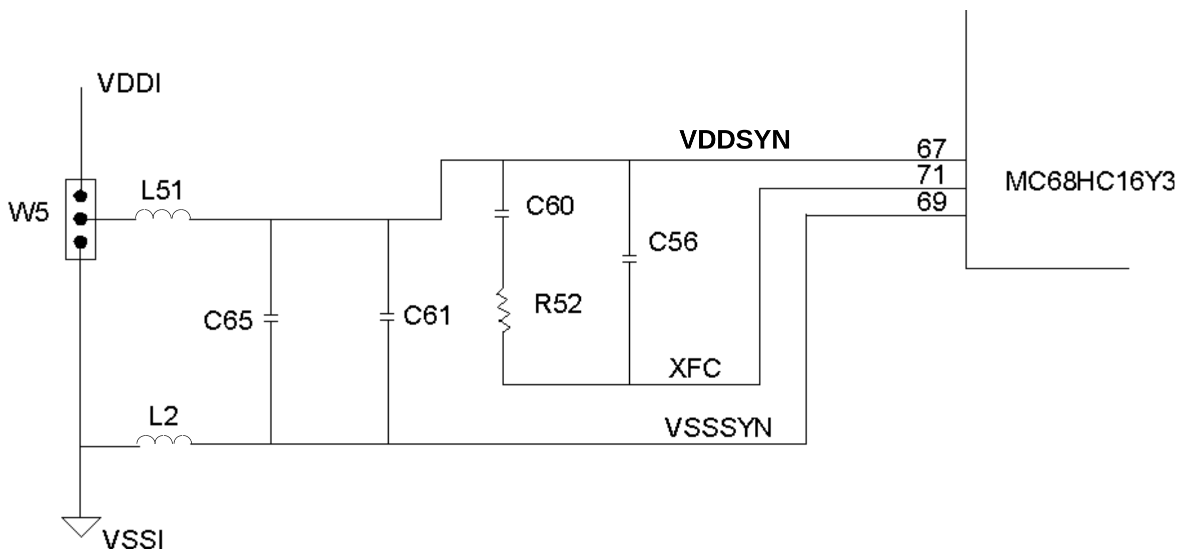
2.2.6 Using a 32 KHz Clock

The factory installed crystal oscillator in location Y1 is rated at 4.194 megahertz. You may change Y1 to change the clock speed of the MPB. The only other oscillator you may install is 32 kilohertz. If you change Y1 to the slower value (32 KHz) you must replace the following capacitors and resistor (see diagram below):

C60 – 1 µf

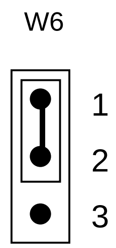
C56 – 1 µf

R52 – 18 kΩ



2.2.7 MCU ID Code Select Header (W6)

Jumper header W6 selects the MCU ID code; either the M68HC16Y3 MCU or M68HC916Y3 MCU. The drawing below shows the factory configuration: fabricated jumper on pins 1 and 2. Use this configuration when an M68HC16Y3 MCU is installed on the MPB. To use the MPB with an M68HC916Y3 MCU installed, place the fabricated jumper on 2 and 3.



NOTE

These jumper settings only apply to when using the M68HC916Y3 MPB in an MMDS1632.

2.2.8 VSSA Insertion Point (E1)

Insertion point E1 is a plate through hole that lets you connect an external ground to the MPB VSSA pin (refer to paragraph 2.2.2). Insert an external ground wire in E1 and solder it into the plate through hole.

NOTE

Insertion point E1 is not populated by the factory.

2.3 MEVB CONFIGURATION

The MEVB contains:

- MPB – MCU-device-specific board that defines the MCU to be evaluated.
- M68MPFB1632 Modular Platform Board (MPFB) – which provides the interface connections to the host computer, logic analyzer connections, and the platform for installing the MPB. For more information about the MPFB and MEVB system connections refer to the M68MPFB1632 Modular Platform Board User's Manual, M68MPFB1632/D. Chapter 3 of this manual contains information to help you get started using your MEVB.

CAUTION

Turn OFF MPFB power when installing the MPB on the MPFB or removing the MPB from the MPFB. Sudden power surges could damage MEVB integrated circuits.

To install the MPB on the MPFB (refer to Figure 2-2):

1. Inspect all connectors for bent or damaged pins.
2. Align the MPB reference mark with the MPFB reference mark.
3. Rotate the MPB until the four MAPI bus connectors on its bottom mate with the MAPI bus connectors on the top of the MPFB. (There is only one way to connect the MPB and the MPFB.)
4. Firmly press the MPB onto the MPFB.

CAUTION

Support the bottom side of MPFB when installing the MPB on the MPFB. Excessive flexing of the MPFB could damage the printed circuit.

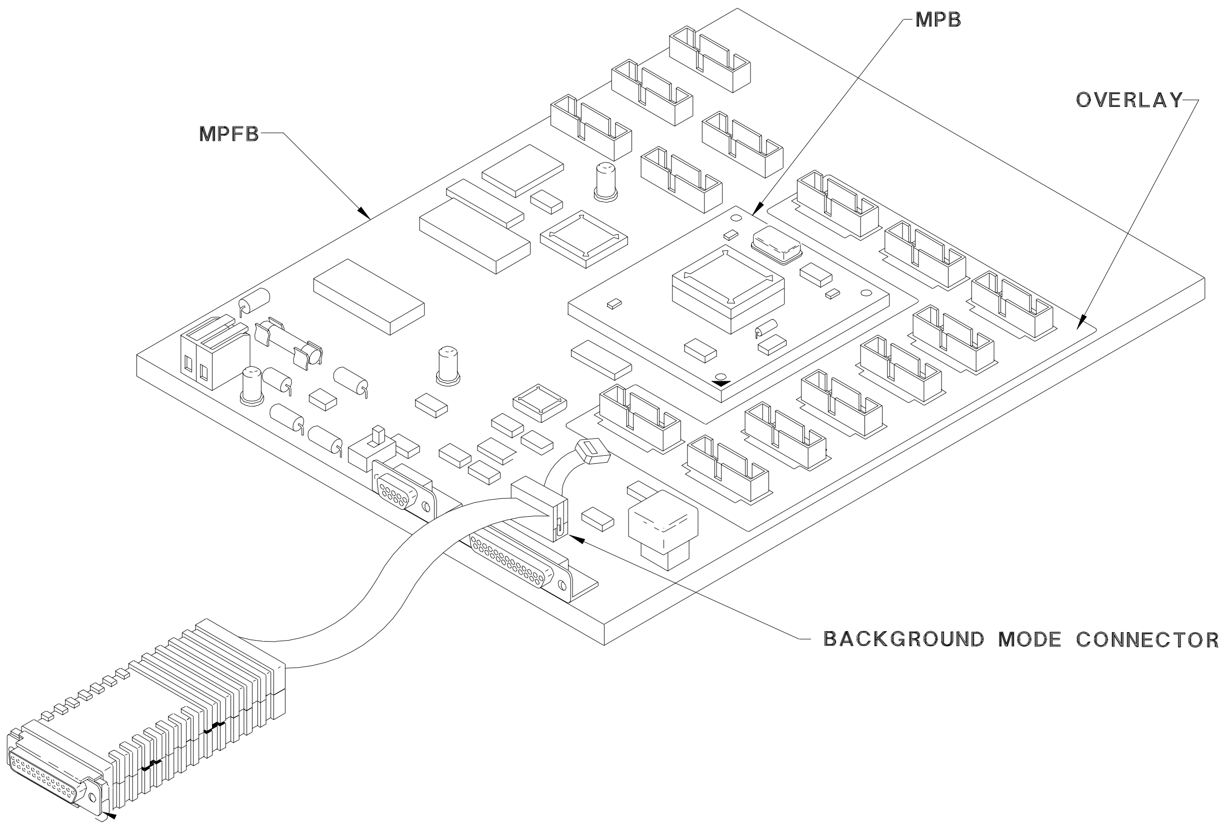


Figure 2-2. MPB – MPFB Interconnection (with SDI interface connector)

After you have installed the MPB, install the plastic overlay on the MPFB: place the overlay over logic analyzer connectors J12 through J20 and press down. Holes in the overlay slide down over plastic clips on the MPFB. These clips hold the overlay in place.

2.4 MPB – MMDS INSTALLATION

The M68MMDS1632 Motorola Modular Development System (MMDS) consists of the station module and an active probe. The active probe consists of a three board set, two cables, and a box:

- MPB – MCU-device-specific board that defines the MCU to be evaluated.
- Enhanced Target Control Board (TCB) – the interface between the MPB, target system, and the station module. The TCB must be purchased separately. For more information about the TCB refer to the MMDS1632 Motorola Modular Development System User's Manual, MMDS1632UM/D.
- Package Personality Board (PPB) – the board that connects the active probe to the target system. The PPB must be purchased separately. For more information about the PPB refer to the appropriate PPB configuration guide.
- Active probe cables (2) – the interface between the active probe and the station module. 01-RE90340W01 REV 0 and 01-RE90341W01 REV 0 are printed on the active probe cables. The active probe cables come with the TCB. For more information about the active probe cables refer to the MMDS1632 Motorola Modular Development System User's Manual, MMDS1632UM/D.
- Active probe box – the protective enclosure for the TCB.

CAUTION

Turn off MMDS and target system power when installing or removing MMDS components. Sudden power surges could damage MMDS and target system integrated circuits.

To configure an active probe (refer to Figure 2-3):

1. Inspect all connectors for bent or damaged pins.
2. Rotate the MPB until the four MAPI bus connectors on its bottom mate with the MAPI bus connectors on the top of the TCB. (There is only one way to connect the MPB and the TCB.) Firmly press the MPB and the TCB together.
3. Rotate the PPB until the four MAPI bus connectors on its top mate with the MAPI bus connectors on the bottom of the TCB. (There is only one way to connect the PPB and the TCB.) Firmly press the PPB and the TCB together.

4. Connect one end of the 01-RE90341W01 REV 0 active probe cable to connector P6 on the MMDS control board; connect the other end to connector J6 on the TCB. Connect one end of the 01-RE90340W01 REV 0 active probe cable to connector P5 on the MMDS control board; connect the other end to connector J5 on the TCB. Secure the connector clamps on TCB connectors J5 and J6.

The active probe is now ready to connect to the target system (refer to the PPB configuration guide for information on connecting the active probe to the target system.)

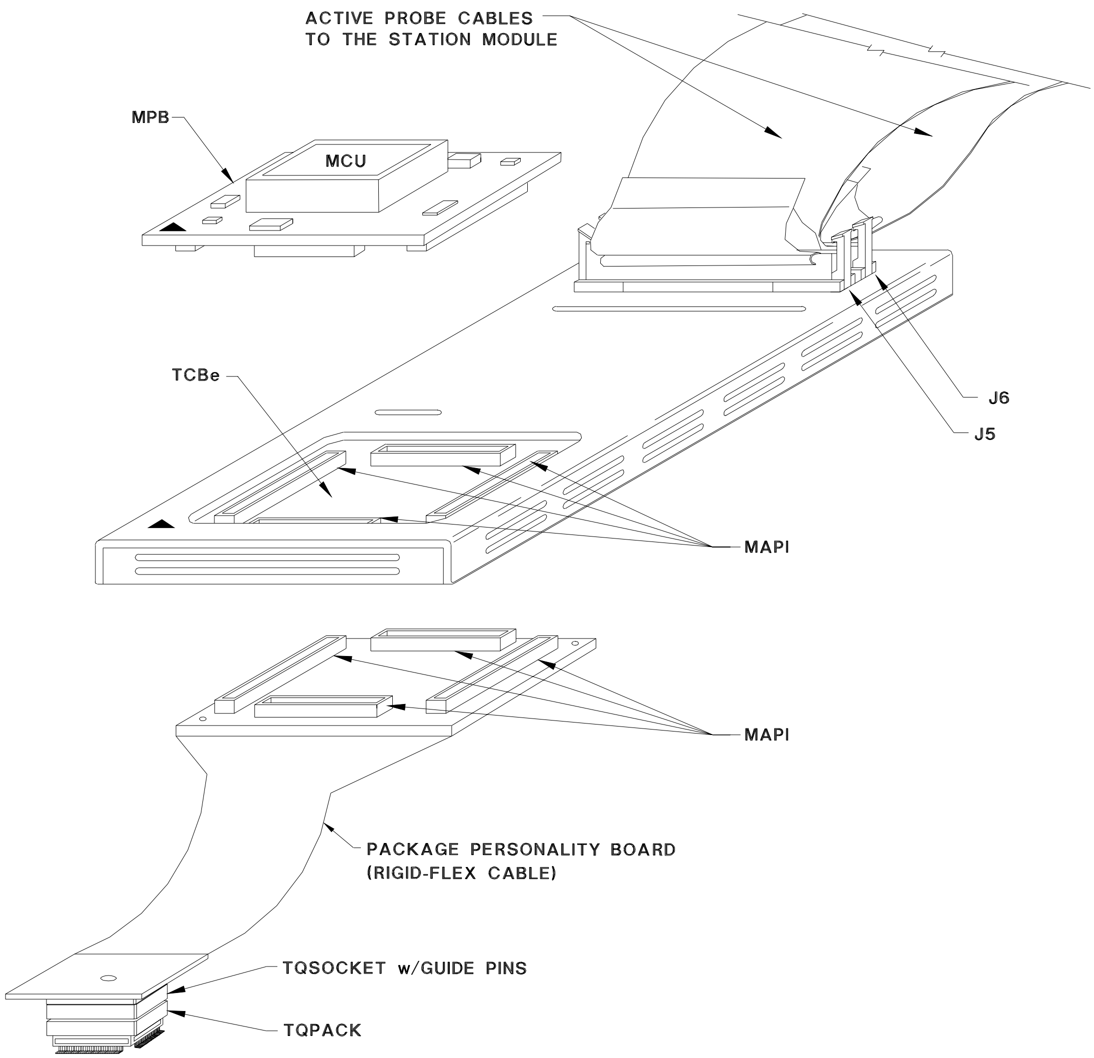


Figure 2-3. Active Probe Interconnection (with Active Probe Box)

CHAPTER 3

MEVB QUICK START GUIDE

3.1 INTRODUCTION

This quick start guide is intended for the user who may not be familiar with Motorola's development tools. This chapter explains the MEVB hardware and software set-up for M68MEVB916Y3 operation. Hardware set-up consists of configuring the MPB and MPFB jumper headers. While software set-up consists of installing and running the appropriate macro script file within the debugger.

For the purpose of this quick start guide the MPB jumper headers should be configured in their default positions. Chapter 2 of this manual contains the default jumper header settings for the MPB.

3.2 CONFIGURING THE MPFB

The MPFB includes jumper-selectable options such as chip select usage, memory type selection and memory size selection for the pseudo ROM sockets, and reset data control.

3.2.1 MPFB Memory Devices

Pseudo ROM refers to memory locations U2 & U4. The two pseudo ROM sockets provide a generic memory socket, and accepts a variety of RAM, EPROM, or EEPROM devices. The pseudo ROM sockets, as shipped from the factory, contain two 32K x 8 RAM devices. These memory are 28-pin package devices.

3.2.2 MPFB Jumper Headers

Configure your MPFB jumper headers per the instructions in Table 3-1. Table 3-1 contains information exclusively intended for quick start and ignores the other jumper headers.

Table 3-1. MPFB Quick Start Jumper Header Configuration

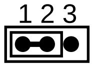
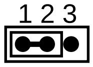
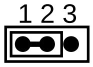
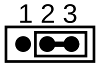
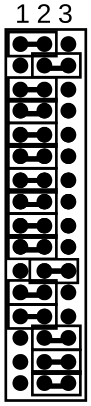
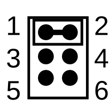
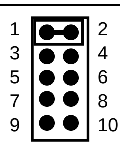
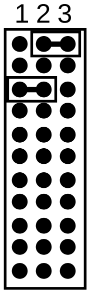
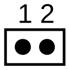
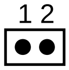
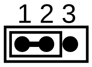
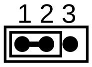
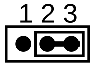
Jumper Header	Type	Description
W2	1 2 3 	Install a jumper on pins 1 and 2 to configure pin 1 of the memory devices in the pseudo ROM sockets (U2 & U4) as a standard address line.
W3	1 2 3 	Install a jumper on pins 1 and 2 to indicate that the memory devices in the pseudo ROM sockets (U2 & U4) have 28-pins.
W4	1 2 3 	Install a jumper on pins 1 and 2 to set the pseudo ROM port size (memory data width) as word.
W5	1 2 3 	Install a jumper on pins 2 and 3 to enable the PRU.
W6	1 2 3 	W6 selects the MCU operation mode. Each 3-pin jumper header set corresponds to an MCU data line. While the reset pin is low, the reset data values are driven on the data bus (D0 – D15). (The MEVB reset data circuit is open drain; a high state is provided via a pull-up resistor.) Each reset data line may be set high (H) or low (L). Consult the appropriate MCU user's manual, data book, or technical summary for reset data information.
W10		Install a jumper on pins 1 and 2 to indicate that RAM is installed in the pseudo ROM sockets (U2 & U4).
W12		Install a jumper on pins 3 and 4 to indicate that the two devices installed in the pseudo ROM sockets (U2 & U4) are 32K x 8.

Table 3-1. MPFB Quick Start Jumper Header Configuration (continued)

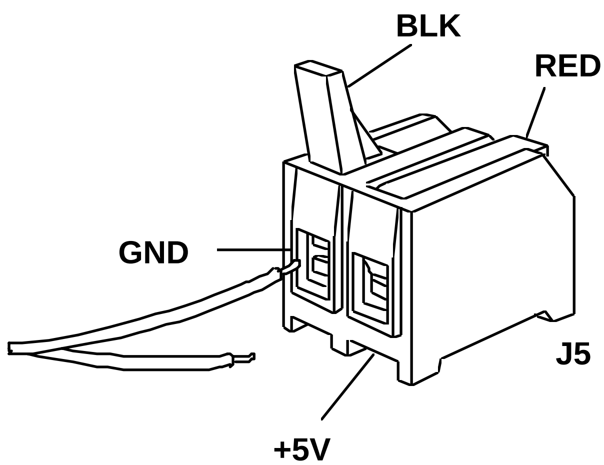
Jumper Header	Type	Description
W14	1 2 3 	Jumper header W14 selects the MCU signal for the memory devices in the fast RAM sockets (U9 & U10) and pseudo ROM sockets (U2 & U4). Pins 1 and 2 select the MCU chip select for the memory devices in the fast RAM sockets. While pins 2 and 3 of jumper header W14 select the chip select for the memory devices in the pseudo ROM sockets. Jumper installed on CSBOOT pins 2 and 3 (factory default); use CSBOOT as the memory device chip enable for memory devices in the pseudo ROM sockets.
W16	1 2 	No jumper installed; the MCU FASTREF signal is pulled high (logic 1) via a resistor during reset. **NOTE** J14 pin-4 and W16 on the MPFB are marked MODCLK, but this signal, when using an M68HC16Y3, is FASTREF. The M68HC16Y3 MEVB overlay is correct and marked FASTREF. Use W16 on the MPFB to select the MCU PLL clock input speed.
W17	1 2 	No jumper installed; the BERR signal is pulled high (logic 1) via a resistor during reset.
W18	1 2 3 	Install a jumper on pins 1 and 2 for unrestricted writes to the memory devices in the pseudo ROM sockets (U2 & U4).
W19	1 2 3 	Install a jumper on pins 1 and 2 to ground the A19 signal to the MPFB memory arrays.
W22	1 2 3 	Install a jumper on pins 2 and 3 to select the evaluation MCU (on the MPB) as an M68HC16 MCU device.

3.3 MEVB INSTALLATION INSTRUCTIONS

MEVB installation requires a user-supplied power supply and host computer. The host computer must have a parallel port and must run MS-DOS, as required by ICD16. The following paragraphs explain MPFB connections. Refer to Chapter 2 for instructions to interconnect the MPB and MPFB.

3.3.1 Power Supply – MPFB Connection

Use MPFB connector J5 to connect a user-supplied power supply to the MEVB. Contact 1 is ground; black lever. Contact 2 is VDD (+5 volts); red lever. Use 20 or 22 AWG wire for power connections. For each wire, trim back the insulation 1/4 in. (.635 cm), lift the appropriate lever of J5 to release tension on the contacts, then insert the bare wire into J5 and close the lever. The MEVB requires a +5Vdc @ 1.0 amp power supply for operation. A 1.5 amp fuse is installed on the MPFB +5Vdc power supply input line.



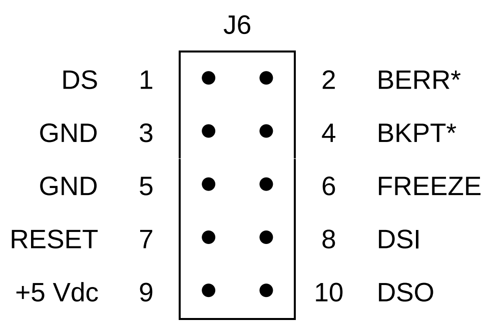
CAUTIONS

Do not use wire larger than 20 AWG in connector J5. Such wire could damage the connector.

Turn off MEVB power when installing or removing the MPB from the MPFB. Sudden power surges could damage MEVB integrated circuits.

3.3.2 Personal Computer – BDM Connection

Personal computer communication with the MEVB requires background debug mode (BDM) hardware. Connect your BDM hardware between your computer's I/O port and the BDM header on the MPFB (MPFB connector J6). The drawing below shows signal assignments for connector J6. For additional information about your BDM software/hardware, including debugging and assembly information, see the appropriate user's manual.



3.4 SOFTWARE INSTALLATION

After you have set up the MEVB hardware you must install the software on your computer. Follow the installation procedure in the appropriate software operations manual.

The MCU must be initialized before the MEVB will function. The following is one possible initialization for the MPB16Y3. You may adapt this example to your debugger. This initialization enables the maximum system clock frequency and disables the software watchdog while enabling the bus monitor. CSBOOT is set to zero-wait state and the block size set to 64K starting at $00000. The SRAM is enabled to reside at $10000 with the stack pointer initialized at $103FE and the instruction pointer (IP) initialized to $00200 (PK=0, IP=200).

Load your program at address $00200.

Below is the MPBY3.ICD initialization macro program listing.

```
symbol SCIMCR FFA00
symbol SYNCR FFA04
symbol CSBARBT FFA48
symbol CSORBT FFA4A
symbol START 00200
dmmw SCIMCR 40CF       Set module mapping to $FFF000-$FFFFFF
dmmw SYNCR B000        Set system clock frequency to 16.78 MHz
watchdog               Disable the watcdog timer
dmmw CSBARBT 0003      Change CSBOOT block size to 64K
dmmw CSORBT 7830       Change wait state to zero
mdf6 START             Display program in PMM window
pk=0                   Initialize CPU registers
a=AA
b=BB
e=0000
ix=0000
iy=0000
iz=0000
hr=0000
ir=0000
k=0000
sp=03fe                Initialize the stack pointer
sk=1
symbol RAMBAH FFB04
symbol RAMMCR FFB00
dmmw RAMBAH 0001       Set SRAM base address
dmmb RAMMCR 00         Enable SRAM array
dmml 10000 4D6F746F    Check SRAM: write Motorola 68HC16 advanced MCUs
dmml 10004 726F6C61
dmml 10008 20363848
dmml 1000C 43313620
dmml 10010 41647661
dmml 10014 6E636564
dmml 10018 20204D43
dmml 1001C 55732020
dmml 10020 36384843
mdf3 10000             Display SRAM in DMM window
ip=START               Start entering your program here
```

CHAPTER 4
MEVB SUPPORT INFORMATION

4.1 INTRODUCTION

The information in this chapter is relevant when the MPB is used in an MEVB (the MPB installed on a MPFB). Signals on the MPFB logic analyzer connectors are defined by the MPB type. The tables of this chapter describe MPFB logic analyzer connector signals when an M68MPB9916Y3 is installed on the MPFB. The signal descriptions on J12 – J20 are the logic analyzer pin-outs on the plastic overlay supplied with the MPB.

NOTE

The signal descriptions in the following tables are for quick reference only. The MC68HC916Y3 User's Manual, MC68HC916Y3UM/AD, contains a complete description of the MC68HC916Y3 MCU signals.

Also contained in this chapter are MAPI bus interface layout and pin assignments information for MPB connectors P1, P2, P3, and P4.

Tables 4-1 through 4-14 list pin assignments for MPFB connectors J7 through J20.

Table 4-1.	Logic analyzer connector J7
Table 4-2.	Logic analyzer connector J8
Table 4-3.	Logic analyzer connector J9
Table 4-4.	Logic analyzer connector J10
Table 4-5.	Logic analyzer connector J11
Table 4-6.	Logic analyzer connector J12
Table 4-7.	Logic analyzer connector J13

Table 4-8.	Logic analyzer connector J14
Table 4-9.	Logic analyzer connector J15
Table 4-10.	Logic analyzer connector J16
Table 4-11.	Logic analyzer connector J17
Table 4-12.	Logic analyzer connector J18
Table 4-13.	Logic analyzer connector J19
Table 4-14.	Logic analyzer connector J20

Table 4-1. Logic Analyzer Connector J7 Pin Assignments

Pin	Mnemonic	Signal
1, 2	SPARE	No connection
3	OE(ALL)	I/O PRU OUTPUT ENABLE – Input, active high; when low disables all PRU outputs.
4 – 11	PEPAR7 – PEPAR0	PEPAR OUTPUTS – Output signals that show the complement (negated contents) of the PEPAR register.
12 – 19	PE7 – PE0	PORT E I/O SIGNALS – PRU replacement of the Port E function.
20	GND	GROUND

Table 4-2. Logic Analyzer Connector J8 Pin Assignments

Pin	Mnemonic	Signal
1, 2	SPARE	No connection
3	OE(ABG)	I/O PRU OUTPUT ENABLE – Input, active high; when low disables port A, port B, and port G outputs.
4 – 11	PA7 – PA0	PORT A I/O SIGNALS – PRU replacement of the Port A function.
12 – 19	PB7 – PB0	PORT B I/O SIGNALS – PRU replacement of the Port B function.
20	GND	GROUND

Table 4-3. Logic Analyzer Connector J9 Pin Assignments

Pin	Mnemonic	Signal
1, 2	SPARE	No connection
3	OE(H)	I/O PRU OUTPUT ENABLE – Input, active high; when low disables the port H outputs.
4 – 11	PH7 – PH0	PORT H I/O SIGNALS – PRU replacement of the Port H function.
12 – 19	PG7 – PG0	PORT G I/O SIGNALS – PRU replacement of the Port G function.
20	GND	GROUND

Table 4-4. Logic Analyzer Connector J10 Pin Assignments

Pin	Mnemonic	Signal
1	+5V	+5 VDC POWER – Input voltage (+5 Vdc @ 1.0 A) used by the MEVB logic circuits. (To make this pin no connection, remove the jumper from header on the MPFB.)
2	SPARE	No connection
3	AS	ADDRESS STROBE – Active-low output signal that indicates whether a valid address is on the address bus.
4 – 19	A15 – A0	ADDRESS BUS BITS 15 – 0 – Sixteen bits of the 24-bit address bus.
20	GND	GROUND

Table 4-5. Logic Analyzer Connector J11 Pin Assignments

Pin	Mnemonic	Signal
1	+5V	+5 VDC POWER – Input voltage (+5 Vdc @ 1.0 A) used by the MEVB logic circuits. (To make this pin no connection, remove the jumper from header on the MPFB.)
2	SPARE	No connection
3	DS	DATA STROBE – Active-low output signal. During a read cycle, indicates that an external device should place valid data on the data bus. During a write cycle, indicates that valid data is on the data bus.
4 – 19	D15 – D0	DATA BUS 15 – 0 – 16 bits of the MCU bi-directional data bus lines.
20	GND	GROUND

Table 4-6. Logic Analyzer Connector J12 Pin Assignments

Pin	Mnemonic	Signal
1, 2	SPARE	No connection
3	CLKOUT	SYSTEM CLOCK OUT – Output signal that is the MCU internal system clock.
4	BERR	BUS ERROR – Active-low signal that indicates that a memory access error has occurred.
5	BKPT / DSCLK	BREAKPOINT – Active-low input signal that signals a hardware breakpoint to the CPU. Development Serial Clock – Clock input signal for the background debug mode.
6	FREEZE QUOT	FREEZE – Output signal that indicates the CPU has acknowledged a breakpoint. QUOTIENT OUT – Output signal that furnishes the quotient bit of the polynomial divider for test purposes.
7	LAT-DSO / (Latched IPIPE0)	LATCHED INSTRUCTION PIPE 0 – Latched output signal of the first state of IPIPE0 for CPU16-based MCUs; indicates instruction pipeline activity.

Table 4-6. Logic Analyzer Connector J12 Pin Assignments (continued)

Pin	Mnemonic	Signal
8	LAT-DSI (Latched IPIPE1)	LATCHED INSTRUCTION PIPE 1 – Latched output signal of the first state of IPIPE1 for CPU16-based MCUs; indicates instruction pipeline activity.
9	DSO / (IPIPE0)	DEVELOPMENT SERIAL OUT – Serial data output signal for background debug mode. INSTRUCTION PIPE 0 for CPU16-based MCUs.
10	DSI / (IPIPE1)	DEVELOPMENT SERIAL IN – Serial data input signal for background debug mode. INSTRUCTION PIPE 1 for CPU16-based MCUs.
11	DSACK1	DATA AND SIZE ACKNOWLEDGE 1 – Active-low input signal that allows asynchronous data transfers and dynamic bus sizing between the MCU and external devices.
12	DSACK0	DATA AND SIZE ACKNOWLEDGE 0 – Active-low input signal that allows asynchronous data transfers and dynamic bus sizing between the MCU and external devices.
13	FC2 / CS5	FUNCTION CODE 2 – Output signal that identifies the processor state and address space of the current bus cycle. CHIP SELECT 5 – Output signal that selects peripheral or memory devices at programmed addresses.
14	FC1	FUNCTION CODE 1 – Output signal that identifies the processor state and address space of the current bus cycle.
15	FC0 / CS3	FUNCTION CODE 0 – Output signal that identifies the processor state and address space of the current bus cycle. CHIP SELECT 3 – Output signal that selects peripheral or memory devices at programmed addresses.
16	SIZ1	TRANSFER SIZE – Active-high output signals that Indicates the number of bytes to be transferred during a bus cycle.
17	SIZ0	TRANSFER SIZE 0 – Active-high output signals that Indicates the number of bytes to be transferred during a bus cycle.

Table 4-6. Logic Analyzer Connector J12 Pin Assignments (continued)

Pin	Mnemonic	Signal
18	R/W	READ/WRITE – Active-high output signal that indicates the direction of data transfer on the bus.
19	BGACK /	BUS GRANT ACKNOWLEDGE – Active-low input signal that indicates that an external device has assumed bus mastership.
	CSE	EMULATOR CHIP SELECT – Output signal that selects external emulation devices at internally-mapped addresses. CSE is used to emulate I/O ports.
20	GND	GROUND

Table 4-7. Logic Analyzer Connector J13 Pin Assignments

Pin	Mnemonic	Signal
1	+5V	+5 VDC POWER – Input voltage (+5 Vdc @ 1.0 A) used by the MEVB logic circuits. (To make this pin no connection, remove the jumper from header on the MPFB.)
2	SPARE	No connection
3	DSACK1	DATA AND SIZE ACKNOWLEDGE 1 – Active-low input signal that allows asynchronous data transfers and dynamic bus sizing between the MCU and external devices.
4	PULL-UP	Not connected; pulled high through a resistor on the MPB.
5	HALT	HALT – Active-low input/output signal that suspends external bus activity, to request a retry when used with BERR, or for single-step operation.
6	AS	ADDRESS STROBE – Active-low output signal that indicates that a valid address is on the address bus.
7	DS	DATA STROBE – Active-low output signal. During a read cycle, indicates that an external device should place valid data on the data bus. During a write cycle, indicates that valid data is on the data bus.

Table 4-7. Logic Analyzer Connector J13 Pin Assignments (continued)

Pin	Mnemonic	Signal
8	BR /	BUS REQUEST – Active-low input signal that indicates that an external device requires bus mastership.
	CS0	CHIP SELECT 0 – Output signal that selects peripheral or memory devices at programmed addresses.
9	BG /	BUS GRANT – Active-low output signal that indicates that the MCU has relinquished the bus.
	CSM	INTERNAL MODULE CHIP SELECT – Active-low output signal that selects external emulation devices at internally-mapped addresses. CSM is used to emulate memory.
10	CSBOOT	BOOT CHIP SELECT – An active-low output chip select for external boot startup ROM
11	CLKOUT	SYSTEM CLOCK OUTPUT – MCU internal clock output signal.
12	A23 /	ADDRESS BUS BIT 23 – One bit of the 24-bit address bus.
	CS10	CHIP SELECT 10 – Output signal that selects peripheral or memory devices at programmed addresses.
13	A22 /	ADDRESS BUS BIT 22 – One bit of the 24-bit address bus.
	CS9	CHIP SELECT 9 – Output signal that selects peripheral or memory devices at programmed addresses.
14	A21 /	ADDRESS BUS BIT 21 – One bit of the 24-bit address bus.
	CS8	CHIP SELECT 8 – Output signal that selects peripheral or memory devices at programmed addresses.
15	A20 /	ADDRESS BUS BIT 20 – One bit of the 24-bit address bus.
	CS7	CHIP SELECT 7 – Output signal that selects peripheral or memory devices at programmed addresses.
16	A19 /	ADDRESS BUS BIT 19 – One bit of the 24-bit address bus.
	CS6	CHIP SELECT 6 – Output signal that selects peripheral or memory devices at programmed addresses.
17 – 19	A18 – A16	ADDRESS BUS 18 – 16 – Three bits of the 24-bit address bus.
20	GND	GROUND

Table 4-8. Logic Analyzer Connector J14 Pin Assignments

Pin	Mnemonic	Signal
1, 2	SPARE	No connection
3	DSACK0	DATA AND SIZE ACKNOWLEDGE 0 – Active-low input signal that allows asynchronous data transfers and dynamic bus sizing between the MCU and external devices.
4	FASTREF	FASTREF – Selection of crystal or clock input frequency driven into the VCO for generation of the MCU system clock. 1=fast reference, 0=slow reference
5	TSC	THREE STATE CONTROL – When TSC is logic high, this input signal forces all output drivers to a high-impedance state.
6	RESET	RESET – Active-low, bi-directional signal to start a system reset.
7	PULL-UP	Not connected; pulled high through a resistor on the MPB.
8	SPARE	No connection
9 – 15	IRQ1 – IRQ7	TARGET INTERRUPT REQUEST 1 – 7 - Active-low input signals from the target that asynchronously provides an interrupt priority level to the CPU. IRQ1 has the lowest priority, IRQ7 has the highest.
16 – 19	SPARE	No connection
20	GND	GROUND

Table 4-9. Logic Analyzer Connector J15 Pin Assignments

Pin	Mnemonic	Signal
1 – 3	SPARE	No connection
4 – 13	GND	GROUND
14	PCLK	AUXILIARY TIMER CLOCK INPUT – External input clock source for the GPT.
15	PWMB	PULSE WIDTH MODULATION B – Repetitive output signals whose high time to low time ratio can be controlled by the CPU.
16	PWMA	PULSE WIDTH MODULATION A – Repetitive output signals whose high time to low time ratio can be controlled by the CPU.
17	PAI	PULSE ACCUMULATOR INPUT – Input signal that increments an 8-bit counter.
18, 19	SPARE	No connection
20	GND	GROUND

Table 4-10. Logic Analyzer Connector J16 Pin Assignments

Pin	Mnemonic	Signal
1 – 4	SPARE	No connection
5	IC1	INPUT CAPTURE 1 – Input signal that latches the contents of the GPT timer counter (TCNT) into the input capture register TIC1 when a selected edge occurs at the pin.
6	IC2	INPUT CAPTURE 2 – Input signal that latches the contents of the GPT timer counter (TCNT) into the input capture register TIC2 when a selected edge occurs at the pin.
7	IC3	INPUT CAPTURE 3 – Input signal that latches the contents of the GPT timer counter (TCNT) into the input capture register TIC3 when a selected edge occurs at the pin.
8	OC1	OUTPUT COMPARE 1 – Output signal that is generated when the GPT timer counter (TCNT) and TOC1 comparator register contain the same value.

Table 4-10. Logic Analyzer Connector J16 Pin Assignments (continued)

Pin	Mnemonic	Signal
9	OC2	OUTPUT COMPARE 2 – Output signal that is generated when the GPT timer counter (TCNT) and TOC2 comparator register contain the same value.
10	OC3	OUTPUT COMPARE 3 – Output signal that is generated when the GPT timer counter (TCNT) and TOC3 comparator register contain the same value.
11	OC4	OUTPUT COMPARE 4 – Output signal that is generated when the GPT timer counter (TCNT) and TOC4 comparator register contain the same value.
12	IC4 /	INPUT CAPTURE 4 – Input signal that latches the contents of the GPT timer counter (TCNT) into the input capture register TIC4 when a selected edge occurs at the pin.
	OC5	OUTPUT COMPARE 5 – Output signal that is generated when the GPT timer counter (TCNT) and TOC5 comparator register contain the same value.
13 – 19	SPARE	No connection
20	GND	GROUND

Table 4-11. Logic Analyzer Connector J17 Pin Assignments

Pin	Mnemonic	Signal
1 – 4	SPARE	No connection
5	VSSA	A/D GROUND – A/D ground reference.
6 – 11	AN5 – AN0	ANALOG TO DIGITAL CONVERSION 5 -0 – Analog input lines to the MCU device.
12	VRH	VOLTAGE REFERENCE HIGH – Input reference supply voltage (high) line (must set jumper on the MPB).
13	VRL	VOLTAGE REFERENCE LOW – Input reference supply voltage (low) line (must set jumper on the MPB).
14, 15	AN6, AN7	ANALOG TO DIGITAL CONVERSION 6 and 7 – Analog input lines to the MCU device.

Table 4-11. Logic Analyzer Connector J17 Pin Assignments (continued)

Pin	Mnemonic	Signal
16	VSSA	A/D GROUND – A/D ground reference.
17 – 19	SPARE	No connection
20	VSSA	A/D GROUND – A/D ground reference.

Table 4-12. Logic Analyzer Connector J18 Pin Assignments

Pin	Mnemonic	Signal
1 – 4	SPARE	No connection
5	PCS0 / SS	PERIPHERAL CHIP SELECT 0 – Active-low output SPI peripheral chip select signal. SLAVE SELECT – Bi-directional, active-low signal that initiates serial transmission when SPI is in slave mode; causes mode fault in master mode.
6	MOSI	MASTER-IN, SLAVE-OUT – Serial input to SPI in master mode; serial output from SPI in slave mode.
7	MISO	MASTER-OUT, SLAVE-IN – Serial output from SPI in master mode; serial input to SPI in slave mode.
8	SCK	SPI SERIAL CLOCK – In master mode, the clock signal from the SPI; in slave mode the clock signal to the SPI.
9	TXDA	TRANSMIT DATA A – Serial data output line to serial communication interface A.
10	RXDA	RECEIVE DATA A – Serial data input line to serial communication interface A.
11	TXDB	TRANSMIT DATA B– Serial data output line to serial communication interface B.
12	RXDB	RECEIVE DATA B – Serial data input line to serial communication interface B.
13 – 16	TPU0 – TPU3	TIME PROCESSOR UNIT CHANNELS – TPU input/output channels.
17 – 19	SPARE	No connection
20	GND	GROUND

Table 4-13. Logic Analyzer Connector J19 Pin Assignments

Pin	Mnemonic	Signal
1 – 4	SPARE	No connection
5 – 12	TPU4 – TPU11	TIME PROCESSOR UNIT CHANNELS – TPU input/output channels..
13 – 19	SPARE	No connection
20	GND	GROUND

Table 4-14. Logic Analyzer Connector J20 Pin Assignments

Pin	Mnemonic	Signal
1 – 4	SPARE	No connection
5 – 8	GND	GROUND
9	PCS2	PERIPHERAL CHIP SELECT 2 – Active-low output SPI peripheral chip select signal.
10	PCS1	PERIPHERAL CHIP SELECT 1 – Active-low output SPI peripheral chip select signal.
11 – 13	GND	GROUND
14	T2CLK	TPU CLOCK – External input clock source to the TPU.
15 – 18	TPU15 – TPU12	TIME PROCESSOR UNIT CHANNELS – TPU input/output channels.
19	SPARE	No connection
20	GND	GROUND

CHAPTER 5
MAPI SUPPORT INFORMATION

5.1 INTRODUCTION

The information in this chapter is relevant when the MPB is to be installed on a target system. The figures in this chapter show the MAPI interface connector layout and pin assignments for MPB connectors P1, P2, P3, and P4.

The connectors required to interface to the MAPI bus are:

2	Robinson Nugent	2 X30 plugs	P50L-060P-AS-TGF
2	Robinson Nugent	2 X40 plugs	P50L-080P-AS-TGF

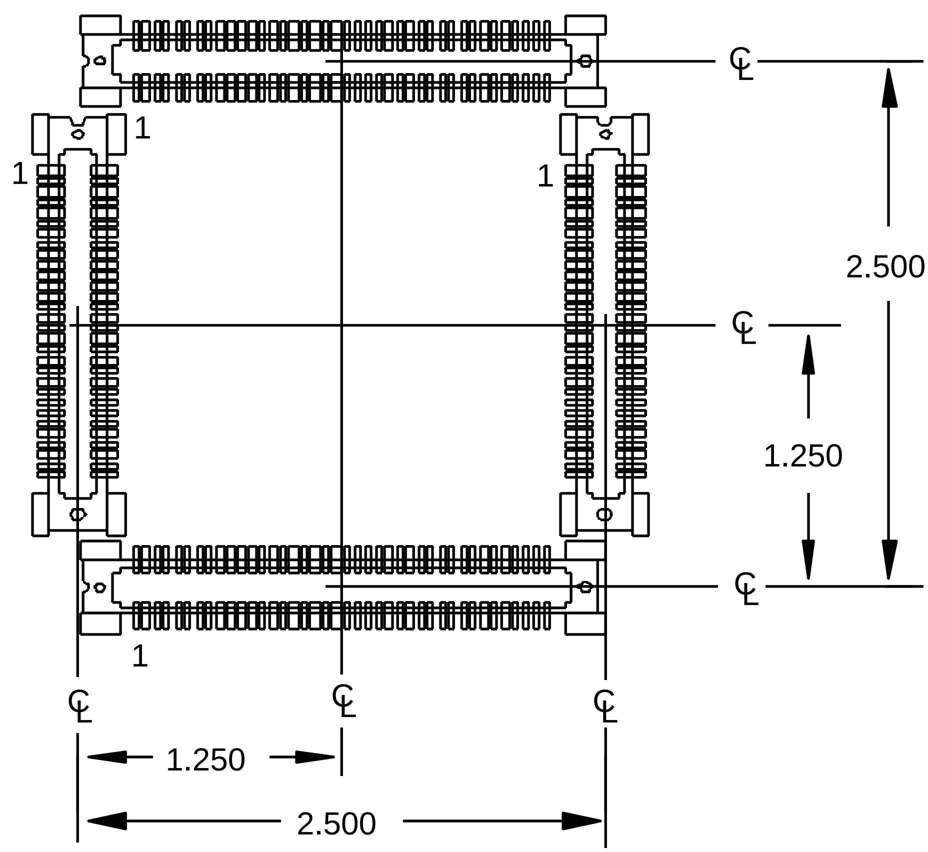


Figure 5-1. MAPI Interface Connector Layout

VRH	1	2	VSSA
VRL	3	4	VSSA
AN6	5	6	VSSA
AN7	7	8	VSSA
VSSA	9	10	VSSA
IC1	11	12	GND
IC2	13	14	GND
IC3	15	16	GND
OC1	17	18	GND
OC2	19	20	GND
OC3	21	22	GND
OC4	23	24	GND
IC4/OC5	25	26	GND
PAI	27	28	GND
PWMA	29	30	GND
PWMB	31	32	GND
PCLK	33	34	GND
GND	35	36	GND
GND	37	38	GND
GND	39	40	GND
GND	41	42	GND
GND	43	44	GND
GND	45	46	GND
GND	47	48	GND
GND	49	50	GND
GND	51	52	GND
GND	53	54	GND
A23 / CS10	55	56	GND
A22 / CS9	57	58	GND
A21 / CS8	59	60	GND
A20 / CS7	61	62	GND
A19 / CS6	63	64	GND
FC2 / CS5	65	66	GND
FC1	67	68	GND
FC0 / CS3	69	70	GND
BGACK / CSE	71	72	GND
BG / CSM	73	74	GND
BR / CS0	75	76	GND
CSBOOT	77	78	GND
+5V	79	80	VPP1

Figure 5-2. MAPI Interface Connector P1 Pin Assignments

Signal	Pin	Pin	Signal
VSSA	1	2	AN0
VSSA	3	4	AN1
VSSA	5	6	AN2
VSSA	7	8	AN3
VSSA	9	10	AN4
VSSA	11	12	AN5
VSSA	13	14	VSSA
GND	15	16	GND
No Connect	17	18	+5V
GND	19	20	GND
A1	21	22	A2
A3	23	24	A4
A5	25	26	A6
A7	27	28	A8
A9	29	30	GND
A10	31	32	A11
A12	33	34	A13
A14	35	36	A15
A16	37	38	A17
A18	39	40	GND
No Connect	41	42	+5V
GND	43	44	GND
GND	45	46	PCS0/SS
GND	47	48	MOSI
GND	49	50	MISO
GND	51	52	SCK
GND	53	54	TXDA
GND	55	56	RXDA
GND	57	58	TXDB
GND	59	60	RXDB

Figure 5-3. MAPI Interface Connector P2 Pin Assignments

Signal	Pin	Pin	Signal
GND	1	2	TPU0
GND	3	4	TPU1
GND	5	6	TPU2
GND	7	8	TPU3
GND	9	10	TPU4
GND	11	12	TPU5
GND	13	14	TPU6
GND	15	16	TPU7
GND	17	18	TPU8
GND	19	20	TPU9
GND	21	22	TPU10
GND	23	24	TPU11
GND	25	26	TPU12
GND	27	28	TPU13
GND	29	30	TPU14
GND	31	32	TPU15
GND	33	34	T2CLK
GND	35	36	GND
GND	37	38	GND
GND	39	40	GND
GND	41	42	PCS1
GND	43	44	PCS2
GND	45	46	GND
GND	47	48	GND
GND	49	50	GND
GND	51	52	GND
GND	53	54	VSTBY
GND	55	56	DSO / IPIPE0
GND	57	58	DSI / IPIPE1
GND	59	60	HALT
GND	61	62	RESET
GND	63	64	BERR
GND	65	66	BKPT / DSCLK
GND	67	68	TSC
GND	69	70	FREEZE
GND	71	72	GND
EXTAL	73	74	GND
GND	75	76	CLKOUT
GND	77	78	GND
+5V	79	80	+5V

Figure 5-4. MAPI Interface Connector P3 Pin Assignments

Signal	Pin	Pin	Signal
+5V	1	2	+5V
GND	3	4	D0
D1	5	6	D2
D3	7	8	D4
D5	9	10	D6
D7	11	12	GND
D8	13	14	D9
D10	15	16	D11
D12	17	18	D13
D14	19	20	D15
GND	21	22	GND
A0	23	24	GND
DSACK0	25	26	GND
DSACK1	27	28	GND
PULL-UP	29	30	GND
PULL-UP	31	32	GND
DS	33	34	GND
AS	35	36	GND
SIZ0	37	38	GND
SIZ1	39	40	GND
R/W	41	42	GND
FASTREF	43	44	GND
IRQ1	45	46	GND
IRQ2	47	48	GND
IRQ3	49	50	GND
IRQ4	51	52	GND
IRQ5	53	54	GND
IRQ6	55	56	GND
IRQ7	57	58	GND
+5V	59	60	VPP4

Figure 5-5. MAPI Interface Connector P4 Pin Assignments

CHAPTER 6
SCHEMATIC DIAGRAMS

6.1 INTRODUCTION

This chapter contains the M68MPB916Y3 MCU Personality Board (MPB) schematic diagrams. These schematic diagrams are for reference only and may deviate slightly from the circuits on your MPB.

TABLE OF CONTENTS

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED
	O	ORIGINAL RELEASE	02/11/94	L.H.
	A	ADDED PULLUPS TO PCS1* & PCS2*	11/15/94	B.B.

DRAWN BY: L.H.	DATE: 02/11/94
DESIGN ENGINEER: L.H.	DATE: 02/11/94
PROJECT LEADER: L.H.	DATE: 02/11/94

MOTOROLA INC.

MICROPROCESSOR AND MEMORY TECHNOLOGIES GROUP

6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA

TITLE: SCHEMATIC - MPB16Y3C

SIZE		DWG. NO.	REV:
A	GEDTTL: BOARD GEDABV: MPB16Y3C	63ASE90507W	A

LAST_MODIFIED=Tue Nov 15 17:58:05 1994

SHEET 1 OF 8

DWG. NO. 63ASE90507W REV: A

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS, 5%, 1/8 WATT.
   ALL CAPACITORS ARE IN UF. 50V.
   ALL VOLTAGES ARE DC.
2. INTERRUPTED LINES CODED WITH THE SAME LETTER OR LETTER COMBINATIONS ARE ELECTRICALLY CONNECTED.
3. (△) DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH THE MANUFACTURER.
4. SPECIAL SYMBOL USAGE:
   * DENOTES - ACTIVE LOW SIGNAL.
   <> DENOTES - VECTORED SIGNALS.
5. INTERPRET DIAGRAM IN ACCORDANCE WITH AMERICAN NATIONAL STANDARDS INSTITUTE SPECIFICATIONS, CURRENT REVISION, WITH THE EXCEPTION OF LOGIC BLOCK SYMBOLOGY.
6. (△) CODE FOR SHEET TO SHEET REFERENCES IS AS FOLLOWS:

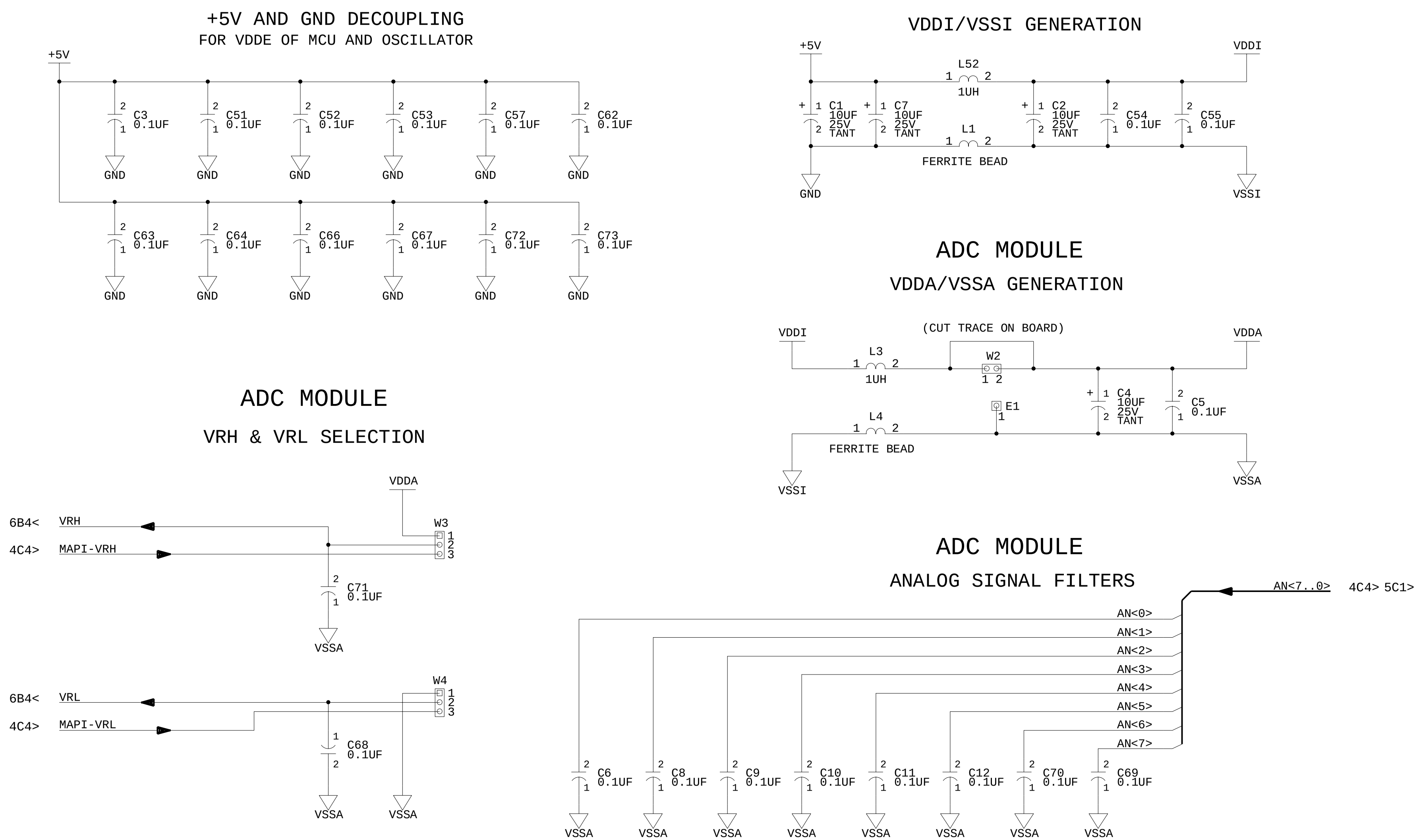
```
        5  C7  < >
SHEET --'  /    \ `-- OUTPUT
ZONE  ----'      `--- INPUT
```

7. VCC LOCATIONS
   UNLESS OTHERWISE SPECIFIED, VCC IS APPLIED TO:
   PIN 8 OF ALL 8-PIN ICS
   PIN 14 OF ALL 14-PIN ICS
   PIN 16 OF ALL 16-PIN ICS
   PIN 20 OF ALL 20-PIN ICS, ETC.
8. GROUND LOCATIONS
   UNLESS OTHERWISE SPECIFIED, GROUND IS APPLIED TO:
   PIN 4 OF ALL 8-PIN ICS
   PIN 7 OF ALL 14-PIN ICS
   PIN 8 OF ALL 16-PIN ICS
   PIN 10 OF ALL 20-PIN ICS, ETC.

NOTES

SIZE		DWG. NO.	REV:
A	GEDTTL: BOARD GEDABV: MPB16Y3C	63ASE90507W	A
LAST_MODIFIED=Tue Nov 15 18:04:33 1994		SHEET 2 OF 8	

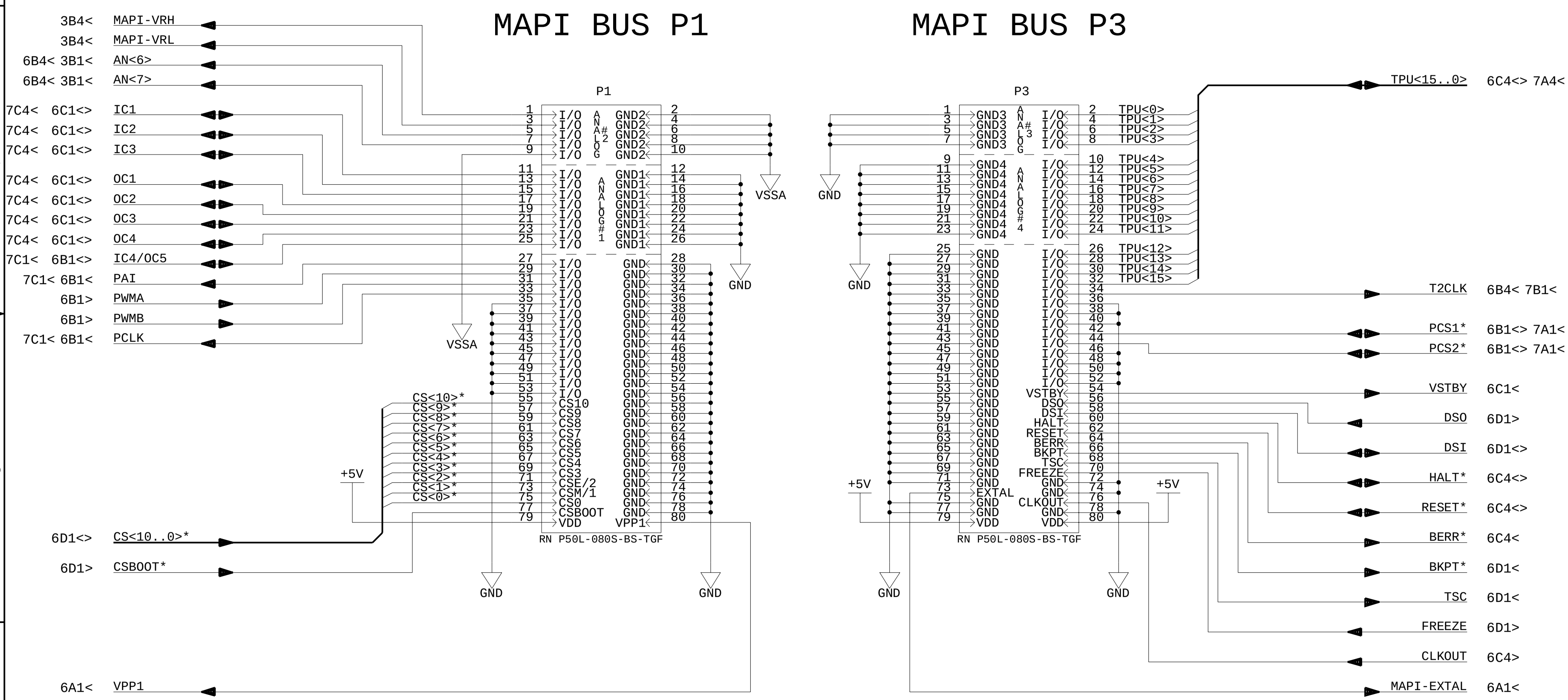
DWG. NO. 63ASE90507W REV: A



BYPASS CAPACITORS, CLEAN POWER & SIGNAL FILTERS

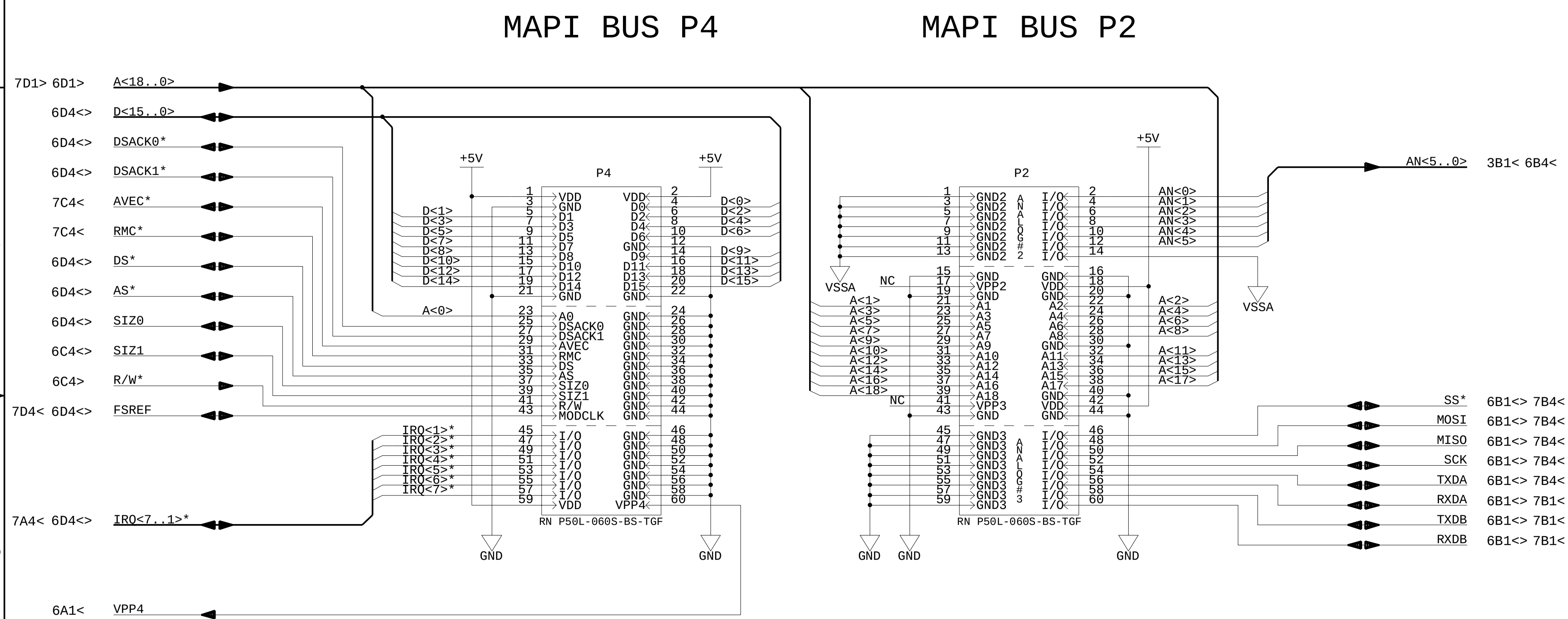
SIZE	GEDTTL: BOARD	DWG. NO.	REV:
A	GEDABV: MPB16Y3C	63ASE90507W	A
LAST_MODIFIED=Thu Nov 17 10:06:11 1994		SHEET 3 OF 8	

DWG. NO. 63ASE90507W REV: A



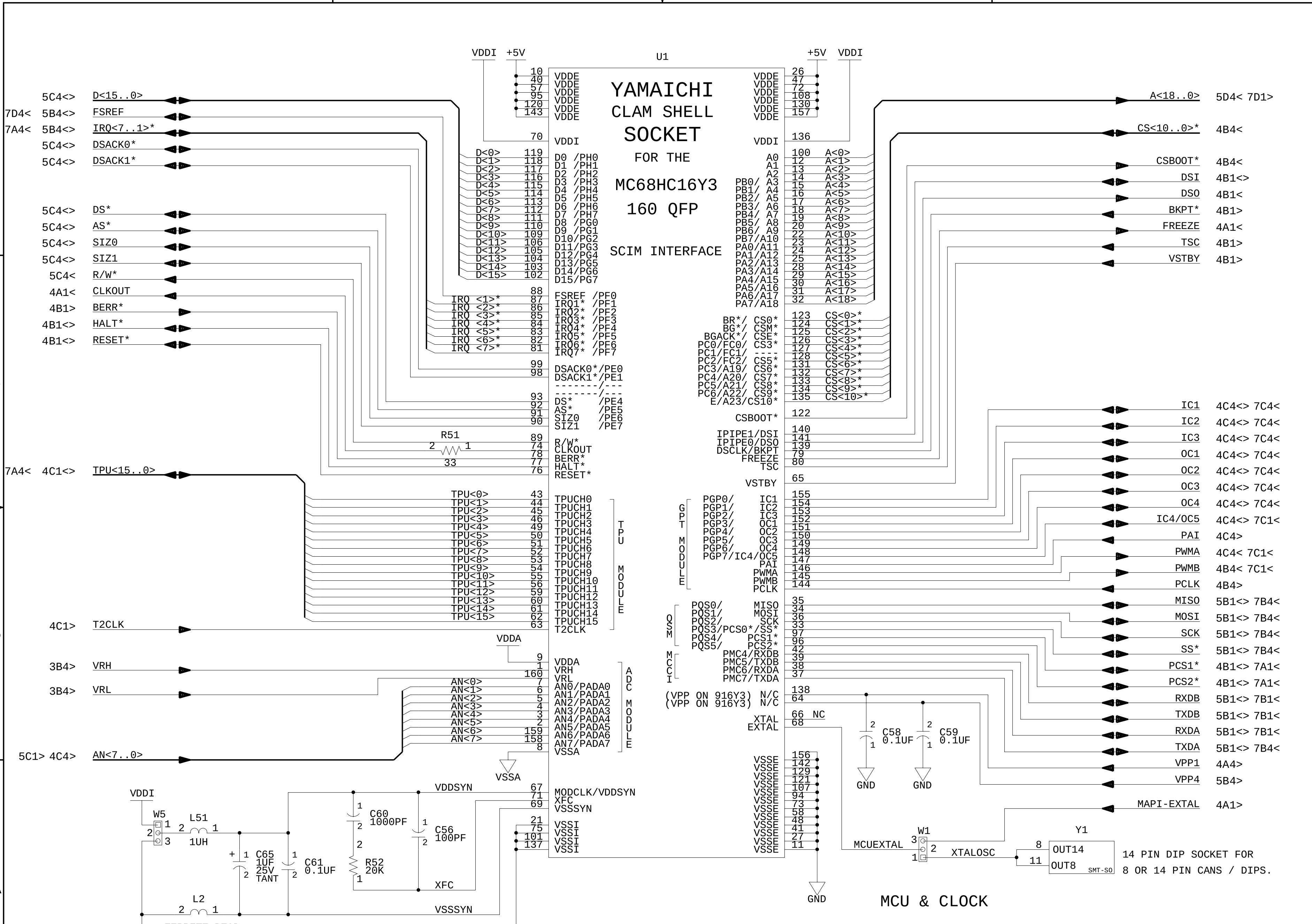
MODULAR ACTIVE PROBE INTERCONNECT P1 & P3

SIZE A	GEDTTL: BOARD	DWG. NO. 63ASE90507W	REV: A
	GEDABV: MPB16Y3C		
LAST_MODIFIED=Thu Nov 17 10:06:14 1994		SHEET 4 OF 8	



MODULAR ACTIVE PROBE INTERCONNECT P2 & P4

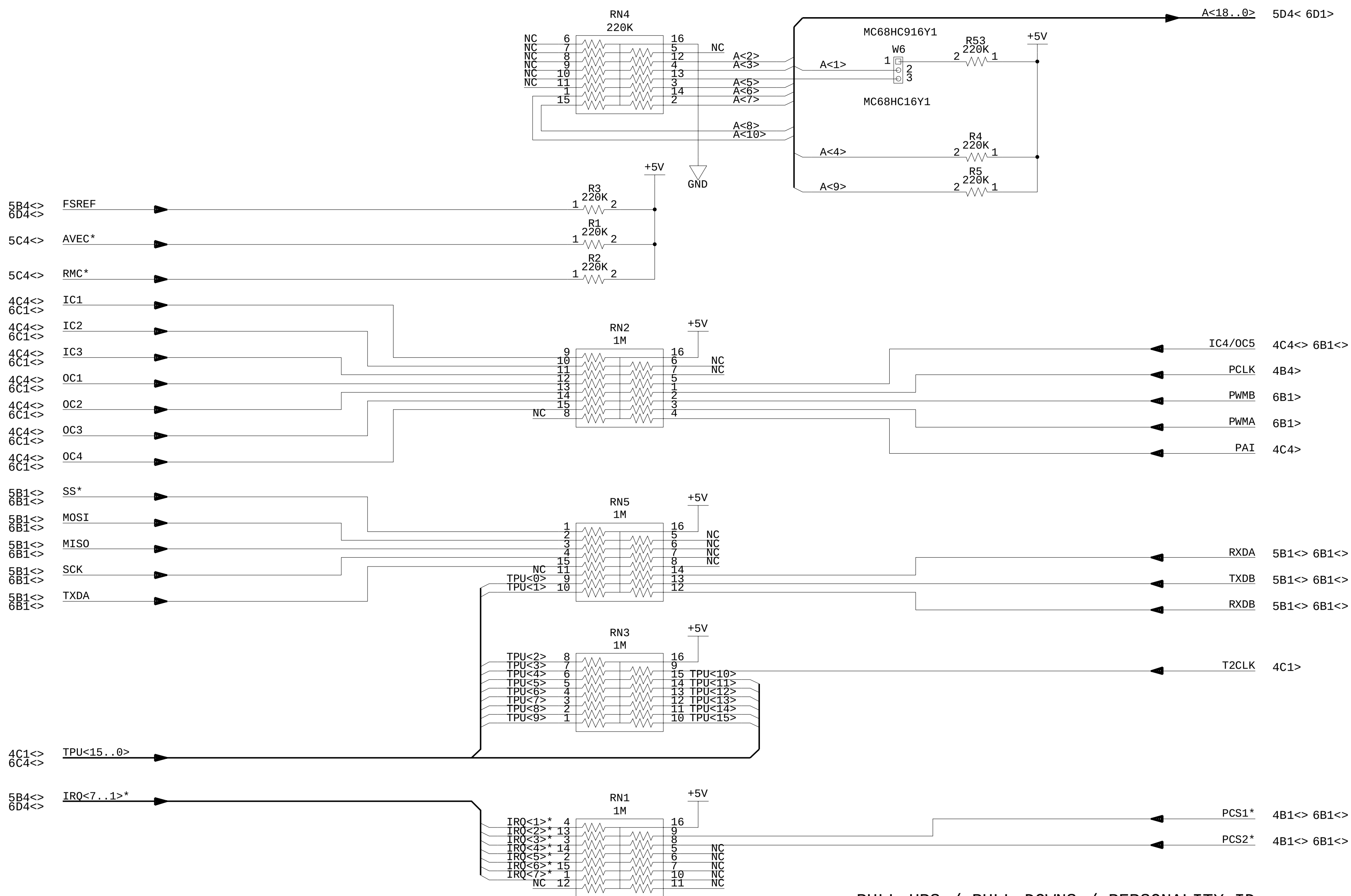
SIZE	GEDTTL: BOARD	DWG. NO.	REV:
A	GEDABV: MPB16Y3C	63ASE90507W	A
LAST_MODIFIED=Thu Nov 17 10:06:18 1994		SHEET 5 OF 8	



NOTE: 1) PLACE THE CAP BETWEEN VDDSYN & XFC AS CLOSE TO MCU PINS AS POSSIBLE.

SIZE	GEDTTL: BOARD	DWG. NO.	REV:
A	GEDABV: MPB16Y3C	63ASE90507W	A
LAST_MODIFIED=Thu Nov 17 10:06:22 1994		SHEET 6 OF 8	

MCU PERSONALITY CODE: MC68HC16Y1=108HEX & MC68HC916Y1=109HEX
(USING A<10..1>)



PULL-UPS / PULL-DOWNS / PERSONALITY ID

SIZE	GEDTTL: BOARD	DWG. NO.	REV:
A	GEDABV: MPB16Y3C	63ASE90507W	A
LAST_MODIFIED=Thu Nov 17 10:06:24 1994		SHEET 7 OF 8	

```
*** Signal Cross-Reference ***
   --- for the entire design --

A <18..0>       5D4< 6D1> 7D1>
AN <7..0>       3B1< 4C4> 5C1> 6B4<
AS *            5C4<> 6D4<>
AVEC *          5C4<> 7C4<
BERR *          4B1> 6C4<
BKPT *          4B1> 6D1<
CLKOUT          4A1< 6C4>
CS <10..0> *    4B4< 6D1<>
CSBOOT *        4B4< 6D1>
D <15..0>       5C4<> 6D4<>
DS *            5C4<> 6D4<>
DSACK0 *        5C4<> 6D4<>
DSACK1 *        5C4<> 6D4<>
DSI             4B1<> 6D1<>
DSO             4B1< 6D1>
FREEZE          4A1< 6D1>
FSREF           5B4<> 6D4<> 7D4<
HALT *          4B1<> 6C4<>
IC1             4C4<> 6C1<> 7C4<
IC2             4C4<> 6C1<> 7C4<
IC3             4C4<> 6C1<> 7C4<
IC4/OC5         4C4<> 6B1<> 7C1<
IRQ <7..1> *    5B4<> 6D4<> 7A4<
MAPI-EXTAL      4A1> 6A1<
MAPI-VRH        3B4< 4C4>
MAPI-VRL        3B4< 4C4>
MISO            5B1<> 6B1<> 7B4<
MOSI            5B1<> 6B1<> 7B4<
OC1             4C4<> 6C1<> 7C4<
OC2             4C4<> 6C1<> 7C4<
OC3             4C4<> 6C1<> 7C4<
OC4             4C4<> 6C1<> 7C4<
PAI             4C4> 6B1< 7C1<
PCLK            4B4> 6B1< 7C1<
PCS1 *          4B1<> 6B1<> 7A1<
PCS2 *          4B1<> 6B1<> 7A1<
PWMA            4C4< 6B1> 7C1<
PWMB            4B4< 6B1> 7C1<
R/W *           5C4< 6C4>
RESET *         4B1<> 6C4<>
RMC *           5C4<> 7C4<
RXDA            5B1<> 6B1<> 7B1<
RXDB            5B1<> 6B1<> 7B1<
SCK             5B1<> 6B1<> 7B4<
SIZ0            5C4<> 6D4<>
SIZ1            5C4<> 6C4<>
SS *            5B1<> 6B1<> 7B4<
T2CLK           4C1> 6B4< 7B1<
TPU <15..0>     4C1<> 6C4<> 7A4<
TSC             4B1> 6D1<
TXDA            5B1<> 6B1<> 7B4<
```

```
TXDB            5B1<> 6B1<> 7B1<
VPP1            4A4> 6A1<
VPP4            5B4> 6A1<
VRH             3B4> 6B4<
VRL             3B4> 6B4<
VSTBY           4B1> 6C1<
```

SIGNAL CROSS REFERENCES

SIZE	GEDTTL: BOARD	DWG. NO.	REV:
A	GEDABV: MPB16Y3C	63ASE90507W	A
LAST_MODIFIED=Tue Nov 15 18:03:45 1994		SHEET 8 OF 8	

DWG. NO. 63ASE90507W REV: A