MOTOROLA

Semiconductor Products Sector
Application Note

Order this document
by AN2105/D

AN2105

Power-On, Clock Selection, and Noise Reduction Techniques for the Motorola MC68HC908GP32

By Y.T. Ng
Applications Engineering
Microcontroller Division
Hong Kong

This application note describes power-on/power-down, clock selection, and noise reduction techniques for applications using the Motorola MC68HC908GP32 MCU device, hereafter referred as the GP32.

For full device specification, please refer to the datasheet, Motorola order number: MC68HC908GP32/H.

Introduction

The GP32 is a popular general purpose device amongst Motorola's HC08 family of Microcontrollers. It has a new generation FLASH memory array, the 32k-bytes can be programmed in less than one second.

The versatility of the GP32 makes the device suitable for many applications and sometimes, finding itself in some very noisy environments. These noise and interference problems are made worse by poor circuit design and PCB layout, resulting in intermittent MCU failures and even complete breakdown.

To avoid these undesirable effects, there are some basic techniques that can be applied during circuit design and PCB layout. The following text describes some recommendations.

DigitalDNA™ from Motorola

Power-Up and Power-Down Requirements

The precautions described below must be followed for MCU power-up and power-down, otherwise unpredictable MCU behavior may occur.

Power supply rise-time

Power supply fall-time

Meeting power-on reset requirements

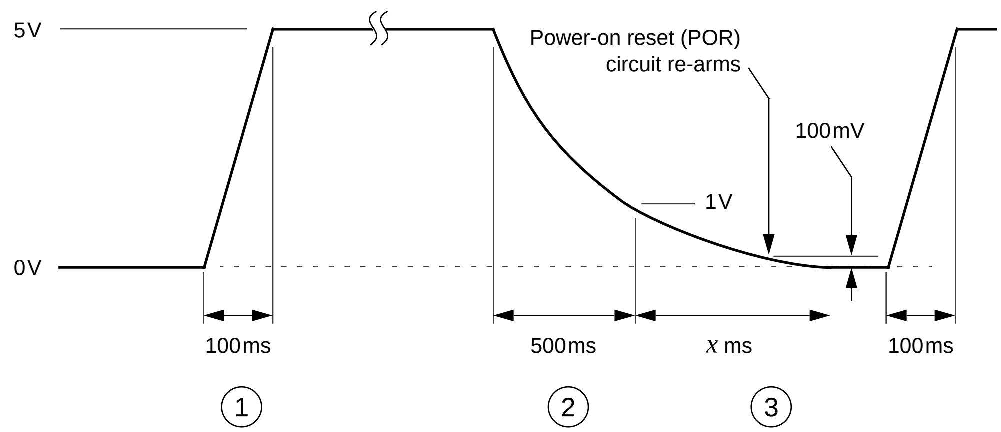


Figure 1. Power Supply Power-Up/Down Requirements

1. At power-up, supply voltage rise-time should be as short as possible; less than 143ms for 5V operation; best to aim for less than 100ms.
2. At power-down, supply voltage should fall below 1V in less than 500ms.
3. Before power-up again, supply voltage must fall below 100mV for the GP32 power-on reset circuit to rearm.
4. In addition, keep the external reset pin ($\overline{RST}$) pulled low at least until supply voltage has reached its operating level.

Improper power-up or power-down conditions cause problems for all MCUs, not just the GP32. Since the MCU contains a microprocessor and running a program, an improper power-up may cause the MCU to behave erratically and execute runaway codes. In severe cases, devices with electrically erasable memory (e.g. FLASH memory) could experience memory erasure if these power-up and power-down parameters are not taken seriously.

The data related to the above requirements are specified in the GP32 datasheet. They are reproduced in the table below, with explanatory notes in the following paragraphs.

	Symbol	Minimum		Typical		Maximum		Unit
Operating voltage	V_{DD}	5	3	5	3	5	3	V
POR rearm voltage	V_{POR}	0	0	—	—	100	100	mV
POR reset voltage	V_{PORRST}	0	0	700	700	800	800	mV
POR rise-time ramp rate	R_{POR}	0.035	0.02	—	—	—	—	V/ms

Data extracted from MC68HC908GP32 datasheet rev. 4.

POR rearm voltage

This parameter indicates the voltage where the power-on reset (POR) circuit becomes ready again (rearms) when the supply voltage falls. For a proper POR in a power-down followed by a power-up situation, the supply voltage must be allowed to fall below 100 mV before a power-up.

POR reset voltage

This parameter indicates the supply voltage where the POR circuit activates and performs a MCU power-on reset.

POR rise-time ramp rate

This parameter indicates supply voltage rise-time requirement for the POR circuit to operate successfully. The V_{DD} rise-time must be faster than the quoted POR rise-time minimum.

Choosing the MCU Reference Clock Frequency

Other than choosing the bus frequency, clocks for other GP32 modules are also important. Some modules require a minimum operating frequency, some depend on the bus frequency, and some depend on the input reference frequency.

Sometimes, the choice of the input reference frequency may be a compromise; so that it satisfies the clock requirements of the GP32 modules for a particular application.

Figure 2 shows the clock distribution to the modules inside the GP32.

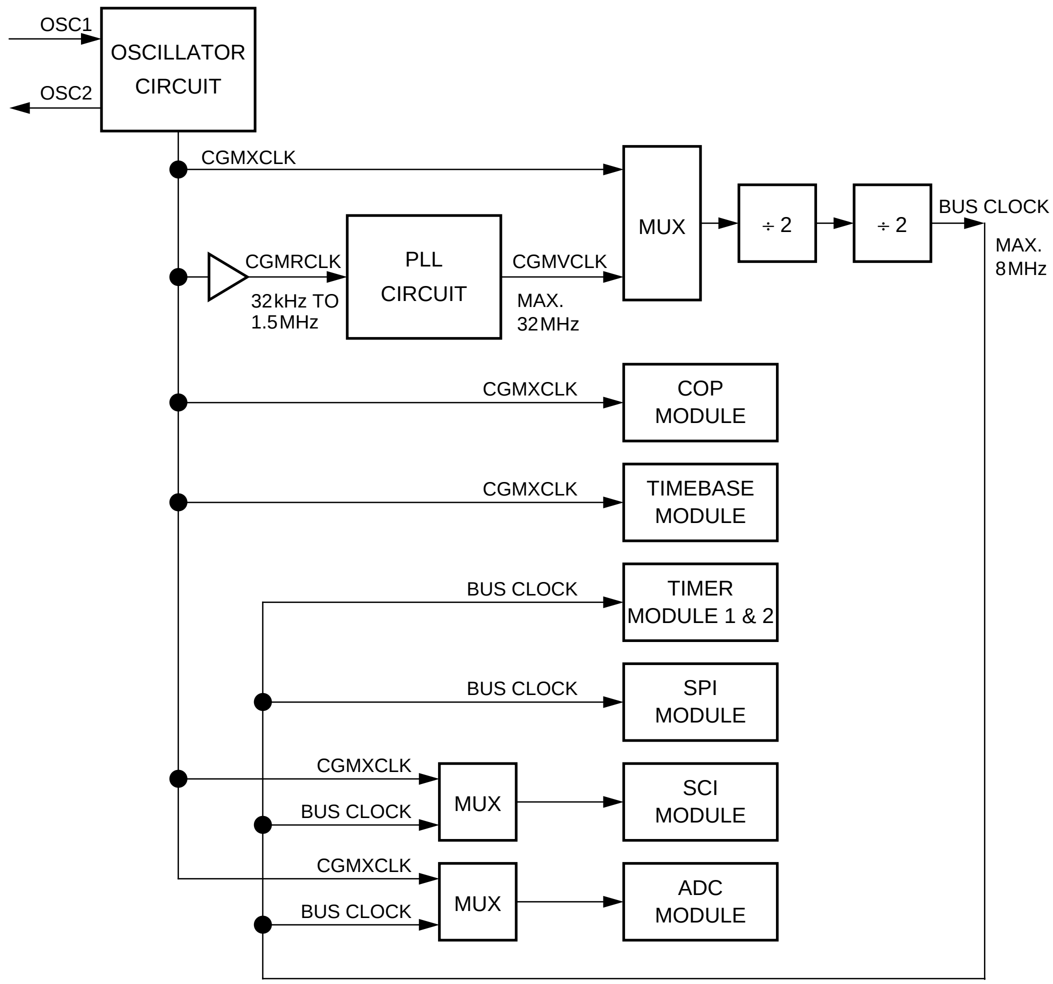


Figure 2. GP32 Clock Distribution

Generating the MCU Reference Clock

A reliable, stable and clean reference clock input is very important in MCU application designs, since the clock is the heart of the MCU.

The recommended method to generate the system clocks for GP32 is to use a low frequency input reference from a 32.768kHz crystal connected across OSC1 and OSC2 pins, and use the GP32's clock generation module (the PLL circuit) to generate the high frequency clock. This method generates less noise, with the higher frequencies contained within the MCU. A low frequency crystal is also cheaper in cost.

Crystal connection between OSC1 and OSC2 pins

Use the following components when using a 32.768 kHz crystal. This is the recommended crystal oscillator configuration.

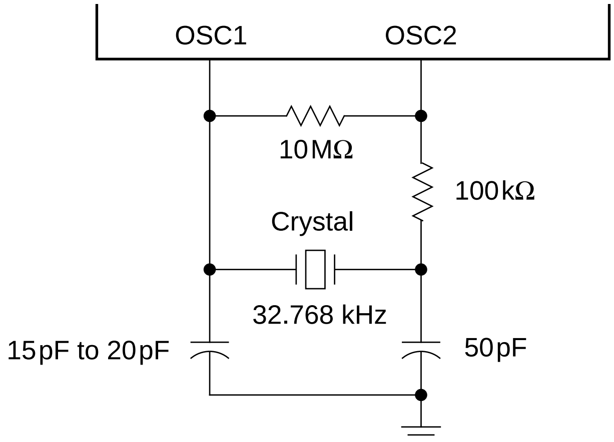


Figure 3. Components for 32 kHz Oscillation

The GP32's PLL circuit uses this 32.768 kHz reference clock for generating the higher frequency bus clock (see page 7). Although the GP32's PLL can accept a reference clock from 32 kHz to 1.5 MHz, the 32.768 kHz is chosen because it is an ideal frequency for driving the timebase module (see Figure 2), for real-time clock generation.

Crystal oscillator start-up time

From Figure 3, the 10 MΩ feedback resistor is used as the oscillator inverter, biased to $\frac{1}{2}V_{DD}$, to set up a high gain inverter amplifier. For the 32.768 kHz crystal oscillator, a 100 kΩ resistor with 50 pF capacitor are added for oscillator start-up time delay. Unlike high frequency oscillators (greater than 1MHz), the 32.768 kHz oscillator cycle is 30.52 µs, which needs significant time for start-up. Figure 4 shows the typical oscillator start-up time for the 32.768 kHz crystal oscillator when power is applied. The typical delay is 130 ms.

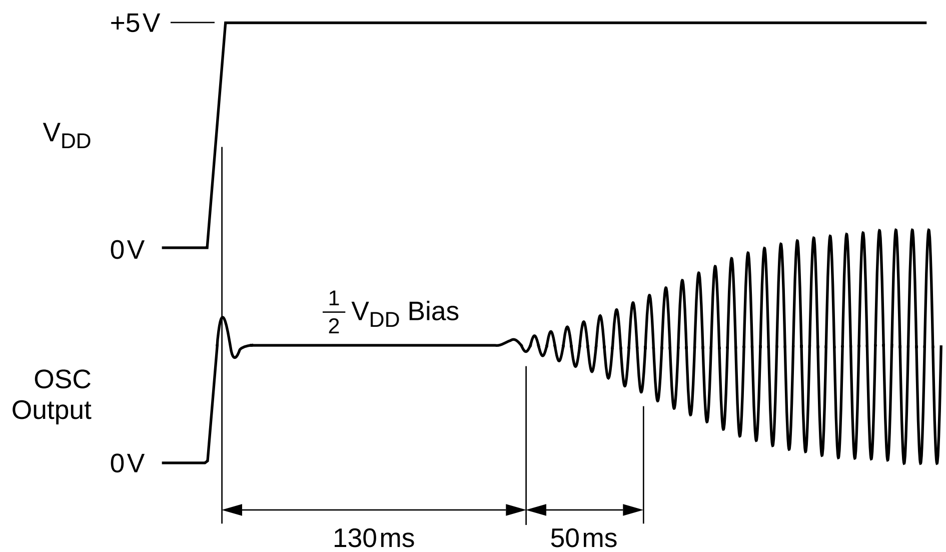


Figure 4. Crystal Oscillator Start-Up

Alternative clock source: External clock drive into OSC1 pin

The alternative to the crystal oscillator connection is to use a square wave from an external oscillator, driven directly into the OSC1 pin, and leaving OSC2 pin unconnected. The square wave should have a 50% duty cycle. Using this method, the maximum clock input is 32 MHz. Note that the PLL circuit cannot use a 32 MHz input clock. The PLL input reference clock range is from 32 kHz to 1.5 MHz.

With the PLL off, a 32 MHz clock input divides to an 8 MHz bus clock. Note also that this 32 MHz clock feeds to the COP and timebase modules (see Figure 2), giving a relatively short COP period.

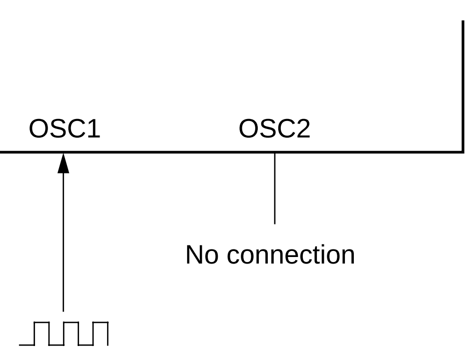


Figure 5. External Oscillator Drive to OSC1

Generating a High Bus Frequency from a Low Frequency Reference

The GP32's PLL can generate up to the maximum bus frequency of 8MHz using a 32.768kHz clock reference.

To be precise, the PLL accepts a reference clock between 32 kHz and 100 kHz. A prescaler is available for dividing the oscillator clock to within the accepted range. This prescaler has an integer value of divide-by-1 to divide-by-15. Therefore, the maximum input reference frequency allowed is 1.5 MHz.

Selecting filter components for the PLL circuit

Use either of the following filter networks for connection to the GP32's CGMXFC pin.

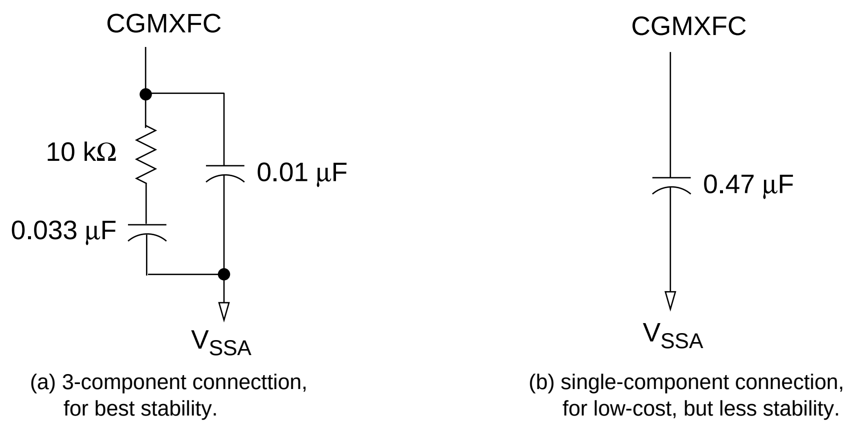


Figure 6. Filter Components for PLL

VCO drives in PLL circuit

Figure 7 shows a diagrammatic representation of the current drives into the voltage controlled oscillator (VCO) for frequency tracking.

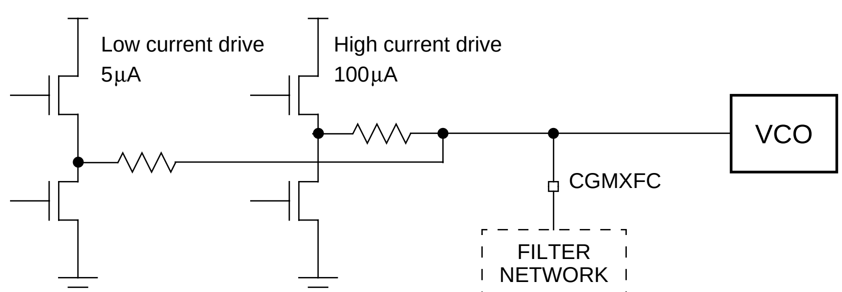


Figure 7. VCO Drives

The typical PLL lock response for the two filter networks are shown in Figure 8 and Figure 9.

PLL lock response

Figure 8 and Figure 9 show actual plots for the PLL lock time, for the two configurations of the external filter.

Single-component filter

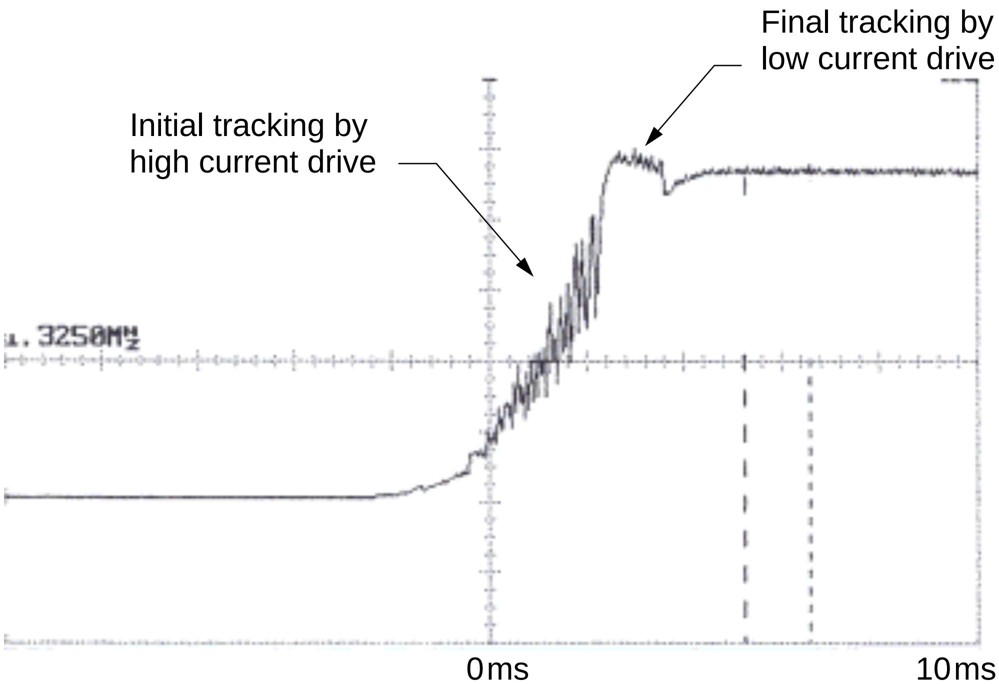


Figure 8. PLL Lock Response with Single-Component Connection

3-component filter

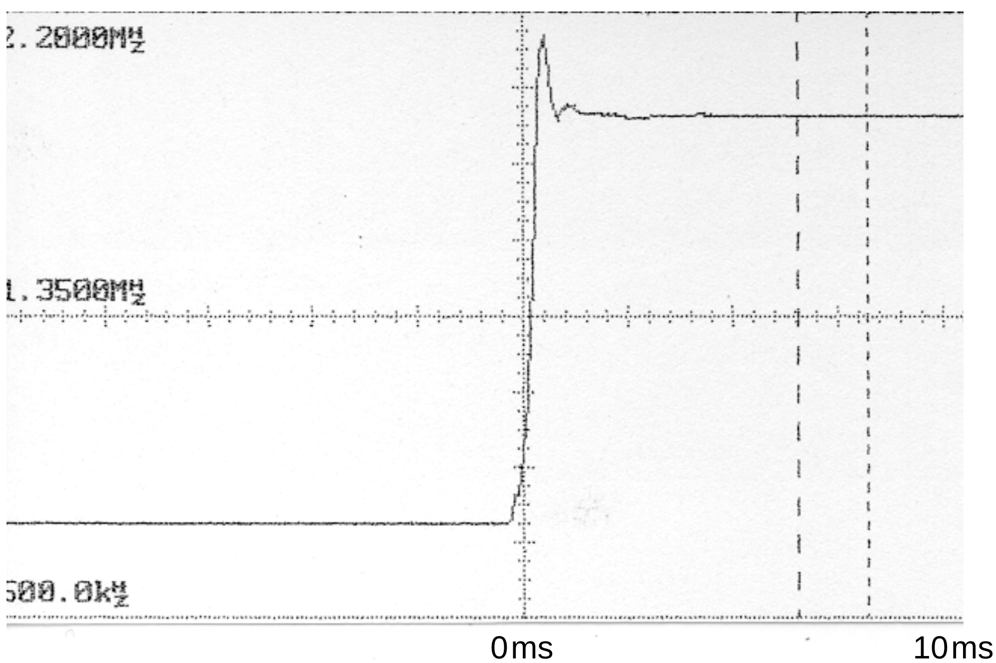


Figure 9. PLL Lock Response with 3-Component Connection

Programming the phase-lock loop

The following code listing is for a VCO frequency of 32 MHz, from a 32.768 kHz clock reference to the MCU. The 32 MHz divides to an 8 MHz bus clock.

Note that the PLL can only be programmed when it is off. Therefore, always clear the PLLON bit before writing to the PLL programming registers.

```
PCTL    EQU     $0036    ; PLL Control Register
PBWC    EQU     $0037    ; PLL Bandwidth Control Register
PMSH    EQU     $0038    ; PLL Multiplier Select Register High
PMSL    EQU     $0039    ; PLL Multiplier Select Register Low
PMRS    EQU     $003A    ; PLL VCO Range Select Register
PMDS    EQU     $003B    ; PLL Reference Divider Select Register

BRCLR   5,PCTL           ; Turn Off PLL

LDA     #$00             ; Set P=0 for PRE[1:0]
STA     PCTL
LDA     #$02             ; Set E=2 for VPR[1:0]
STA     PCTL
LDA     #$D1             ; Set N=977 for MUL[11:0]
STA     PMSL
LDA     #$03
STA     PMSH
LDA     #$D0             ; Set L=208 for VRS[7:0]
STA     PMRS
LDA     #$01             ; Set R=1 for RDS[3:0]
STA     PMDS
BSET    5,PCTL           ; Turn On PLL
BSET    7,PBWC           ; Enable Auto Bandwidth Control
BRCLR   6,PBWC,*         ; Loop until LOCK bit set
BSET    4,PCTL           ; Select VCO clock as system clock
NOP
NOP
```

For programming the VCO to other frequencies, please refer to *Programming the PLL* section in the GP32 datasheet (rev. 4 datasheet, section 6.4.6, page 113).

PCB Layout for Critical Signals

Power supply decoupling

Connect these critical components as close as possible to the MCU and with the shortest return path to the MCU ground pin. Each V_{DD} pin should be decoupled to ground with its own capacitors.

PLL filter network connections

Crystal oscillator connections

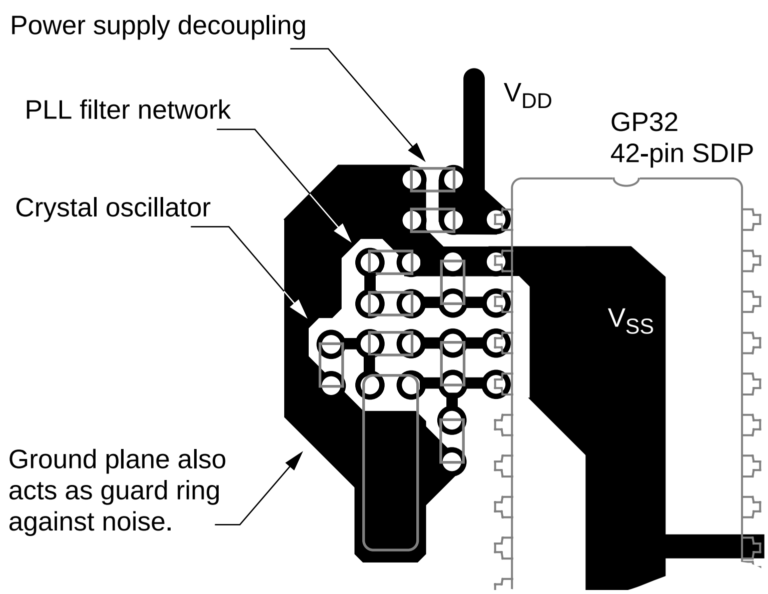


Figure 10. Critical Component PCB Layout

Grounding multiple V_{SS}

Connect device ground pins together at the center with the shortest path.

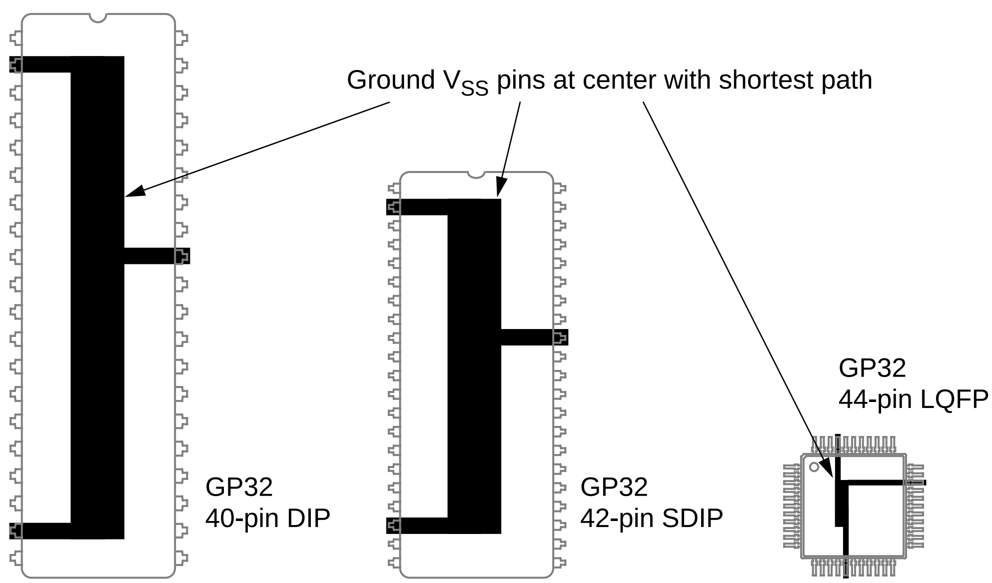


Figure 11. Grounding Multiple V_{SS}

Ground return for high-current devices

Keep high current return ground paths separate from low current return ground paths, and join them at a single point near the regulator or the power supply input.

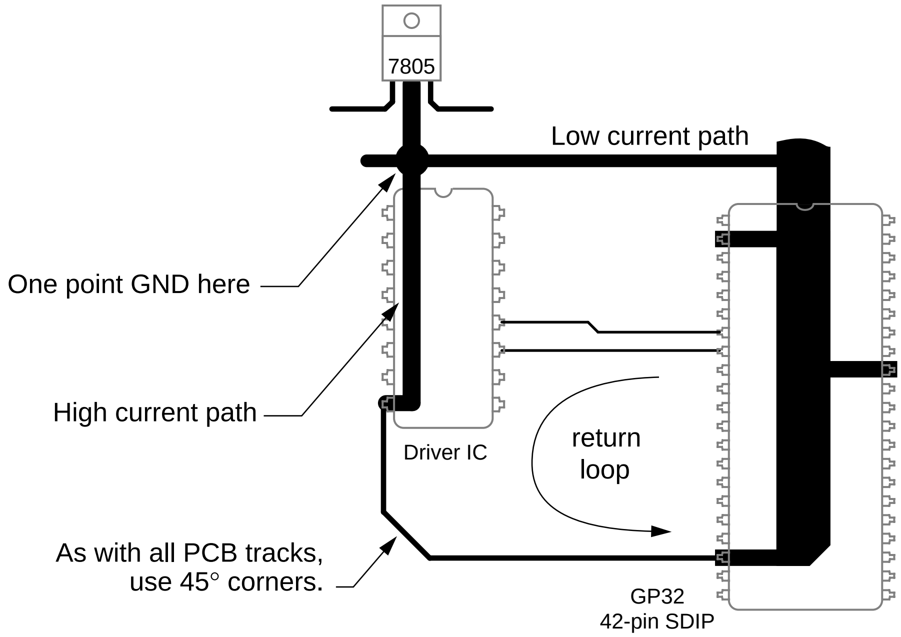


Figure 12. Ground Return for High Current Devices

Long signal line to ADC pins

Terminate a long PCB trace carrying analog signal with a decoupling capacitor — at the MCU ADC input pin.

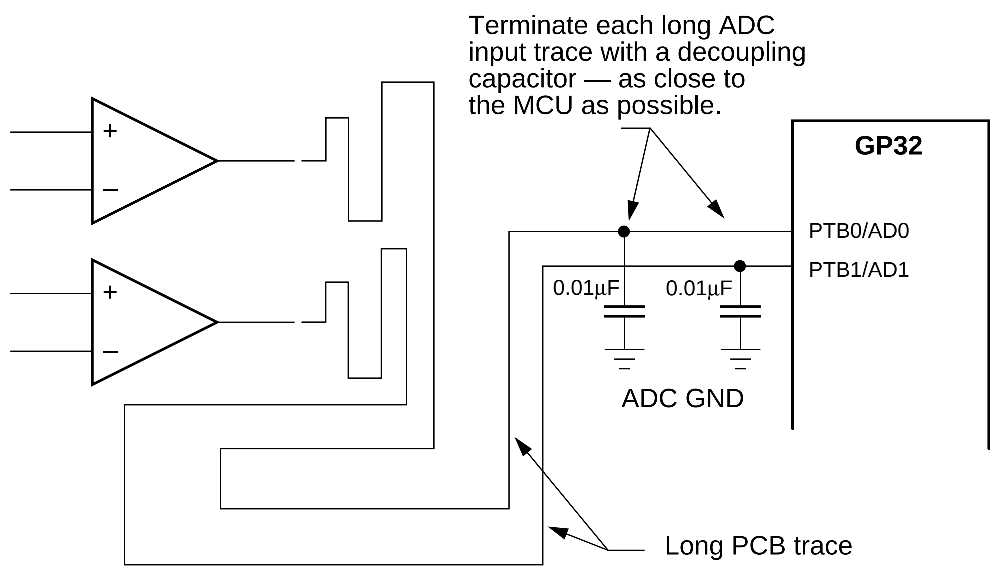
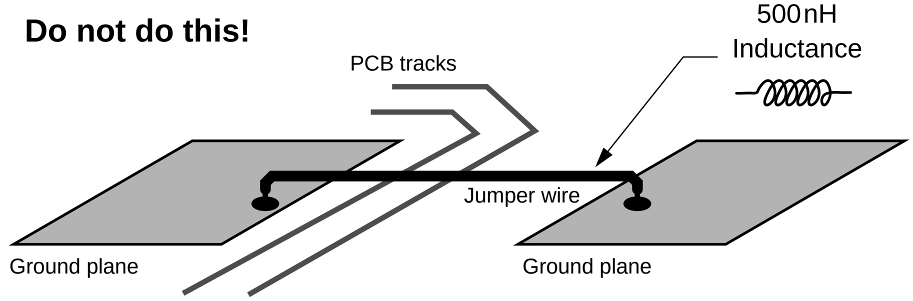


Figure 13. Long Analog Paths

Connecting multiple ground planes

Avoid connecting multiple ground planes together using a single wire, as shown in Figure 14.



$$V = L\,di/dt$$
$$L = 500\,nH,\ I = 10\,mA,\ t = 5\,ns$$
$$V = 1\ volts$$

Figure 14. Avoid Connecting Multiple Ground Planes

The single wire will have inductance, causing a potential difference between the two ground planes.

How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution; P.O. Box 5405, Denver, Colorado 80217. 1-303-675-2140 or 1-800-441-2447

JAPAN: Motorola Japan Ltd.; SPS, Technical Information Center, 3-20-1, Minami-Azabu, Minato-ku, Tokyo 106-8573 Japan. 81-3-3440-3569

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre, 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong. 852-26668334

Technical Information Center: 1-800-521-6274

HOME PAGE: http://www.motorola.com/semiconductors/

MOTOROLA