

MMDS and MMEVS Changes for MC68HC908ASxxA, MC68HC908AZxxA, and MC68HC908AB32

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Introduction and Background

The 0.5- μ MC68HC(9)08AB/AS/AZ devices^{1, 2} utilize a new EEPROM (electrically erasable programmable read-only memory) technology which differs slightly from older devices. The programming algorithm is backward compatible, but an accurate and specific timebase is now needed for proper program and erasure. Control of this timebase is shared between the tool, either the Motorola Modular Development System (MMDS) or the Motorola Modular Evaluation System (MMEVS), and the user's code. An abundant number of clocking options exists.

This document explains the device operation in an MMDS environment and gives examples on how to handle different circumstances.

1. Devices include: MC68HC908AB32, MC68HC908AS60A, MC68HC908AZ60A, MC68HC908AZ32A, MC68HC908AS32A, and MC68HC08AZ32A.

2. Unique memory configuration files are available for each MCU. These files are available at <http://www.motorola.com/mcu/>

Device Operation

When the user writes data to EEPROM locations using LOAD (load S19 file), MM (memory modify), and BF (block fill) commands, the MMDS programs the data in the internal EEPROM of the resident microcontroller on the emulation board.

However, before executing the commands to write data to EEPROM locations, the user must set up the EEPROM timebase properly.

CAUTION: *If the user sets the wrong timebase divider and executes the LOAD, MM, or BF commands, the EEPROM will be incorrectly programmed and might get damaged.*

For more details regarding the EEPROM constant timebase, refer to the EEPROM section in the relevant data book.

To set the EEPROM timebase, determine:

1. Which EEPROM reference clock source is selected? (CGMXCLK or system bus clock)

The EEPROM reference clock source is defined by the EEDIVCLK bit in configuration register 2 (CONFIG-2). The microcontroller selects CGMXCLK on reset. To calculate a correct EEPROM timebase divider value, the user has to know which clock is currently used as the EEPROM reference clock source. (Example situations of this are discussed later in this document.) For simplicity, Motorola recommends the user leave EEDIVCLK in its default state.

2. Is the EEPROM timebase divider initialized correctly?

To set the correct timebase divider, the user has two options: (Example situations of this are discussed later in this document.)

- a. Program the correct divider value to the EEDIVNVR (or relevant EExDIVNVR). The programmed divider value is loaded to EEDIV (or relevant EExDIV) after each reset.

- b. Write the correct divider value to the EEDIV (or relevant EExDIV). The EEDIV (or relevant EExDIV) is NOT a write-once register. The last written divider value is held until the next reset occurs.

NOTE: *To program a divider value to the EEDIVNVR (or relevant EExDIVNVR) using the MM command, method “b” must be used.*

The setting of the timebase might have to be changed during the user’s debugging process, depending on the selected EEPROM reference clock and the EEPROM divider value at a debugging point. Therefore, the user has to understand the current debug condition and change the setting of the timebase accordingly before executing the commands.

Environment Examples

As mentioned previously, many situations are possible during the debug process. The following situations are examples in which the user should change the EEPROM divider setting before writing data to EEPROM locations using LOAD, MM, or BF commands.

Situation A — When the EEPROM reference clock source is switched from the CGMXCLK to the system bus clock. A divider value has to be recalculated and a new value has to be written to the EEDIV (or relevant EExDIV).

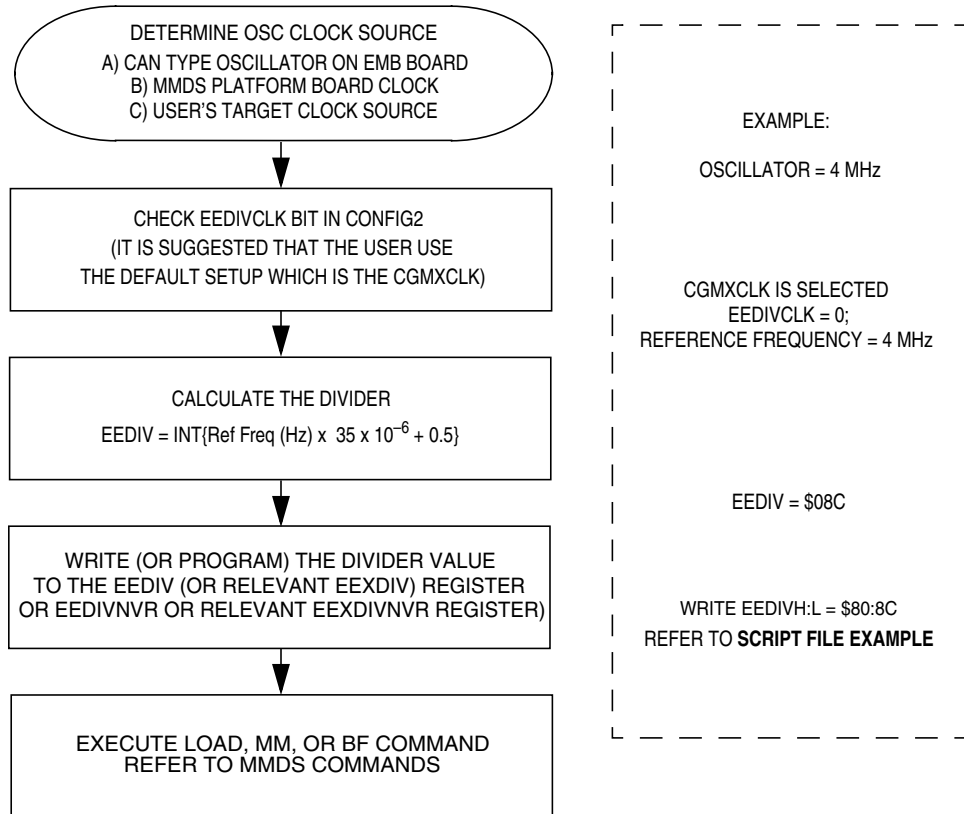
Situation B — When a reset occurs, the microcontroller automatically loads the data from the EEDIVNVR (or relevant EExDIVNVR) to the EEDIV (or relevant EExDIV), and the CGMXCLK is selected as the EEPROM reference clock source. If the user had temporarily set the timebase divider in the EEDIV (or relevant EExDIV) for a certain reference clock speed, the divider value is changed to data in the EEDIVNVR (or relevant EExDIVNVR) after a reset. If the user also previously selected the system bus clock as the reference clock source, it has now been switched to CGMXCLK. Before executing the commands, make sure that the timebase divider value is set properly.

Situation C — When the system bus clock is selected as the EEPROM reference clock source and a system bus clock speed is changed by PLL. When the user selects the system bus clock source, a timebase divider value has to be calculated using the system bus clock speed. Whenever the bus clock speed is changed by the PLL, the divider value also has to be recalculated and written to the EEDIV (or relevant EExDIV).

Situation D — When execution of the user's code is stopped by the STOP command or at a break point. This example is a case where the bus speed is generated by the PLL in the user's code. When a microcontroller comes back from the user code to the monitor by a STOP command or at a breakpoint, the PLL bus speed is maintained until the next reset occurs or the PLL is turned off. If the system bus clock is selected as the reference clock source, make sure that the timebase divider value is set up correctly before executing the commands (LOAD, MM, BF).

NOTE: *The MMDS does not automatically set up a correct divider value. Therefore, the user is responsible for setting it correctly.*

Divider Setup Example Flowchart



Script File Example

If the user needs to set up the timebase divider quite often during his/her debug, using a script file is convenient. The following is a sample script file.

To understand the SCRIPT command, refer to the MMDS operations manual, Motorola document order number M68MMDS0508OM/D.

```
; In this example, the CGMXCLK is selected as the EEPROM reference
; source clock and the frequency is 4 MHz.
; Set an EEDIV (or relevant EE1DIV) value at EEDIVH and EEDIVL (or relevant EE1DIVH and EE1DIVL)
registers
mm FE1A 80
mm FE1B 8C
; Set an EE2DIV value at EE2DIVH and EE2DIVL registers (not required for devices with only one
EE array - refer to relevant databook)
mm FF70 80
mm FF7B 8C
```

Emulation Board Hardware Modifications

Two pins ($\overline{\text{IRQ}}$ and $\overline{\text{RESET}}$ on the M68HC08 Family of MCUs) have special three-state input functions to allow either special modes to be entered or for disabling the COP watchdog timer. The new 0.5- μ devices have slightly different input structures to detect a higher voltage input on the $\overline{\text{IRQ}}$ and $\overline{\text{RESET}}$ pins than the older devices. A component change on the board is necessary to ensure consistent operation on the MMDS08. **Figure 1** shows the old and new circuits.

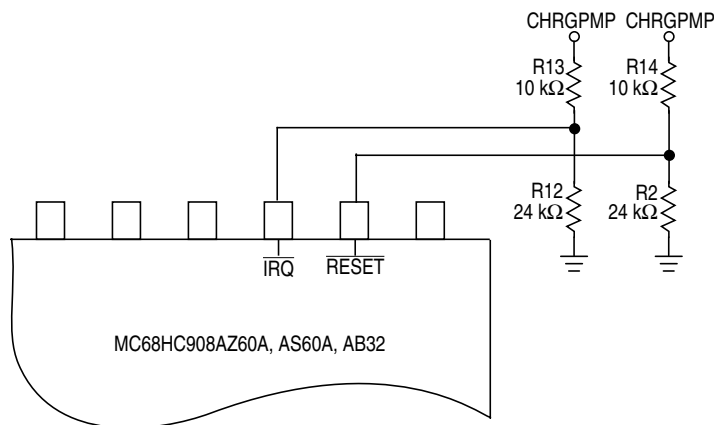


Figure 1. Emulation Board Configured for AZ/AS/AB (Original Design)

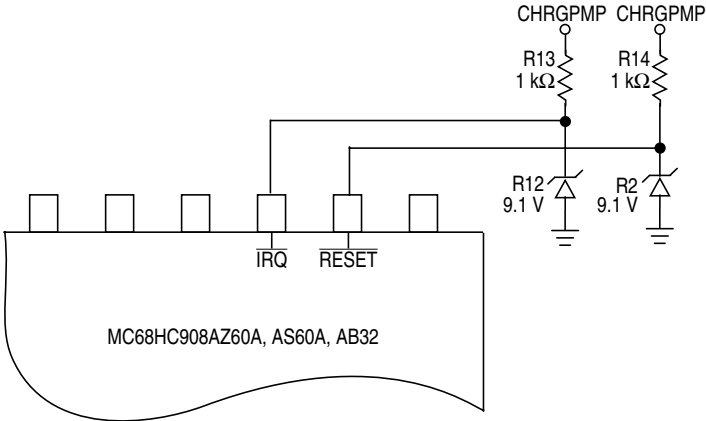


Figure 2. Emulation Board Configured for AZ/AS/AB (Modified Design)

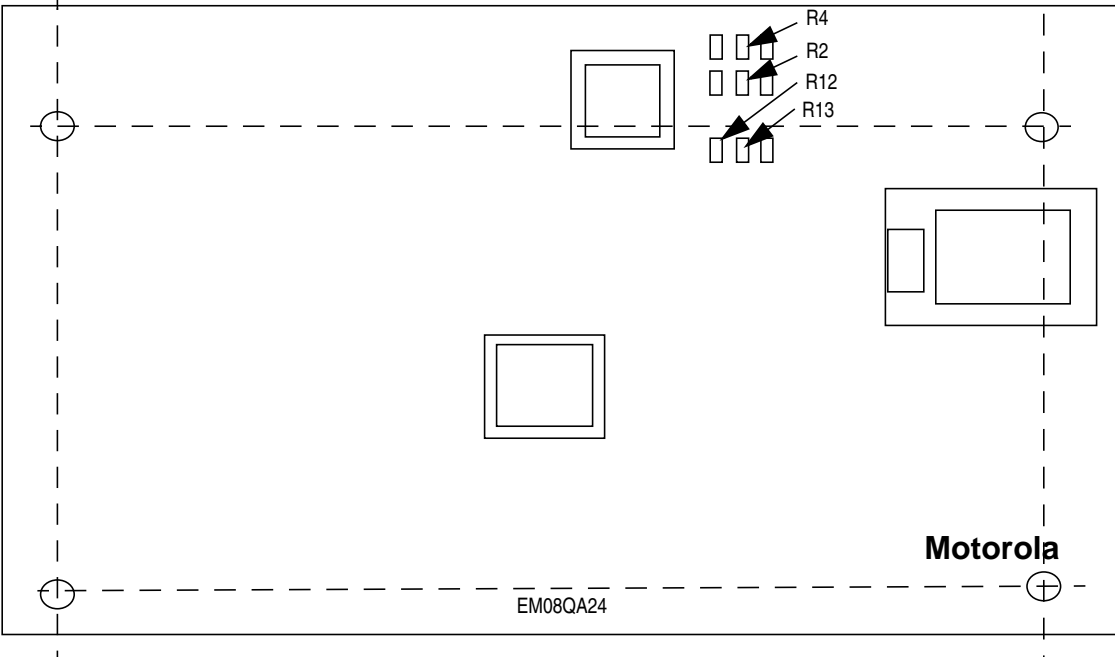



Figure 3. M68EM08AZ60 Showing Approximate Location of R13–R16

Conclusion

Existing emulation modules can be modified for use with the new 0.5- μ M68HC08 and M68HC908 devices. This document has detailed the special EEPROM procedures and the hardware differences from the older devices.

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