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M68HC705L4 PROGRAMMER BOARD

(REVision A PWBs only)

APPLICATION NOTE

INTRODUCTION

This application note describes the programming technique used to program and verify the XC68HC705L4 microcontroller (MCU) internal OTPROM/EPROM, and how to construct the programmer board (PGMR) used in conjunction with this application note. All that is required to program the XC68HC705L4 OTPROM/EPROM MCU is the PGMR and a +5 volt and V_{PP} dc power supply.

The PGMR can be fabricated for either shrink dual-in-line package (SDIP) MCU device programming, quad flat pack (QFP) MCU programming or plastic leaded chip carrier (PLCC) MCU device programming.

PROGRAMMING TECHNIQUE

The PGMR programming technique allows the user program, contained in an external EPROM, to be copied into the internal PROM (OTPROM/EPROM) of the XC68HC705L4 MCU device.

The XC68HC705L4 MCU device is inserted into the PGMR. The applicable program/verify routine is selected via jumper header JP3, and power is applied to the PGMR via switch S1. The MCU is taken out of reset and placed in the run mode via switch S2, and MCU control is transferred to the bootstrap ROM. The selected programming routine is then executed.

PROGRAM AND VERIFY MCU PROM

In the program and verify MCU PROM routine, the contents of an external 16K EPROM are copied into the MCU PROM areas of the applicable device. There is a direct correlation of addresses between the two devices. Non-MCU PROM addresses are ignored so data contained in those areas are not accessed. Unprogrammed external EPROM address locations should contain $00 to speed up the programming operation. During the programming routine, the PROGRAM LED D3 is illuminated. At the end of the programming routine, D3 is turned off, and the verification routine is entered. If the contents of the MCU PROM and external EPROM exactly match, then the VERIFY LED D2 is illuminated.

During the verification routine, all locations are compared to the data residing in external EPROM. The verification routine will stop if a discrepancy has been detected and the error address location will be placed on the external memory address bus.

Verify MCU PROM

The verify MCU PROM contents routine is normally entered automatically after the MCU PROM is programmed. Direct entry of this mode will cause the MCU PROM contents to be compared to external EPROM contents residing at the same address locations. Both D2 and D3 LEDs are turned off at this time until verification is completed. Upon completion of the verification routine (every location verified) the VERIFIED LED D2 is illuminated. If D2 does not illuminate, a discrepancy has been detected and the error address location will be placed on the external memory address bus.

NOTE

MCU PROM blank checking can be accomplished by placing $00 into the external EPROM (SKT1) and following the above verify MCU PROM routine.

PROGRAMMING MODULE PREPARATION

The PGMR must be prepared/configured prior to any program/verify operations. Board preparation consists of the external power source (+5V and V_{PP}), EPROM installation, DIP PGMR configuration, and PLCC, QFP or SDIP PGMR configuration.

External Power Source

Power connector P1 is used to connect an external power supply to the PGMR. A +5 Vdc @ 100 mA power source is connected to connector P1 pins labeled +5V and GND. The programming voltage power source is connected to pins labeled V_{PP} and GND. Refer to the specific device data sheet for programming voltage (V_{PP}) specifications.

NOTE

The programming voltage (V_{PP}) must be measured at SKT3 pin 19 during programming cycle (D3) PROGRAM LED illuminated.

EPROM Installation

The basic EPROM device used on the PGMR (at location SKT1) is a 27128 or 27C128, 16K EPROM, 28-pin device. This EPROM device contains the user code to be programmed into the applicable PROM MCU device.

SDIP PGMR Configuration

For the shrink dual-in-line package (SDIP) device programming, the PGMR printed wiring board (PWB) must be fabricated with a SDIP zero-insertion-force (ZIF) socket located at SKT3.

PLCC PGMR Configuration

For the plastic leaded chip carrier (PLCC) device programming, the PGMR printed wiring board (PWB) must be fabricated with a PLCC zero-insertion-force (ZIF) socket located at SKT2.

QFP PGMR Configuration

For quad flat pack (QFP) MCU device programming, the PGMR PWB must be fabricated with QFP ZIF sockets located at SKT 4.

PROGRAMMING OPERATION

To program the XC68HC705L4 MCU PROM, perform the following steps:

1. Place switch S1 to POWER-OFF (left) position.
2. Install MCU and EPROM devices into PGMR.
3. Place switch S2 to RESET-IN (left) position.
4. Check that the jumpers are set as follows:

   JP1 - 27C128 position

   JP2 - Program / verify position

   JP3 - Program position to program device
5. Place switch S1 to POWER-ON (right) position.
6. Place switch S2 to RESET-OUT (right) position.

   PROGRAM LED illuminates signifying programming sequence being performed. VERIFY LED illuminates signifying verification is completed.
7. Place switch S2 to RESET-IN (left) position.
8. Remove power (via S1), or select and run new routine.

PROGRAMMER BOARD CONSTRUCTION

The PGMR is a two-sided Printed Wiring Board (PWB). Table 1 provides the parts list for the PGMR. Component tolerances are generally not critical. Use of Integrated Circuit (IC) or Zero Insertion Force (ZIF) sockets are recommended for both EPROM and MCU devices. This will simplify the removal and installation of both devices. Figure 1 is the schematic diagram for the PGMR board.

TABLE 1 - PGMR Parts List

REFERENCE DESIGNATION	COMPONENT DESCRIPTION
C1,C3	Capacitor, 47 µF @ 35 Vdc
C2,C4,C5,C8-C11	Capacitor, 0.1 µF @ 50 Vdc
C6, C7	Capacitor, 22pF @ 50 Vdc
D1	Diode, 1N4735
D2, D3	LED, HP # HLMP-4700 or equivalent
JP1-JP3	Header, 3-pin, single row, 3M #929450-01-30
P1	Power connector, Augat # RDI 2SV-03
R9	Resistor, 10M, 1/4W, 5%
R3-R6	Resistor, 10K, 1/4W, 5%
R7, R8	Resistor, 470, 1/4W, 5%
R1, R2	Resistor, 51, 1/4W, 5%
U1,U2	74HC393
S1, S2	Switch, DPDT, Augat ALCO # MHS223
SKT1	Socket, DIP, 28-pin ZIF, Welcon # 613-7280316
SKT2	Socket, PLCC, 68 pin ZIF, Yamaichi IC120-0684-204
SKT3	Socket, SDIP, 64 pin ZIF, Yamaichi IC85-64075
SKT4	Socket, QFP, 64 pin ZIF, Yamaichi IC51-0644-692
Y1	2 MHz crystal or ceramic resonator

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Figure 1 - PGMR Schematic Diagram