M68EML05P6A
EMULATION MODULE

NOTES, UNLESS OTHERWISE SPECIFIED

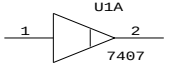
1. VCC PIN LOCATIONS :

   VCC IS APPLIED TO PIN 8 OF ALL 8-PIN IC's, PIN 14 OF ALL 14-PIN IC's, PIN 16 OF ALL 16-PIN IC's, PIN 20 OF ALL 20-PIN IC's, ETC.

2. GROUND PIN LOCATIONS :

   GROUND IS APPLIED TO PIN 4 OF ALL 8-PIN IC's, PIN 7 OF ALL 14-PIN IC's, PIN 8 OF ALL 16-PIN IC's, PIN 10 OF ALL 20-PIN IC's, ETC.

3. DEVICE TYPE, PIN NUMBERS, AND REFERENCE DESIGNATOR OF GATES ARE SHOWN AS FOLLOWS :



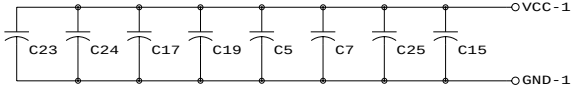
7407 = DEVICE TYPE
1 AND 2 = PIN NUMBERS
U1A = REFERENCE DESIGNATORS

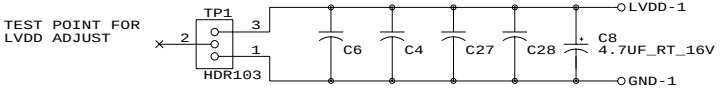
4. RESISTANCE VALUES ARE IN OHMS.
5. RESISTORS ARE 1/4 WATT, 5%.
6. CAPACITANCE VALUES ARE IN MICROFARADS.

REVISIONS

ECN #	PCB REV	SCH REV	DESCRIPTION	DATE
125	O	2	Test mode timing is on E and not PH2 as expected. Change clock for early signals to PH2*. Cut LOCKOUT from U6 SETDFF pin. Cut LVDD from the U2 SETDFF pin. Diode on WR_DDRD signal to ensure write of 0 to DDRD7. Redo RESET circuit for LV Bidi.	10/21/96
126	A	3	Implement modifications from ECO 125 in new rev of PWB.	10/22/96
129	A	4	Changed SCLK signal from PH2 to E-EM. Provided LOCKOUT signal buffered through MACH to A/D PRU.	2/25/97

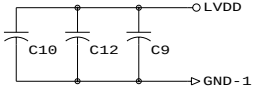
Decouple Caps for ICs as labeled.
All caps are 0.1 uF @ 50 V



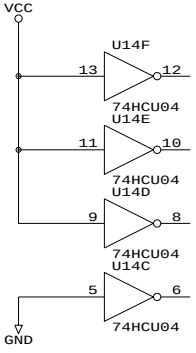


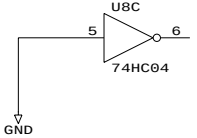
GROUND PLANE ----> GND-1

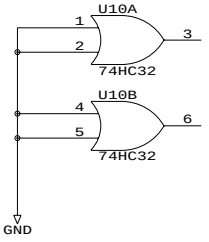
SPLIT POWER PLANE ----> VCC-1 & LVDD-1



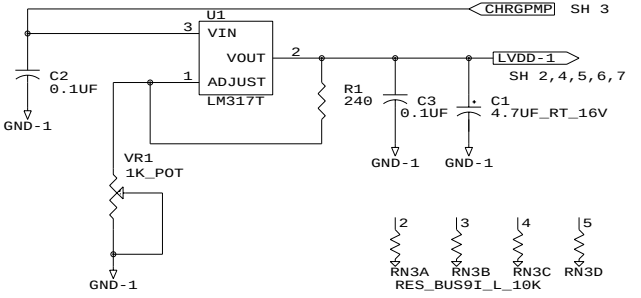
Spare Gates







VOLTAGE REGULATOR



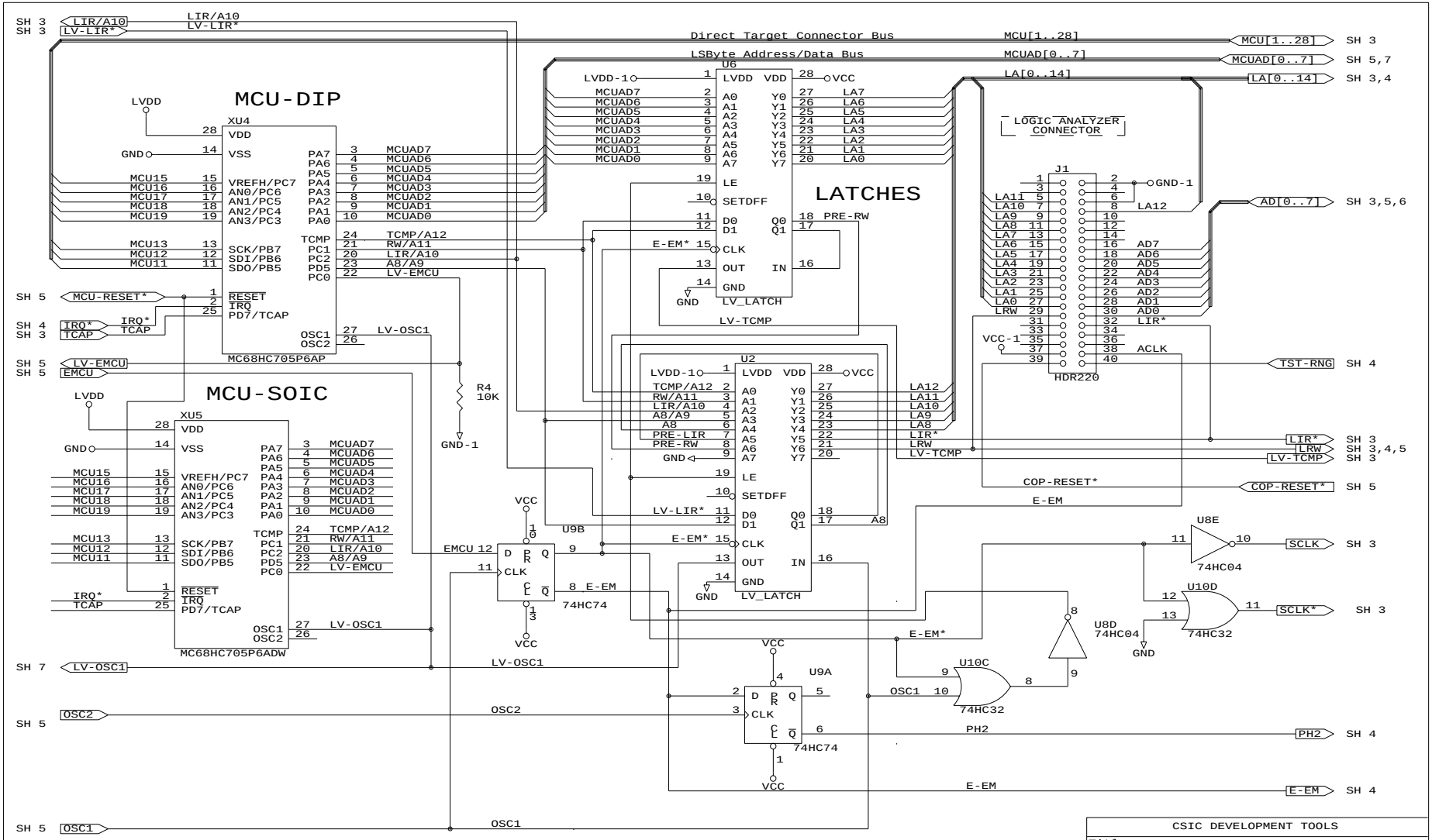
ORCAD IV FLAT FILES

|LINK
|LP6AR4S2.SCH
|LP6AR4S3.SCH
|LP6AR4S4.SCH
|LP6AR4S5.SCH
|LP6AR4S6.SCH
|LP6AR4S7.SCH

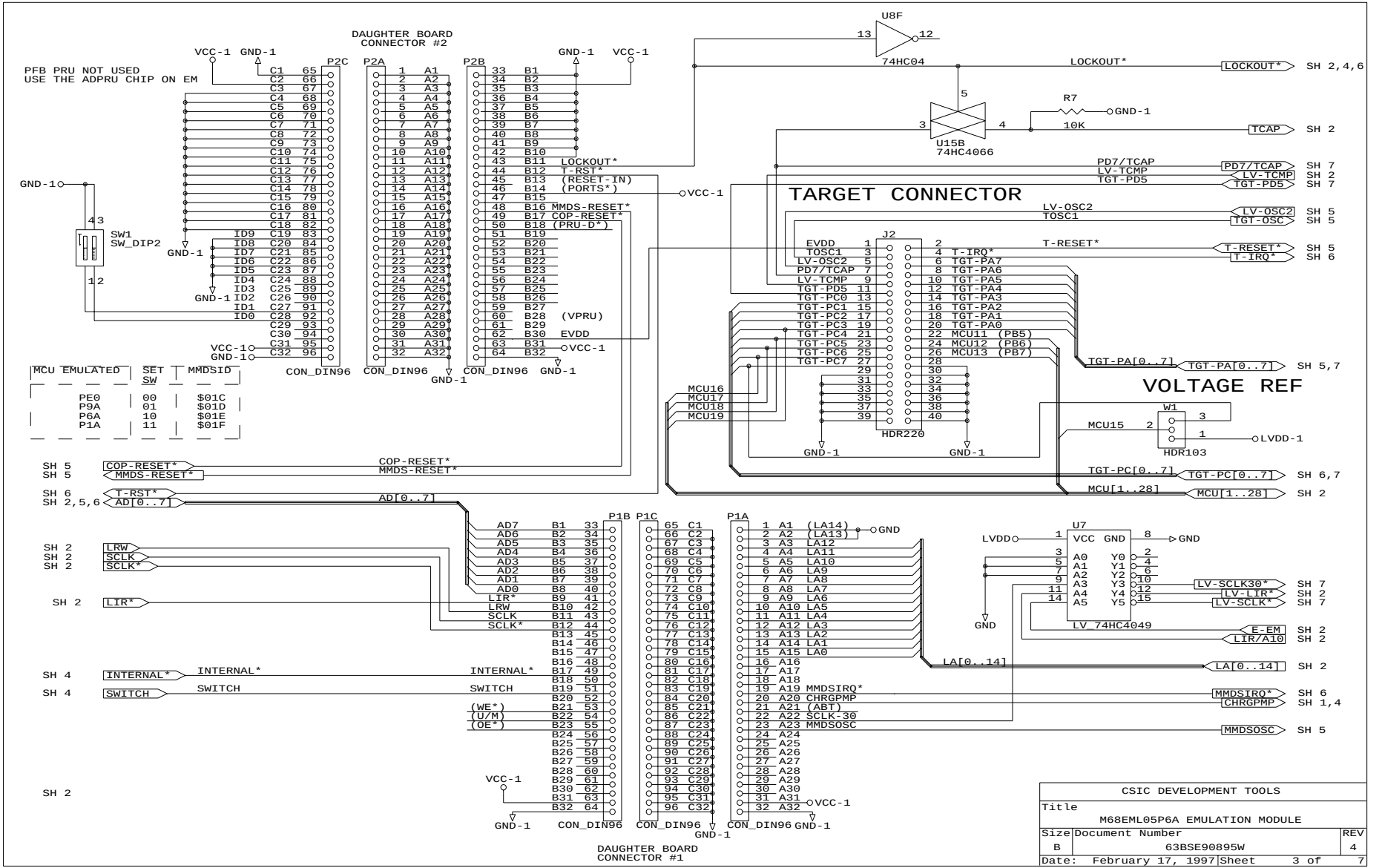
COMPUTER GENERATED DRAWING : DO NOT REVISE MANUALLY

CSIC DEVELOPMENT TOOLS

Title		
M68EML05P6A EMULATION MODULE		
Size	Document Number	REV
B	63BSE90895W	4
Date: February 25, 1997	Sheet 1 of 7	



CSIC DEVELOPMENT TOOLS		
Title: M68EML05P6A EMULATION MODULE		
Size: B	Document Number: 63BSE90895W	REV: 4
Date: February 17, 1997	Sheet: 2 of 7	



CSIC DEVELOPMENT TOOLS		
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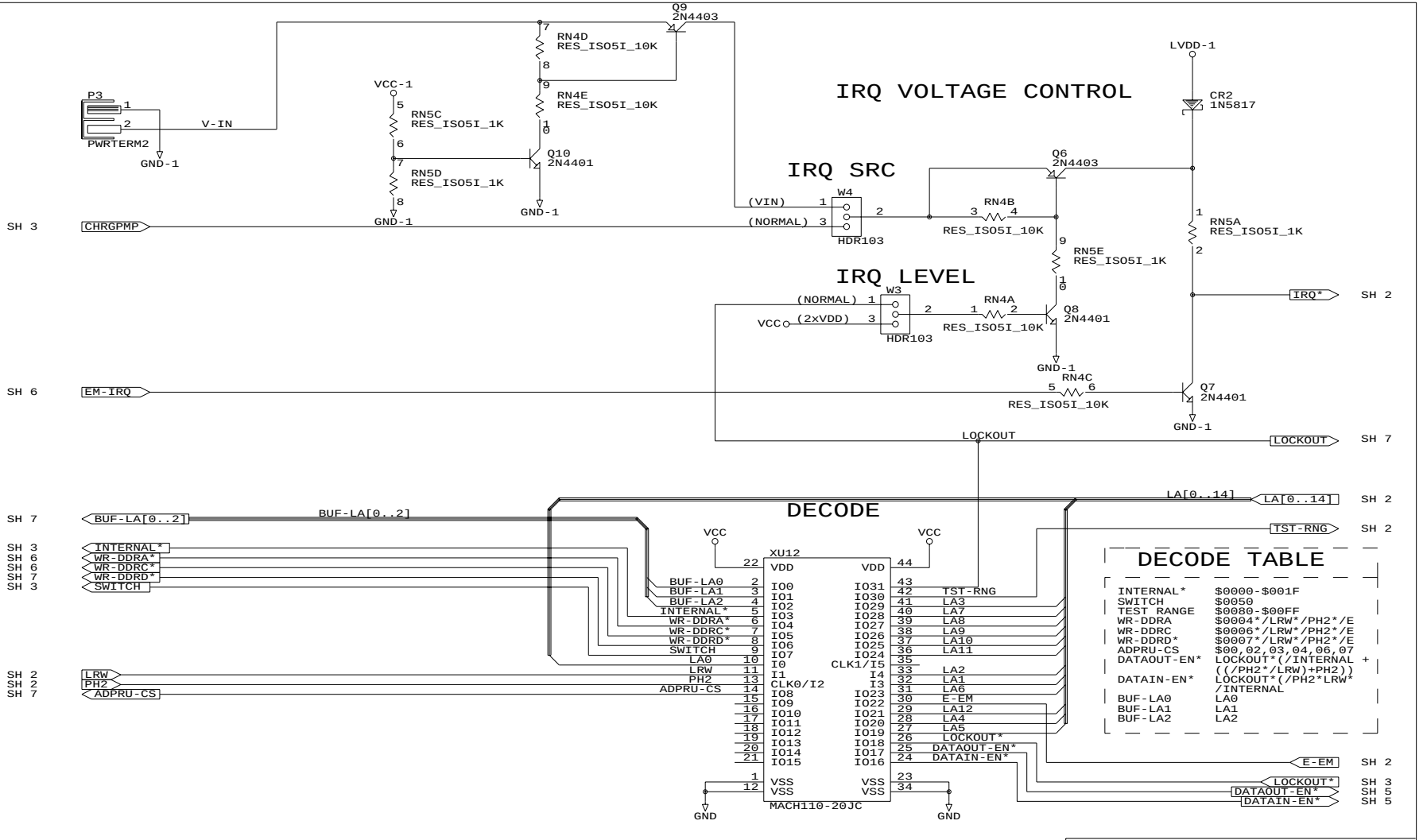
Size: B	Document Number: 63BSE90895W	REV: 4
Date: February 17, 1997	Sheet: 3 of 7	



DECODE TABLE

INTERNAL*	$0000-$001F
SWITCH	$0050
TEST RANGE	$0080-$00FF
WR-DDRA	$0004*/LRW*/PH2*/E
WR-DDRC	$0006*/LRW*/PH2*/E
WR-DDRD*	$0007*/LRW*/PH2*/E
ADPRU-CS	$00,02,03,04,06,07
DATAOUT-EN*	LOCKOUT*(/INTERNAL + (((/PH2*/LRW)+PH2))
DATAIN-EN*	LOCKOUT*(/PH2*LRW* /INTERNAL
BUF-LA0	LA0
BUF-LA1	LA1
BUF-LA2	LA2

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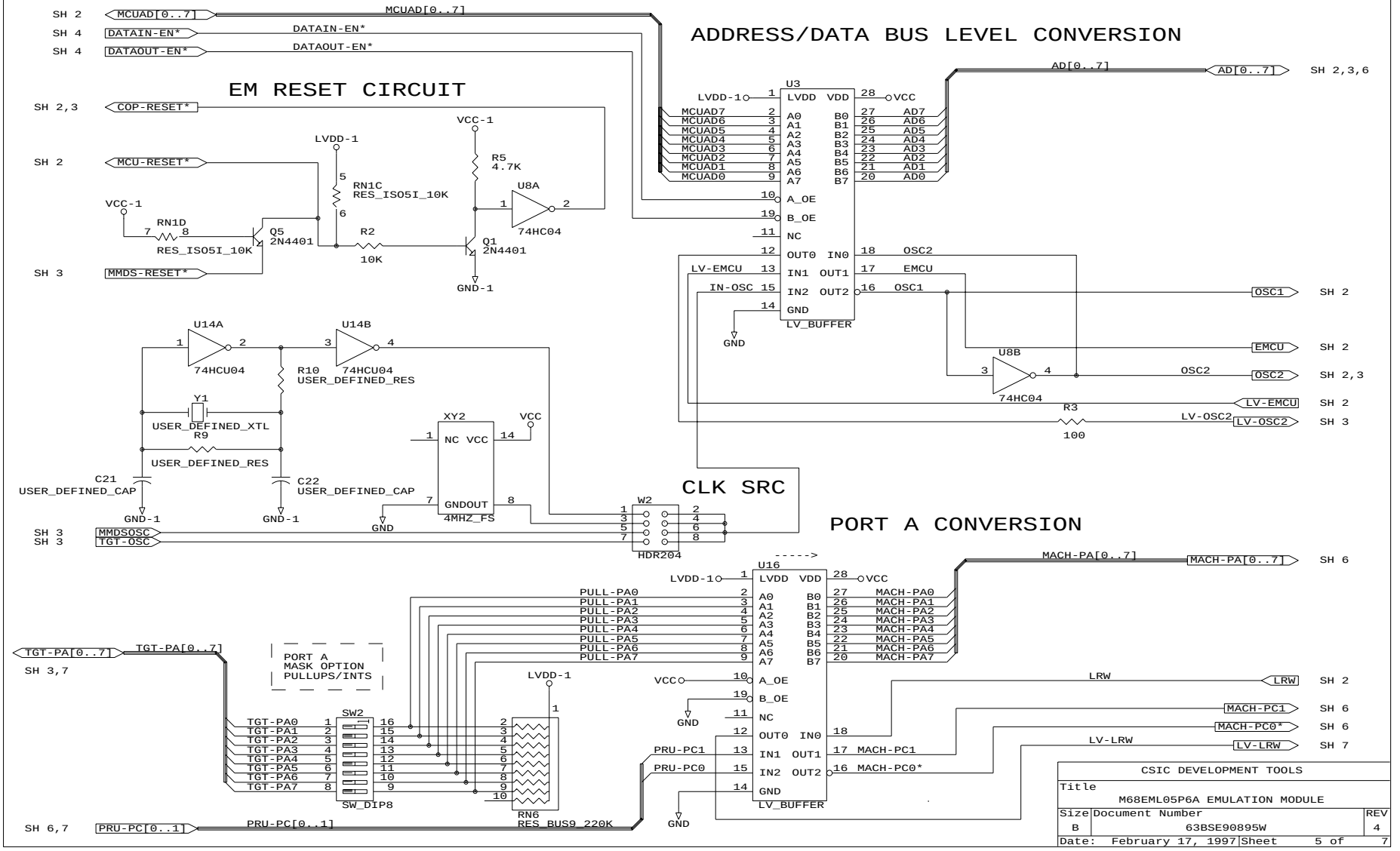
B	63BSE90895W		4
Date:	February 17, 1997	Sheet	4 of 7


ADDRESS/DATA BUS LEVEL CONVERSION
EM RESET CIRCUIT
CLK SRC
PORT A CONVERSION
SH 2 MCUAD[0..7]
MCUAD[0..7]
SH 4 DATAIN-EN*
DATAIN-EN*
SH 4 DATAOUT-EN*
DATAOUT-EN*
SH 2,3 COP-RESET*
SH 2 MCU-RESET*
SH 3 MMDS-RESET*
VCC-1
LVDD-1
RN1C RES_ISO5I_10K
RN1D RES_ISO5I_10K
R5 4.7K
R2 10K
Q5 2N4401
Q1 2N4401
U8A 74HC04
GND-1
U3
LVDD-1
VCC
MCUAD7
MCUAD6
MCUAD5
MCUAD4
MCUAD3
MCUAD2
MCUAD1
MCUAD0
A_OE
B_OE
NC
OUT0 IN0
IN1 OUT1
IN2 OUT2
GND
LV_BUFFER
AD[0..7]
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
LV-EMCU
IN-OSC
OSC2
EMCU
OSC1
U8B 74HC04
R3 100
LV-OSC2
LV-EMCU
U14A 74HCU04
U14B 74HCU04
R10 USER_DEFINED_RES
Y1 USER_DEFINED_XTL
R9 USER_DEFINED_RES
C21 USER_DEFINED_CAP
C22 USER_DEFINED_CAP
XY2 4MHZ_FS
NC VCC
GNDOUT
W2 HDR204
SH 3 MMDSOSC
SH 3 TGT-OSC
GND
TGT-PA[0..7]
SH 3,7
PORT A MASK OPTION PULLUPS/INTS
SW2 SW_DIP8
TGT-PA0
TGT-PA1
TGT-PA2
TGT-PA3
TGT-PA4
TGT-PA5
TGT-PA6
TGT-PA7
RN6 RES_BUS9_220K
PULL-PA0
PULL-PA1
PULL-PA2
PULL-PA3
PULL-PA4
PULL-PA5
PULL-PA6
PULL-PA7
U16
MACH-PA0
MACH-PA1
MACH-PA2
MACH-PA3
MACH-PA4
MACH-PA5
MACH-PA6
MACH-PA7
MACH-PA[0..7]
LRW
MACH-PC1
MACH-PC0*
LV-LRW
PRU-PC1
PRU-PC0
MACH-PC1
MACH-PC0*
SH 6,7 PRU-PC[0..1]
PRU-PC[0..1]
SH 2,3,6
SH 2
SH 2,3
SH 6
SH 7
CSIC DEVELOPMENT TOOLS
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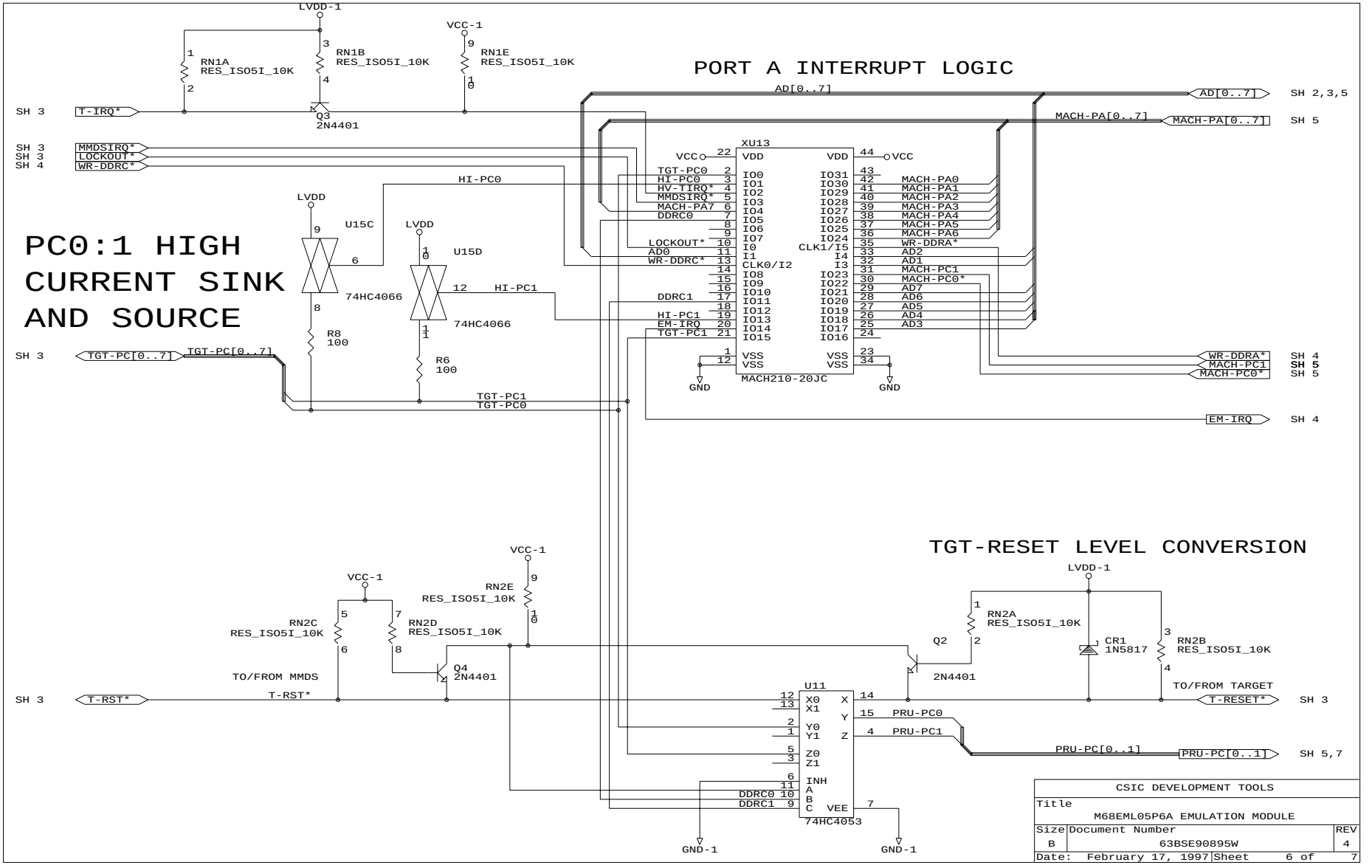
M68EML05P6A EMULATION MODULE
Size B
Document Number 63BSE90895W
REV 4
Date: February 17, 1997
Sheet 5 of 7


PORT A INTERRUPT LOGIC
PC0:1 HIGH CURRENT SINK AND SOURCE
TGT-RESET LEVEL CONVERSION
LVDD-1
VCC-1
RN1A RES_ISO5I_10K
RN1B RES_ISO5I_10K
RN1E RES_ISO5I_10K
Q3 2N4401
SH 3
T-IRQ*
MMDSIRQ*
LOCKOUT*
WR-DDRC*
AD[0..7]
SH 2,3,5
MACH-PA[0..7]
SH 5
XU13
MACH210-20JC
HI-PC0
HI-PC1
LVDD
U15C
U15D
74HC4066
R8 100
R6 100
TGT-PC[0..7]
TGT-PC1
TGT-PC0
WR-DDRA*
MACH-PC1
MACH-PC0*
SH 4
EM-IRQ
RN2A RES_ISO5I_10K
RN2B RES_ISO5I_10K
RN2C RES_ISO5I_10K
RN2D RES_ISO5I_10K
RN2E RES_ISO5I_10K
CR1 1N5817
Q2 2N4401
Q4 2N4401
TO/FROM MMDS
T-RST*
TO/FROM TARGET
T-RESET*
U11
74HC4053
PRU-PC0
PRU-PC1
PRU-PC[0..1]
SH 5,7
GND
GND-1
CSIC DEVELOPMENT TOOLS
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REV 4
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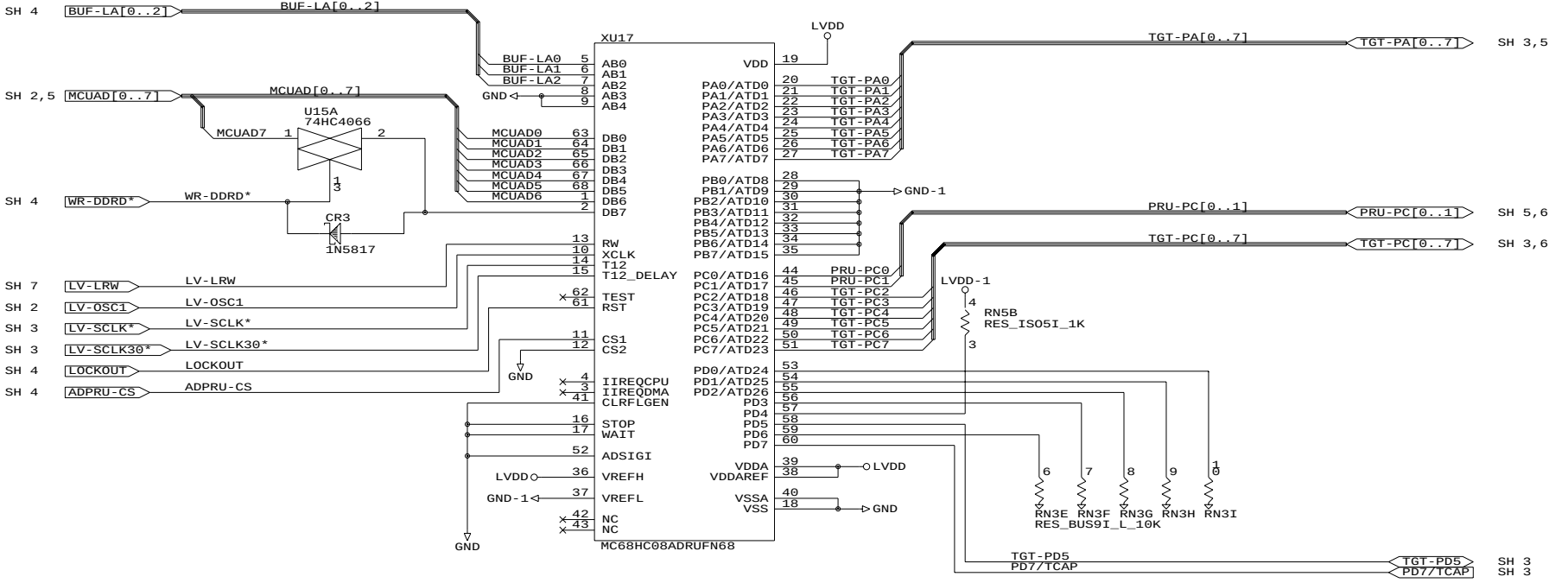
Sheet 6 of 7

A/D PORT REPLACEMENT



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