M68HC11EVBU2/D

April 1998

M68HC11EVBU

UNIVERSAL EVALUATION BOARD

USER'S MANUAL

ADDENDUM

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Introduction

M68HC11EVBU2 is a promotional version of the standard M68HC11EVBU. This document describes the upgrade modifications that have been made to the original.

A 32K byte RAM was added in the wire-wrap area to provide more user memory. This RAM is accessible from address location $8000 through $FFFF except where an on-chip resource has higher priority. The board defaults to normal-expanded mode rather than single-chip mode so this additional RAM can be used.

For the M68HC11EVBU2 normal configuration, the MC68HC11E9 MCU on-chip ROM occupies the address space from $D000 through $FFFF. A factory ROM test pattern uses the 4K from $D000 through $DFFF and the BUFFALO monitor program uses the space from $E000 through $FFFF. The on-chip EEPROM occupies the space from $B600 through $B7FF. The BUFFALO monitor does not use any of this new RAM so the spaces from $8000 through $B5FF and $B800 through $CFFF are available to the user.

On the original M68HC11EVBU board a cut-trace short across jumper header J4 holds the MCU's MODA pin low and forces the board to restart in normal single chip mode. This short has been removed from the M68HC11EVBU2 board so the board normally resets into normal expanded mode. While the EVBU2 is in expanded mode, Ports B and C are defined as a multiplexed address/data bus so these port pins are not available as general purpose I/O pins as they were in the original M68HC11EVBU.

In addition to the 32K x 8 RAM (U7 - MCM60L256), the EVBU2 has a 74HC373 latch (U6) and a 74HC00 quad NAND (U8). The latch de-multiplexes the low order addresses from port C of the MCU. The 74HC00 decodes the select signal for the RAM to map it to the $8000 through $FFFF area of the memory map. Even though the external 32K RAM is selected when the internal ROM is accessed, there is no conflict because the MC68HC11E9 ignores the external data bus during those cycles.

Do not operate the M68HC11EVBU2 board in special expanded test mode with the IRVNE control bit in the HPRIO register set to 1. This mode is requested when the EVBU2 is reset with a shorting jumper installed on J3 and no jumper installed on J4. This could cause a data bus fight between the external RAM data bus drivers and port C during visible internal access cycles. This conflict could interfere with normal operation.

A new cut-trace jumper header (J16) was also added to the EVBU2. A PC board trace normally shorts pins 1 to 2 of this jumper. In the unlikely event that you want to replace the 32K byte RAM (U7) with an 8K byte device, cut the shorting trace between pins 1 and 2 of J16 and short pin 2 to 3 of J16. Pin 1 of an 8K byte RAM is a no-connect and J16 connects a logic 1 to a high-true enable input of an 8K byte RAM. The resulting address decode for the 8K byte RAM would cause it to be mapped at $8000-9FFF, $A000-BFFF, $C000-DFFF, and $E000-FFFF. Although this looks like the same mapping as the 32K device, you could not store different values at

$8000, $A000, $C000, and $E000 because all of these addresses select the same physical byte in the 8K RAM. If you leave the cut-trace short intact on J16 and install an 8K device, it would be mapped at $A000-BFFF and $E000-FFFF (only where A13 and A15 equal 1).

Using Ports B and C as general purpose I/O pins

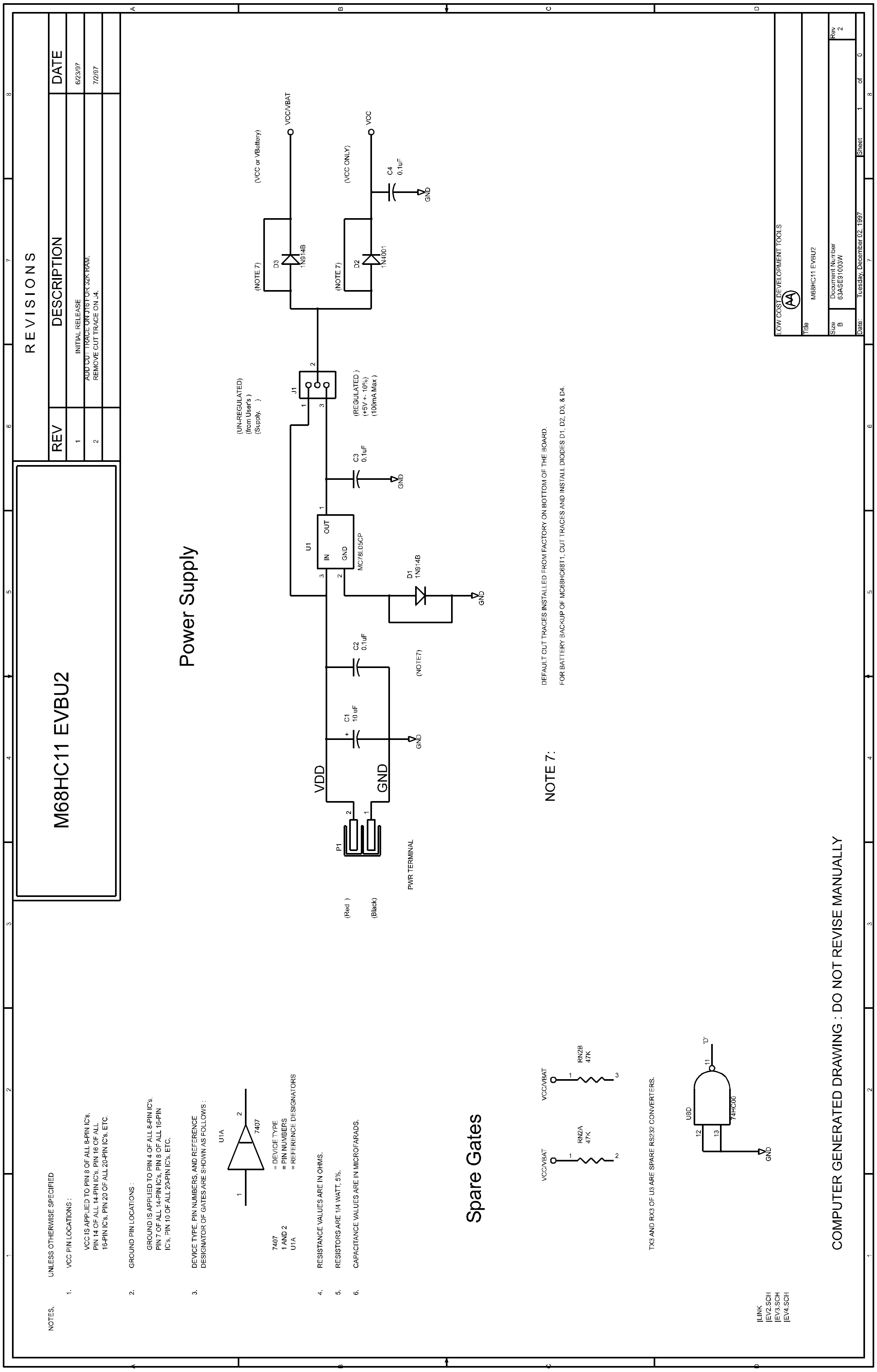
Remove the RAM (U7) from its socket, and place a jumper across jumper header J4. This makes the EVBU2 look just like an unmodified M68HC11EVBU. The jumper on J4 cause the board to reset into single chip mode so ports B and C are general purpose I/O pins rather than being used as the multiplexed address/data bus.

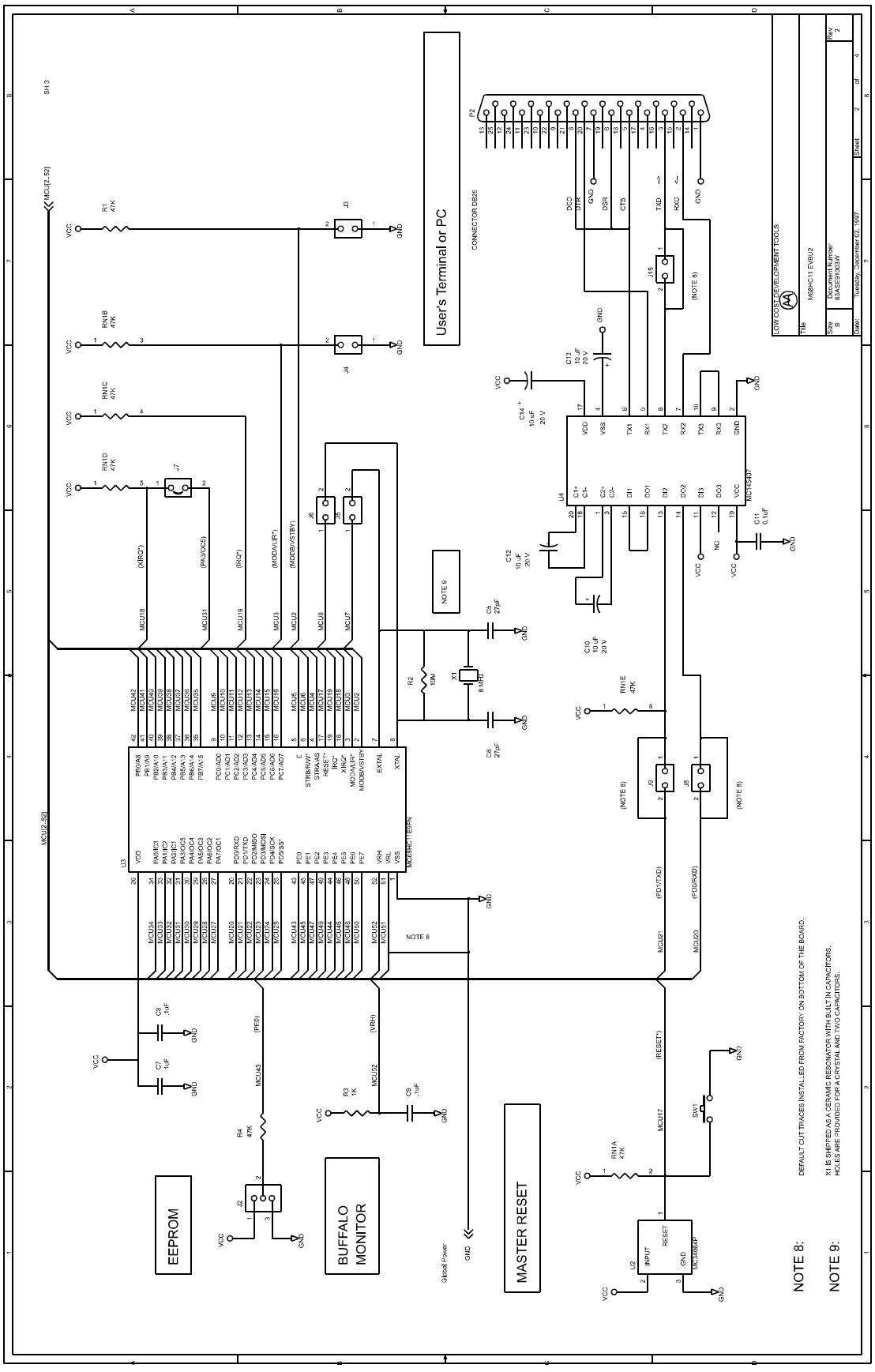
Using PCbug11

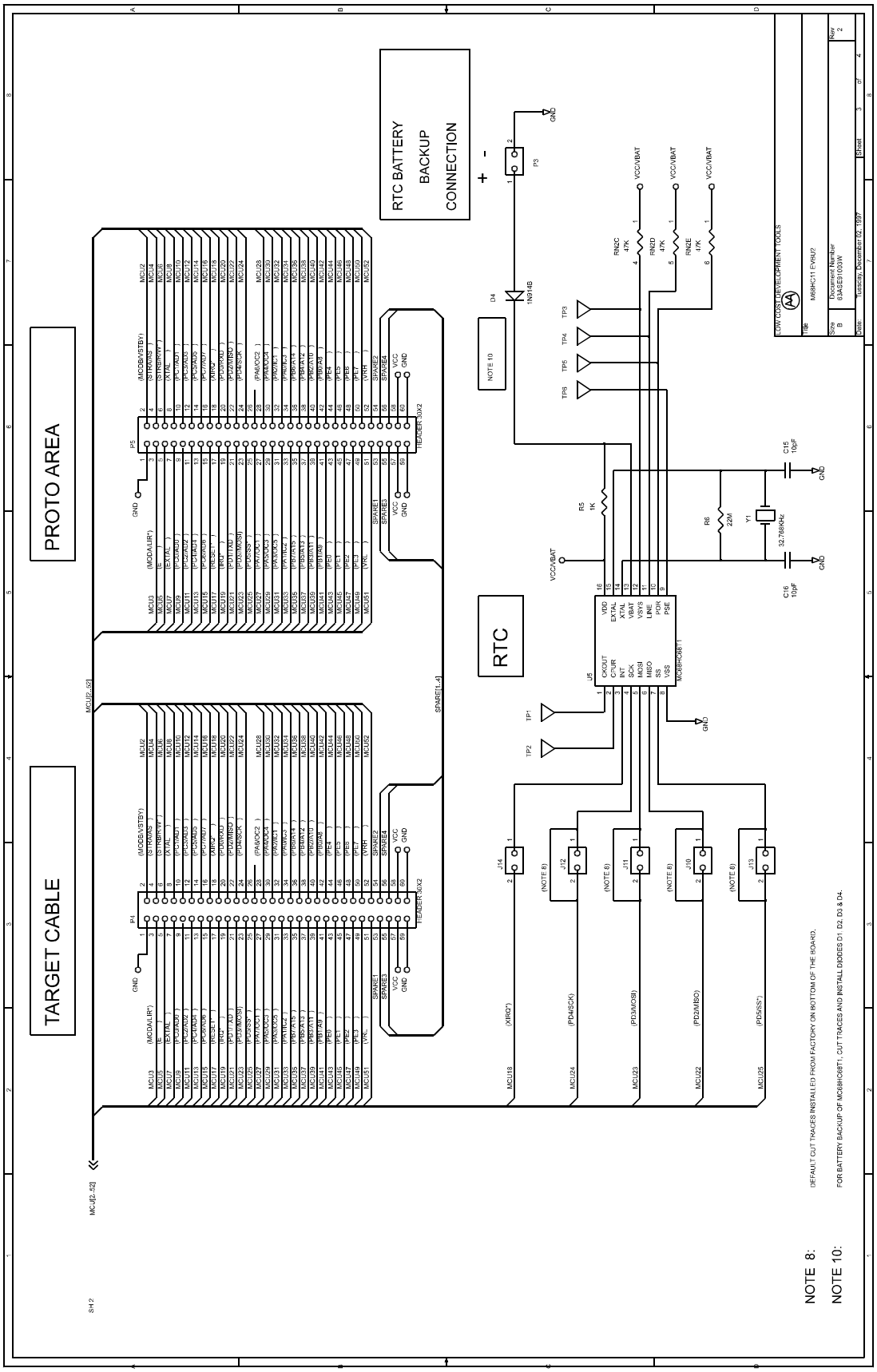
PCbug11 expects the board to be reset in special bootstrap mode, so place jumpers across J3 and J4. When you reset the board, bootstrap mode is selected as PCbug11 expects.

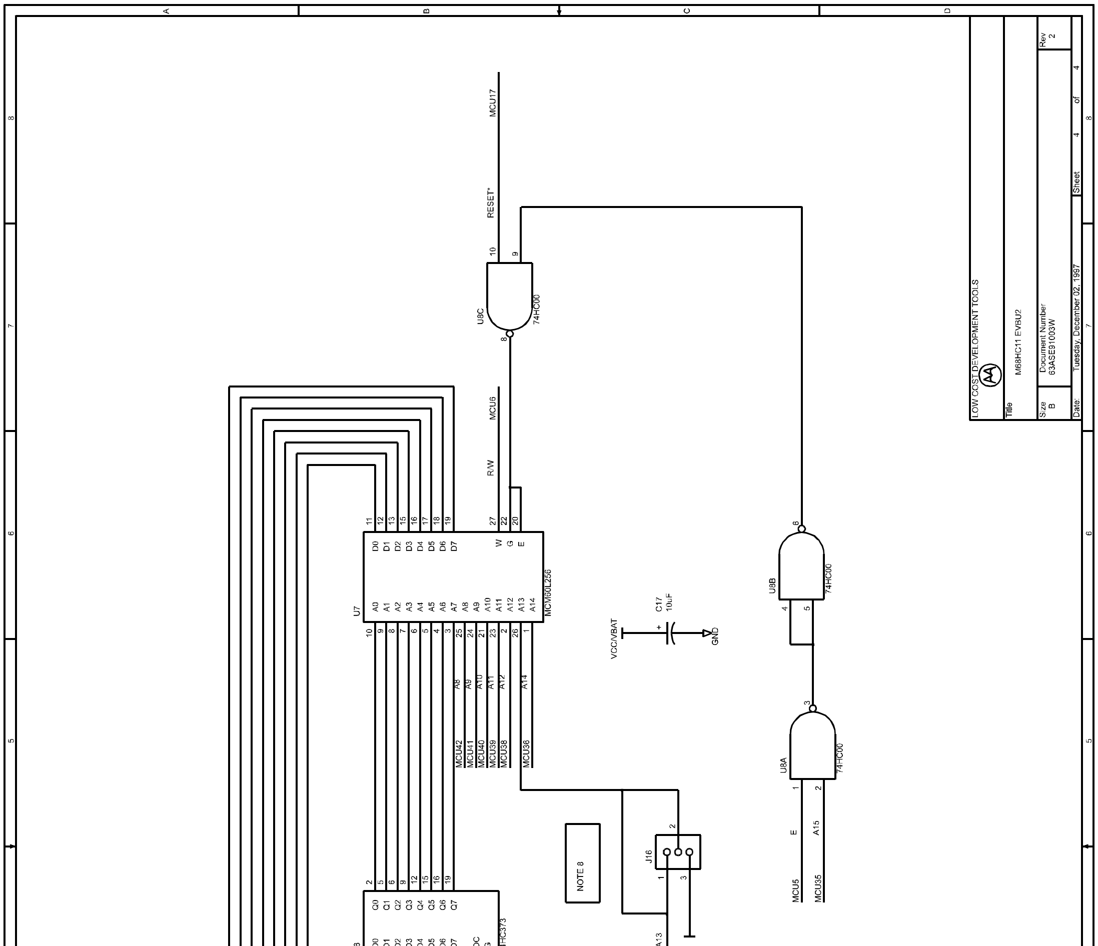
Schematic

A new schematic is provided in the next four pages. The first three pages are identical to the original M68HC11EVBU except the default cut-trace shorting J4 has been removed. Sheet 4 shows the new 32K byte RAM and associated circuitry.


M68HC11 EVBU2
REVISIONS
REV
DESCRIPTION
DATE
1
INITIAL RELEASE
6/23/97
2
ADD CUT TRACE ON J15 FOR 32K RAM.
REMOVE CUT TRACE ON J4.
7/2/97
Power Supply
VDD
GND
P1
PWR TERMINAL
(Red)
(Black)
C1
10 uF
C2
0.1uF
(NOTE7)
U1
MC78L05CP
IN
OUT
GND
D1
1N914B
C3
0.1uF
J1
(UN-REGULATED)
(from User's)
(Supply.)
(REGULATED)
(+5V +- 10%)
(100mA Max)
D3
1N914B
D2
1N4001
(NOTE 7)
(VCC or VBattery)
VCC/VBAT
(VCC ONLY)
VCC
C4
0.1uF
NOTE 7:
DEFAULT CUT TRACES INSTALLED FROM FACTORY ON BOTTOM OF THE BOARD.
FOR BATTERY BACKUP OF MC68HC68T1, CUT TRACES AND INSTALL DIODES D1, D2, D3, & D4.
NOTES:
UNLESS OTHERWISE SPECIFIED
1. VCC PIN LOCATIONS :
VCC IS APPLIED TO PIN 8 OF ALL 8-PIN IC's, PIN 14 OF ALL 14-PIN IC's, PIN 16 OF ALL 16-PIN IC's, PIN 20 OF ALL 20-PIN IC's, ETC.
2. GROUND PIN LOCATIONS :
GROUND IS APPLIED TO PIN 4 OF ALL 8-PIN IC's, PIN 7 OF ALL 14-PIN IC's, PIN 8 OF ALL 16-PIN IC's, PIN 10 OF ALL 20-PIN IC's, ETC.
3. DEVICE TYPE, PIN NUMBERS, AND REFERENCE DESIGNATOR OF GATES ARE SHOWN AS FOLLOWS :
7407 = DEVICE TYPE
1 AND 2 = PIN NUMBERS
U1A = REFERENCE DESIGNATORS
4. RESISTANCE VALUES ARE IN OHMS.
5. RESISTORS ARE 1/4 WATT, 5%.
6. CAPACITANCE VALUES ARE IN MICROFARADS.
Spare Gates
RN2A
47K
RN2B
47K
U8D
74HC00
TX3 AND RX3 OF U3 ARE SPARE RS232 CONVERTERS.
COMPUTER GENERATED DRAWING : DO NOT REVISE MANUALLY
LOW COST DEVELOPMENT TOOLS
M68HC11 EVBU2
Document Number
63ASE91003W
Tuesday, December 02, 1997
Sheet 1 of 8
Rev 2


User's Terminal or PC
CONNECTOR DB25
EEPROM
BUFFALO MONITOR
MASTER RESET
NOTE 8:
DEFAULT CUT TRACES INSTALLED FROM FACTORY ON BOTTOM OF THE BOARD.
NOTE 9:
X1 IS SHIPPED AS A CERAMIC RESONATOR WITH BUILT IN CAPACITORS.
HOLES ARE PROVIDED FOR A CRYSTAL AND TWO CAPACITORS.
LOW COST DEVELOPMENT TOOLS
M68HC11 EVBU2
Document Number
83ASE91003W
Tuesday, December 02, 1997


TARGET CABLE
PROTO AREA
RTC BATTERY BACKUP CONNECTION
RTC
NOTE 8:
DEFAULT CUT TRACES INSTALLED FROM FACTORY ON BOTTOM OF THE BOARD.
NOTE 10:
FOR BATTERY BACKUP OF MC68HC68T1, CUT TRACES AND INSTALL DIODES D1, D2, D3 & D4.


LOW COST DEVELOPMENT TOOLS
Title
M68HC11 EVBU2
Size
B
Document Number
63ASE91003W
Rev
2
Date
Tuesday, December 02, 1997
Sheet
4
of
4
U7
MCM60L256
U8
74HC373
U8A
U8B
U8C
74HC00
C17
10uF
VCC/VBAT
GND
J16
NOTE 8
RESET*
R/W
AS
MCU[2..52]