M68EM05C0UM/D

M68EM05C0

EMULATION MODULE

USER'S MANUAL

MOTOROLA

M68EM05C0

Emulation Module
User's Manual

Table of Contents

General Description

Contents

Introduction

Your M68EM05C0 gives your Motorola development tool the ability to emulate target systems based on the MC68HC05C0 MCUs. By substituting a different emulation module (EM), you can enable your Motorola development tool to emulate other MCUs. Refer to *Motorola's Development Tool Selector Guide*, order number SG173/D, for a complete list of available EMs.

This hardware user's manual explains connection, configuration, and operation information specific to the M68EM05C0 emulation module. The module can be installed in two Motorola development systems. To configure your M68EM05C0 for either an MMDS05 or an MMEVS05/MMEVS08, follow the instructions given in **MMDS/MMEVS Configuration and Operation** on page 17.

Emulation Components

Motorola’s complete emulation system consists of the emulation module described in this manual as well as other separately purchased options described in the following paragraphs.

The following items are included with the M68EM05C0 emulation module:

- **An M68EM05C0 emulation module (EM)** — the printed circuit board that enables system functionality for 05C0 MCUs. The female connectors, on the bottom of the module, mate with male connectors on a development system platform board. The EM also has a connector for the target cable assembly.
- **Configuration software** — 3 1/2-inch diskette containing personality files for this module.

Separately purchased Motorola modular development tool options include:

- **An MMEVS05/MMEVS08 (MMEVS) modular evaluation system** — The MMEVS is an economical development tool that provides real-time in-circuit emulation. The unit's integrated design environment includes an editor, an assembler, a user interface, and a source-level debugging program.
- **An MMDS05 modular development system** — The MMDS is a high-performance development tool that has all the capabilities of the MMEVS. In addition, it also has a bus state analyzer and real-time memory windows.
- **Flex cable target assembly** — Refer to **Target Cable Assemblies** on page 10 for more information.

User supplied components include:

- **Host computer** — see the appropriate development tool user’s manual for minimum requirements.
- **Power supply** — +5 Vdc required for the MMEVS.

Emulation Module Layout

Figure 1 shows the layout of the M68EM05C0. Jumper header W1 lets you select the clock-signal source. W2 configuration determines the port D emulation source. Jumper header W3 selects muxed or non-muxed mode emulation. Jumper header W4 controls internal read visibility. W5 determines where external memory resides.

Target connectors J2 and J3 are the interface to a target system; these connectors use a separately purchased target cable assembly. When you install the M68EM05C0 on the MMDS05, the target cable passes through the slit in the station module enclosure. Connector J1 connects to a logic analyzer.

DIN connectors P1 and P2 connect the EM and a development system platform board.

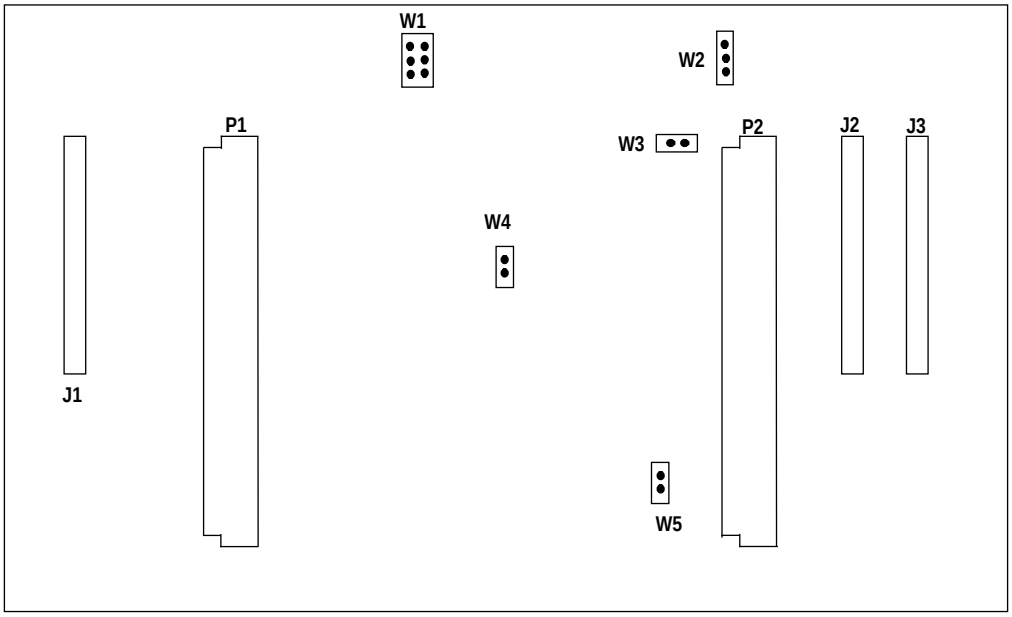


Figure 1. M68EM05C0 Emulation Module

Target Cable Assemblies

To connect your M68EM05C0 to a target system, you need a separately purchased target cable assembly.

The target cable connects to the emulator via connectors J2 and J3 on the M68EM05C0 emulation module. Pin assignments and signal descriptions for connectors J2 and J3 can be found in **Target Cable Connector Pin Assignments** on page 12.

Figure 2 represents a target cable assembly. An assembly consists of a flex cable and a target head adapter. One end of the flex cable plugs onto M68EM05C0 connectors J2 and J3 with orientation shown in **Figure 2**. The other end of the flex cable plugs into the target head adapter. The adapter then inserts into the MCU socket of your target system.

The MCU package in your target system determines the correct flex cable and target head adapter needed:

- For a 44-pin PLCC package, use flex cable M68CBL05C and target head adapter M68TC05C0FN44.
- For a 40-pin DIP package, use flex cable M68CBL05B and target head adapter M68TB05C0P40.
- For a 42-pin SDIP package, use flex cable M68CBL05B and target head adapter M68TB05C0B42.

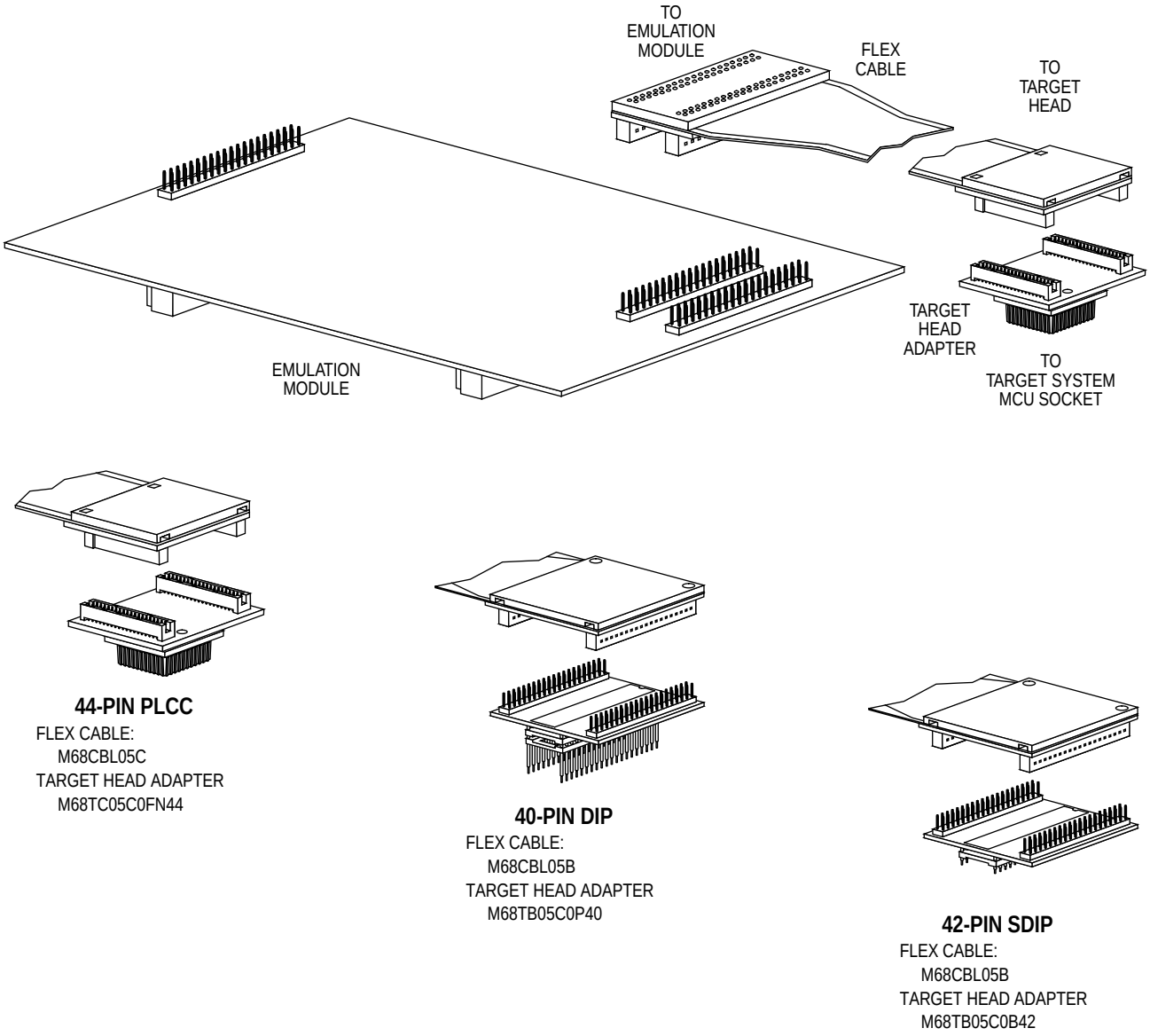


Figure 2. Target Cable Assembly

Connector Information

The reachable connectors on the M68EM05C0 module provide access to the user mode emulation signals (J2 and J3) as well as select internal signals (J1). Connectors J2 and J3 are used for a cable interface to a user's target system, while connector J1 is used to connect a logic analyzer.

Target Cable Connector Pin Assignments

Figure 3 shows the pin assignments for connectors J2 and J3. **Table 1** lists signal descriptions for connector J2; **Table 2** lists signal descriptions for connector J3.

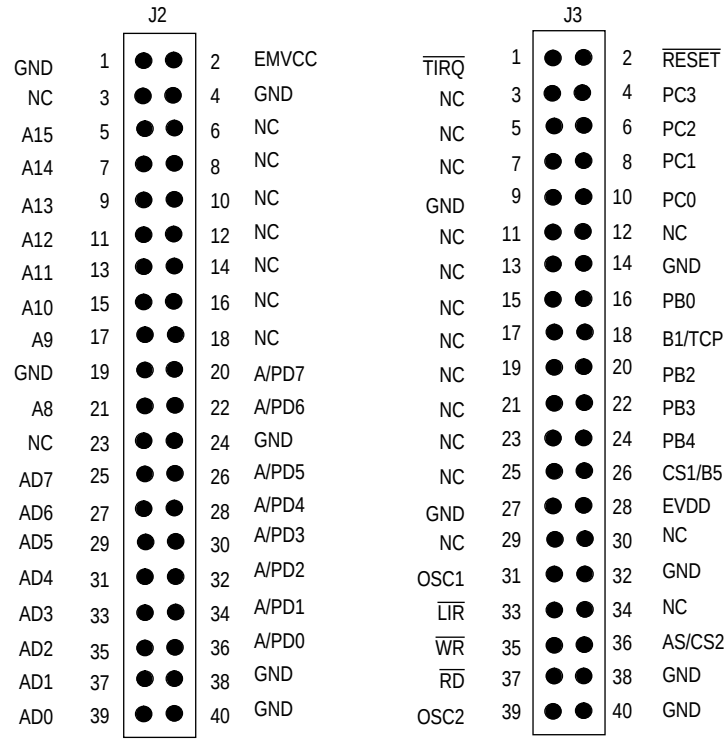


Figure 3. Target Connector Pin Assignment

Table 1. Connector J2 Signal Descriptions

Pin	Mnemonic	Signal
1, 4, 19, 24, 38, 40	GND	GROUND
2	EMV_{CC}	+5 Vdc POWER — Connection to the system voltage V_{CC}
3, 6, 8, 10, 12, 14, 16, 18, 23	NC	No connection
5, 7, 9, 11, 13, 15, 17, 21	$\overline{A15}$, A14–A8	Upper address lines — These upper address lines constitute the upper address byte. $\overline{A15}$ is active low (inverted). A14-A8 are active high.
20, 22, 26, 28, 30, 32, 34, 36	A/PD7–A/PD0	In muxed mode, these lines are port D (bits 7–0) — general-purpose I/O lines controlled by software via data direction and data registers. In non-muxed mode, these lines are the dedicated lower address byte A7–A0.
25, 27, 29, 31, 33, 35, 37, 39	AD7–AD0	In muxed mode, these lines are the multiplexed lower address byte and the data byte. In non-muxed mode, these lines are the data byte.

Table 2. Connector J3 Signal Descriptions

Pin	Mnemonic	Signal
1	$\overline{T\text{-}IRQ}$	TARGET INTERRUPT REQUEST — Active-low input signal from the target that asynchronously applies an MCU interrupt
2	$\overline{RESET}$	Active-low bidirectional signal to/from the target system driven low to pull the MCU into reset
3, 5, 7, 11, 12, 13, 15, 17,19, 21, 23, 25, 29, 30, 34	NC	No connection
4, 6, 8, 10	PC3–PC0	PORT C (bits 3–0) — General-purpose I/O lines controlled by software via data direction and data registers
9,14, 27, 32, 38, 40	GND	GROUND
16	PB0	PORT B bit 0 — General-purpose I/O lines controlled by software via data direction and data registers Becomes the timer compare (TCMP) output pin when the output compare mode feature of the 16-bit timer subsystem is enabled

Table 2. Connector J3 Signal Descriptions (Continued)

Pin	Mnemonic	Signal
18	PB1/TCP	PORT B bit 1 — General-purpose I/O lines controlled by software via data direction and data registers Becomes the timer capture (TCAP) input pin when the input capture mode feature of the 16-bit timer subsystem is enabled
20, 22, 24	PB2, PB3, PB4	PORT B (bits 2, 3, 4) , General-purpose I/O lines controlled by software via data direction and data registers Pins become the RDI, TDO, and SCK lines respectively when serial communication interface subsystem is enabled.
26	$\overline{CS1}$/PB5	CHIP SELECT 1/PORT B 5 — General-purpose I/O lines controlled by software via data direction and data registers Can also be a dedicated chip select line via manipulation of the CS1P1 and CS1P0 bits of the configuration register.
28	EV_{DD}	EXTERNAL VOLTAGE DETECT — Connected to target V_{CC} used to sense target power applied, for target status in MMDS05 status window
31	OSC1	OSCILLATOR 1 — A possible clock source input for the M68EM05C0 board; system bus frequency is OSC1÷4; use of this signal is controlled by jumper header W1.
33	$\overline{LIR}$	LOAD INSTRUCTION REGISTER — Active-low output used to indicate that a fetch of the next opcode is in progress. Note that the mode is not latched on the emulator, but is controlled via jumper header W3.
35	$\overline{WR}$	WRITE — Active-low output used to indicate that a write cycle is in progress
36	AS/$\overline{CS2}$	ADDRESS STROBE/CHIP SELECT 2 — In muxed mode, this pin is the address strobe signal. In non-muxed mode, this pin is the active-low chip select 2 signal.
37	$\overline{RD}$	READ — Active-low output used to indicate that a read cycle is in progress
39	OSC2	OSCILLATOR 2 — Output clock signal. Inversion of the OSC1 clock.

Logic Analyzer Connector Pin Assignments

Figure 4 shows the pin assignments for logic analyzer connector J1. This connector provides the emulator easy access to many of the signals used internally. **Table 3** lists signal descriptions for this connector.

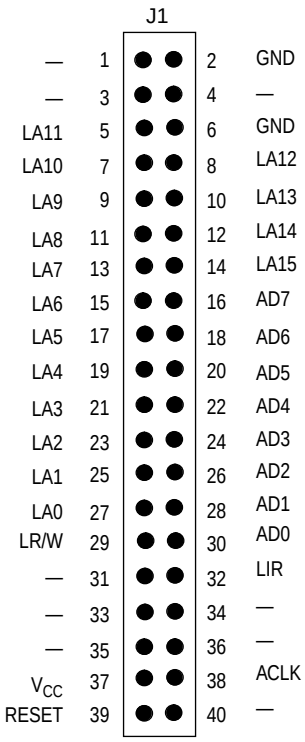


Figure 4. Connector J1 Pin Assignments

Table 3. Logic Analyzer Connector J1 Signal Descriptions

Pin	Mnemonic	Signal
1, 3, 4, 31, 33, 34, 35, 36, 40	NC	No connection
2, 6	GND	GROUND
14, 12, 10, 8	LA15–LA12	LATCHED ADDRESSES (bits 15–12) — MCU latched output address bus
5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27	LA11–LA0	LATCHED ADDRESSES (bits 11–0) — MCU latched output address bus
16, 18, 20, 22, 24, 26, 28, 30	AD7–AD0	DATA BUS (bits 7–0) — MCU multiplexed I/O bus
29	LR/$\overline{W}$	LATCHED READ/WRITE — The MCU's write signal is latched and used on the emulator to control emulator memory accesses.
32	$\overline{LIR}$	LOAD INSTRUCTION REGISTER — Active low signal indicating an opcode fetch cycle is in process.
37	V_{CC}	+5 Vdc POWER — Connection to the system voltage V_{CC}
38	ACLK	ANALYZER CLOCK — The latched addresses are valid on the latched address bus at the rising edge of ACLK. Also, data is valid on the AD BUS at ACLK's rising edge.
39	$\overline{RESET}$	RESET — Active-low signal; will be asserted during internally or externally caused resets

MMDS/MMEVS Configuration and Operation

Contents

Introduction

The following paragraphs explain how to configure and use your M68EM05C0 as part of an MMDS or MMEVS system. For other parts of system installation and configuration, see either the *MMDS05 Operations Manual* (MMDS05OM/D) or *MMEVS05/MMEVS08 Operations Manual* (MMEVS0508OM/D).

The topics covered in this chapter are:

- **Setting M68EM05C0 Jumper Headers** on page 19 explains how to set the M68EM05C0 jumper headers.
- **Personality Files Usage** on page 23 discusses the personality file usage on the M68EM05C0 board.
- **MC68HC05C0 Emulation** on page 24 explains special considerations for emulating with this module.
- **Remaining System Installation** on page 26 covers the final steps to system installation.

NOTE: *You can configure an M68EM05C0 already installed in the system platform board. To do so, remove system power and then follow the guidance of this chapter.*

CAUTION: *Be sure to switch off power before you reconfigure an installed EM. Reconfiguring EM jumper headers with the power on can damage emulation circuits.*

Setting M68EM05C0 Jumper Headers

Your M68EM05C0 has five jumper headers — W1 through W5. The following explains how to configure these components.

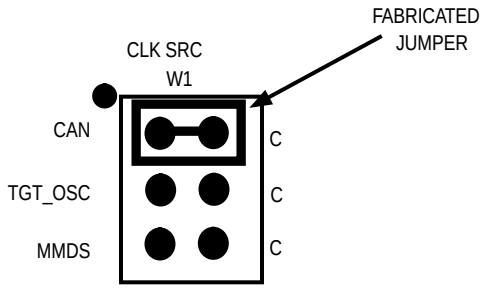
Clock Source Select Header, W1

Jumper header W1 determines the source of the clock signal. The diagram here illustrates the jumper header where the pins marked C indicate common pins. The default configuration selects the 16-MHz canned oscillator clock source (at board location Y1).

The other possible clock sources are one originating from the platform board or a user supplied clock source coming through target cable connected to J2 and J3. For the platform board source clock, reposition the W1 jumper between pins MMDS and C, then use the system's OSC command to select a frequency. For a user supplied source, reposition the W1 jumper between pins TGT_OSC and C.

NOTE: *The user supplied source should be a CMOS level square wave.*

NOTE: *In muxed mode, 8 MHz is the maximum OSC1 frequency (2-MHz bus speed). In non-muxed mode, 16 MHz is the maximum rated OSC1 frequency (4-MHz bus).*

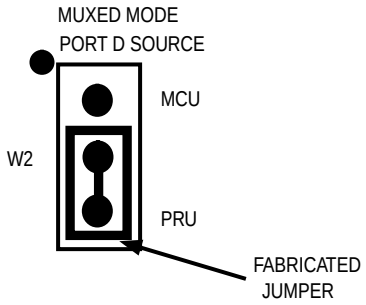


Port D Source Select Header, W2

The port D source header controls the muxed mode port D source for the M68EM05C0 emulation module. The proper configuration for this jumper is determined by the version of MC68HC05C0 silicon used as the resident MCU and installed in the XU11 socket on the M68EM05C0 board.

For first pass silicon, the port D I/O logic is rebuilt external to the MCU using a port replacement unit (PRU). The W2 jumper should be in the PRU position. In this position, the port D keyscan interrupts feature is not available in emulation.

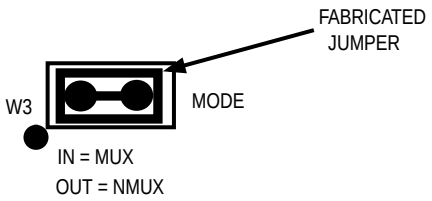
For later versions of silicon, the emulator uses port D I/O logic on the resident MCU. The W2 jumper should be in the MCU position. The keyscan interrupts feature is supported with this configuration.



Mode Select Header, W3

Jumper header W3 controls the mode the resident MC68HC05C0 MCU will operate in. When the jumper is installed, the MCU will come out of reset in muxed mode. The data is multiplexed with the lower order address bits in this mode.

Non-muxed mode is entered out of reset if the jumper is removed from the header. In this mode, address and data have individual, separate lines.

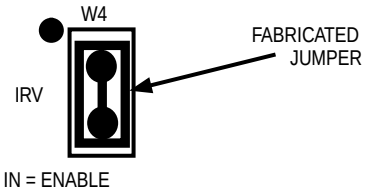


Internal Read Visibility (IRV) Header, W4

The internal read visibility jumper enables both the internal read visibility (IRV) and load instruction register visibility (LIRV) bits of the configuration register. That is, to emulate these bits being set or cleared, you should configure this jumper appropriately instead of modifying the associated bits in the configuration register (CNFGR).

NOTE: *In emulation, both bits are controlled by this one jumper and are either both set or both cleared.*

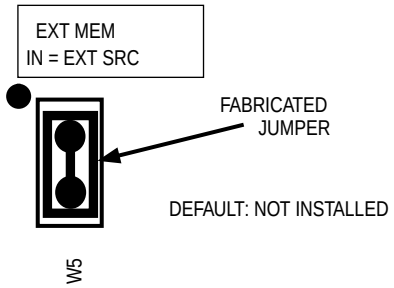
When the jumper is installed, internal read visibility is enabled. The $\overline{RD}$, $\overline{WR}$, $\overline{LIR}$ and chip selects will be active during internal location accesses. When the jumper is removed, the control signals will not be active for internal location accesses.



When internal read visibility is disabled, the user should be aware of functional differences between emulation and an MCU being used in a user's system. In emulation, the address and data pins will continue to be driven with the internal access address and data. When an MCU is placed in a user's system and internal visibility is disabled, an internal access will cause the address pins to be driven with the last accessed external address. The data pins (or muxed address/data pins) are driven to the last external data.

External Memory Select Header, W5

Jumper header W5 determines where the external memory range $0240-$FFFF resides. The default position, with the jumper removed, will use the RAM residing on the control board. If the jumper is installed, the user should connect external memory to the emulator through a target cable connected to J2 and J3.



NOTE: *The 0-page external range $001C–$003F will always be accessed from an external source. The user is required to connect this external memory to the emulator through the target cable.*

Personality Files Usage

Your MMDS or MMEVS development system uses a specific personality file to emulate an MC68HC05C0 MCU: file 00023Vxx.MEM. This file is on an individual disk shipped with the M68EM05C0. This file name follows the pattern for all personality files, **`00ZZZVxx.MEM`**, where **`ZZZ`** is the EM identifier of MCU name and **`xx`** is the version of the file.

System software loads a default personality file upon power-up. If you use the M68EM05C0 on the MMDS or MMEVS, file 00023Vxx.MEM is the default.

The default version of personality file will assign RAM and ROM as follows:

RAM $40–$23F

ROM: $0240–$FFFF

The purpose of memory definitions is seen in the way the emulator handles writes to the two types of memory. During user code execution, attempts to write to a location mapped as ROM will generate a write protect error and user code execution is halted; code should never write to a ROM location. However, a write to a location mapped as RAM does not stop code execution.

With an understanding of MMDS/MMEVS handling of memory mapping, the user can customize the memory map to emulate application needs. The memory settings can be altered using the system's SETMEM command.

The 0-page external range from $001C to $003F cannot be configured as RAM or ROM using the SETMEM command. It is mapped as an external source and will attempt to access memory/registers from the user's system through the target cable connected to J2 and J3.

MC68HC05C0 Emulation

NOTE: *Be aware that the COP is enabled out of reset.*

Be aware that several bits in the configuration register (CNFGR) are one-time writable. Each bit should be configured properly on the first write to the CNFGR register after any reset.

The following paragraphs detail differences between the performance of an MC68HC05C0 MCU run in single-chip operation and the way certain features will perform during emulation.

Port D Pullups/ Interrupts

In single-chip mode operation:

Port D can be configured to generate interrupts on port pins pulled low.

In emulation:

The source for port D emulation is controlled by the W2 jumper. If you are using first pass silicon in the resident MCU (socket XU11) and the W2 jumper is in the PRU position, then the port D keyscan interrupt functions are not supported in emulation.

Keyscan interrupt functions are supported in emulation with later silicon and the W2 jumper placed in the MCU position.

Mode Selection

In single-chip mode operation:

The state of the LIR/MODE pin during a power-on reset selects the mode the MCU will run in: muxed or non-muxed.

In emulation:

The MCU mode is selected by the jumper position of W3 on the M68EM05C0 module.

IRV and LIRV Operation and the Configuration Register

In single-chip mode operation:

The IRV bit defaults to 0 and internal cycles are not visible externally until the IRV bit in the CNFGR register is set.

The LIRV bit defaults to 0 and the LIR signal is not driven out until the LIRV bit in the CNFGR register is set.

When internal read visibility is disabled, the control signals (RD, WR, and the chip select lines) will not be active during an internal access. External address pins will be driven to the value of the last external access address and the data pins will be driven to the last external data.

In emulation:

The IRV and LIRV are defaulted to 1 and must remain a logic 1. Writes to the CNFGR register should always leave these bits set.

The IRV jumper (W4 on the M68EM05C0) can be used to control the control signals ($\overline{\text{LIR}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, and the chip select lines) driven out during an internal access cycle. If the jumper is installed, the control signals will be driven to the target. Note that even if the internal read visibility is disabled by removing the W4 jumper, the address and data lines of the internal cycle will still be visible to the target system in emulation.

Pullup on $\overline{\text{IRQ}}$

In single-chip mode operation:

There is no pullup on the $\overline{\text{IRQ}}$ pin. Your application must pull the $\overline{\text{IRQ}}$ pin to V_{DD} level to prevent interrupts.

In emulation:

The $\overline{\text{IRQ}}$ pin is pulled up on the module. Be aware that an application without the $\overline{\text{IRQ}}$ pin pulled high will emulate correctly but will fail in the application because of a floating IRQ line. The $\overline{\text{IRQ}}$ pin pulled high on the module causes these results.

Remaining System Installation

When you have configured headers W1–W5, you have completed M68EM05C0 configuration:

- Ensure that the power to the development tool is off.
- If installing the M68EM05C0 in an MMDS05 station module, remove the panel from the station module top.
- Fit together EM connectors P1 and P2 (on the bottom of the board) and platform board DIN connectors. Snap the corners of the EM onto the plastic standoffs.
- Connect the target cable, if appropriate.
- If installing in an MMDS05, replace the panel.

At this point, you are ready to make remaining cable connections, as necessary, and restore power.

For instructions, consult either the *MMEVS05/MMEVS08 Operations Manual* (MMEVS0508OM/D) or *MMDS05 Operations Manual* (MMDS05OM/D).

Schematics

Contents

M68EM05C0 Schematics

Refer to the following pages for the five sheets of schematics for the M68EM05C0 emulation module.

M68EM05C0 Schematics (Sheet 1 of 5)

NOTES, UNLESS OTHERWISE SPECIFIED

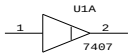
1. VCC PIN LOCATIONS :

   VCC IS APPLIED TO PIN 8 OF ALL 8-PIN IC's, PIN 14 OF ALL 14-PIN IC's, PIN 16 OF ALL 16-PIN IC's, PIN 20 OF ALL 20-PIN IC's, ETC.

2. GROUND PIN LOCATIONS :

   GROUND IS APPLIED TO PIN 4 OF ALL 8-PIN IC's, PIN 7 OF ALL 14-PIN IC's, PIN 8 OF ALL 16-PIN IC's, PIN 10 OF ALL 20-PIN IC's, ETC.

3. DEVICE TYPE, PIN NUMBERS, AND REFERENCE DESIGNATOR OF GATES ARE SHOWN AS FOLLOWS :



7407 = DEVICE TYPE
1 AND 2 = PIN NUMBERS
U1A = REFERENCE DESIGNATORS

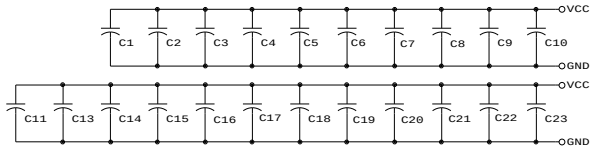
4. RESISTANCE VALUES ARE IN OHMS.
5. RESISTORS ARE 1/4 WATT, 5%, UNLESS OTHERWISE SPECIFIED.
6. CAPACITANCE VALUES ARE IN MICROFARADS.

M68EM05C0 EMULATION MODULE

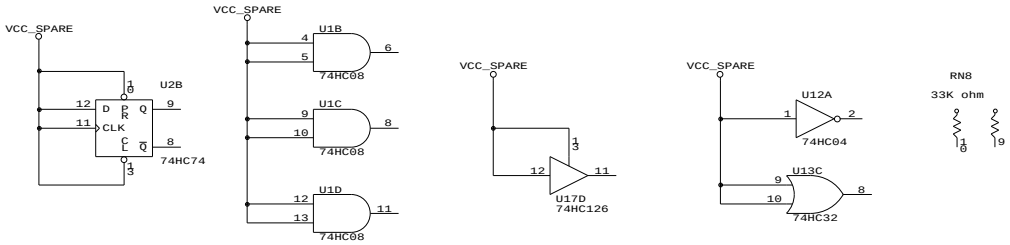
REVISIONS

ECN #	PCB REV	SCH REV	DESCRIPTION	DATE
69	A	2	Bring in target clock source. Modify LRW signal to control board. Bring FG signal into MACH.	12/8/94
	B	3	New REV of PWB	5/31/95

Decouple Caps for ICs.
All caps are 0.1 uF @ 50V,10%



Spare Gates



LINK
05C0R3S2.SCH
05C0R3S3.SCH
05C0R3S4.SCH
05C0R3S5.SCH

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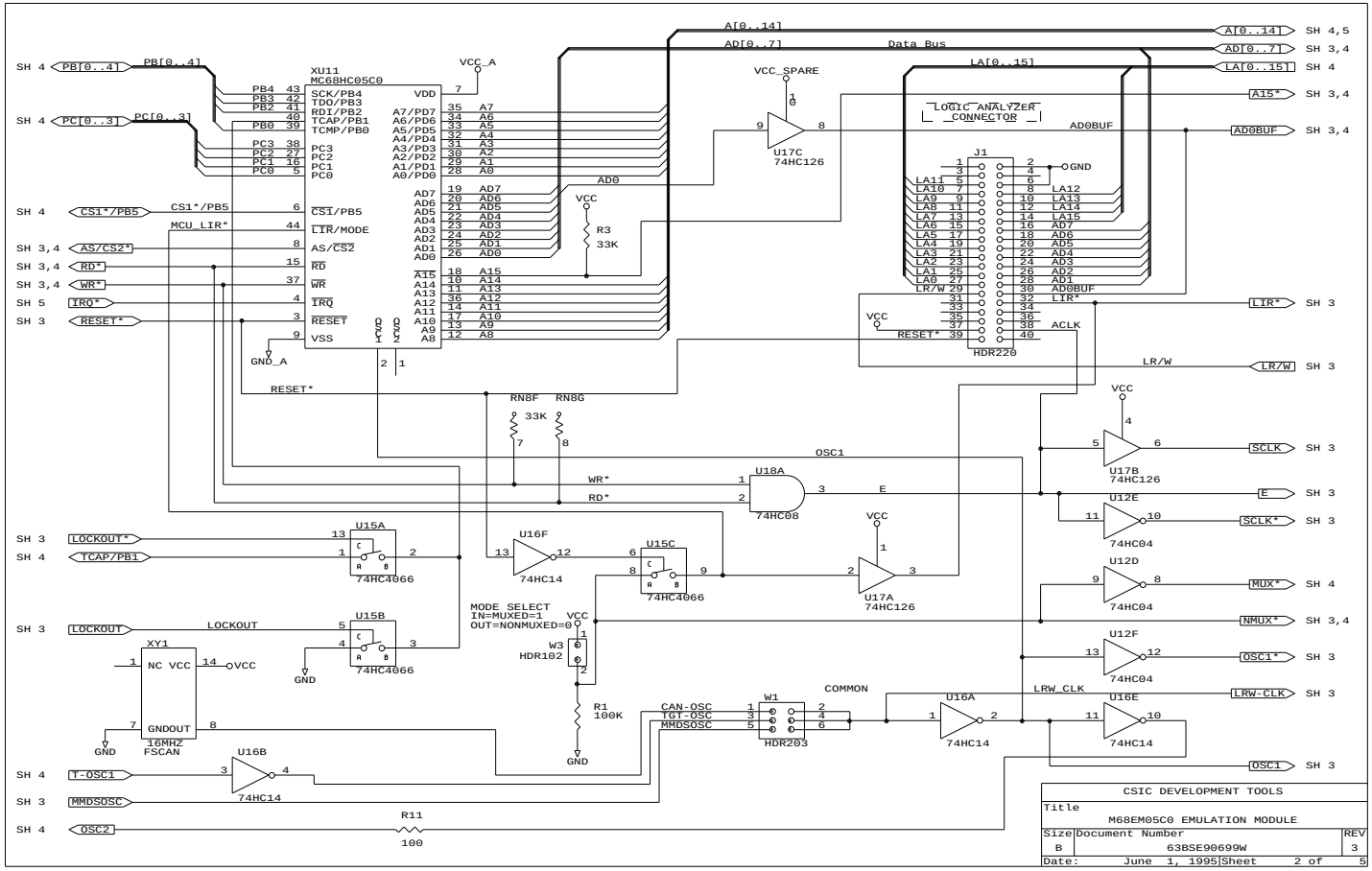
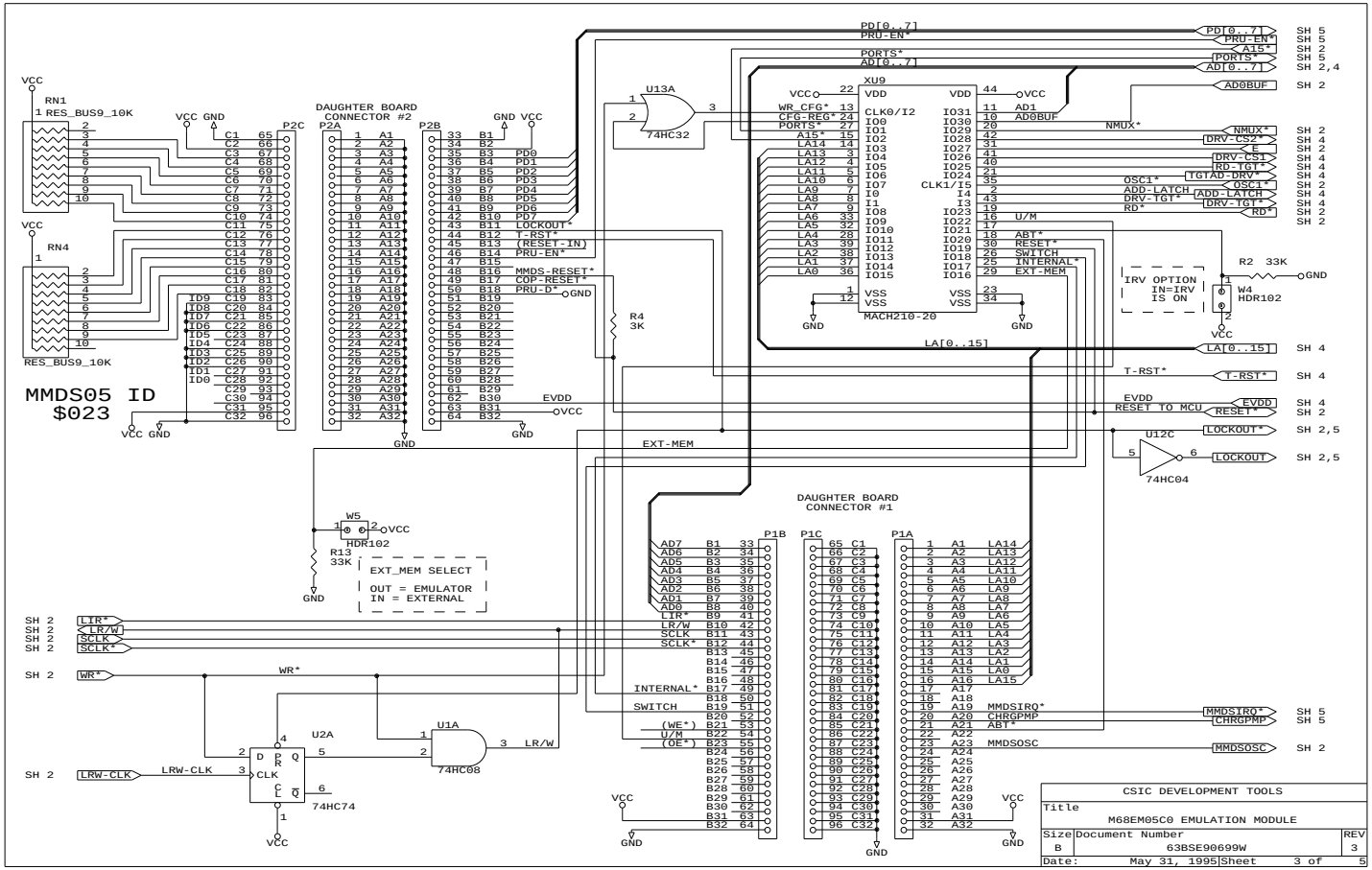
CSIC DEVELOPMENT TOOLS		
Title: M68EM05C0 EMULATION MODULE		
Size: B	Document Number: 63BSE90699W	REV: 3
Date: June 2, 1995	Sheet 1 of 5	

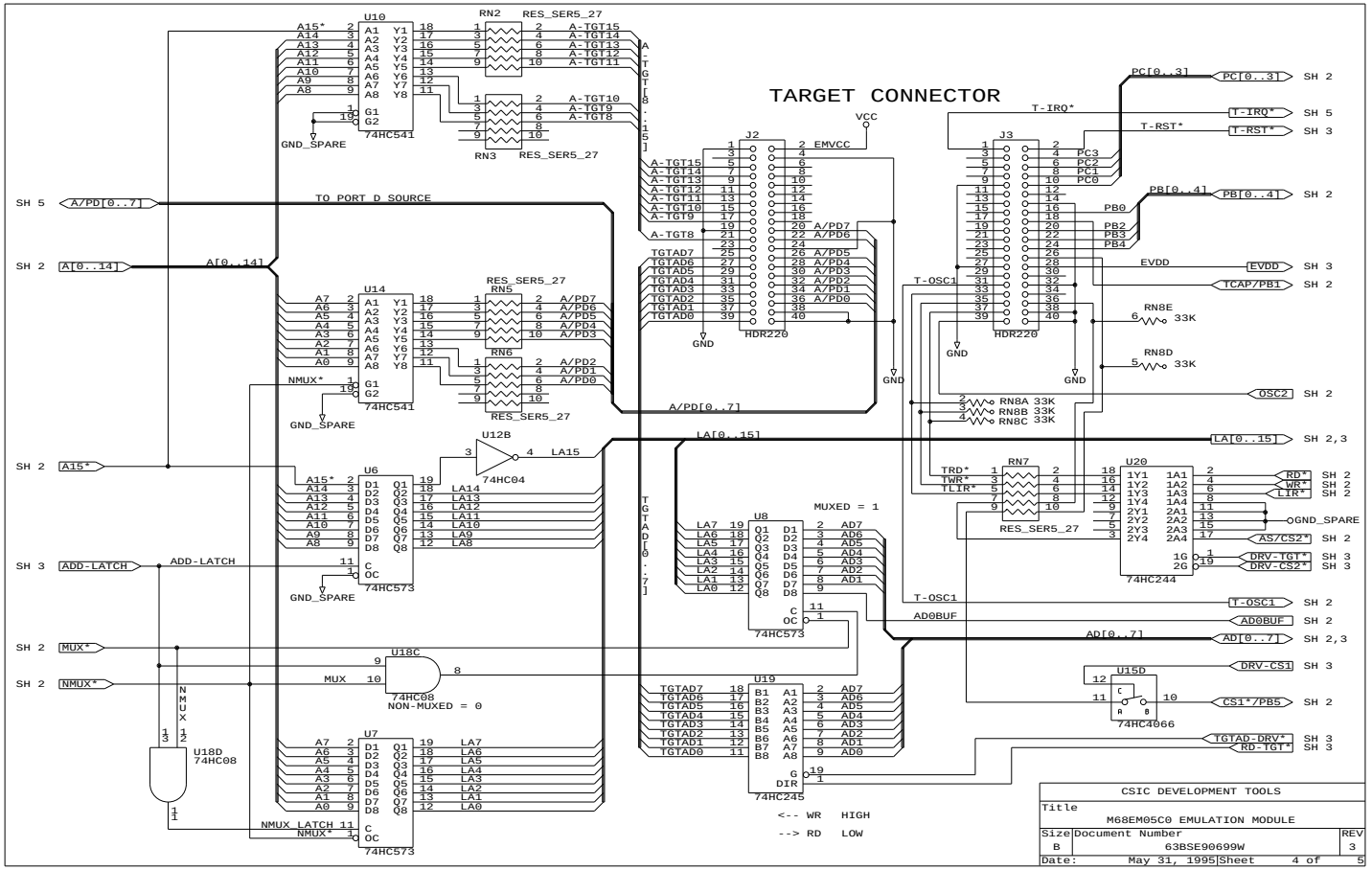
M68EM05C0 Schematics (Sheet 2 of 5)



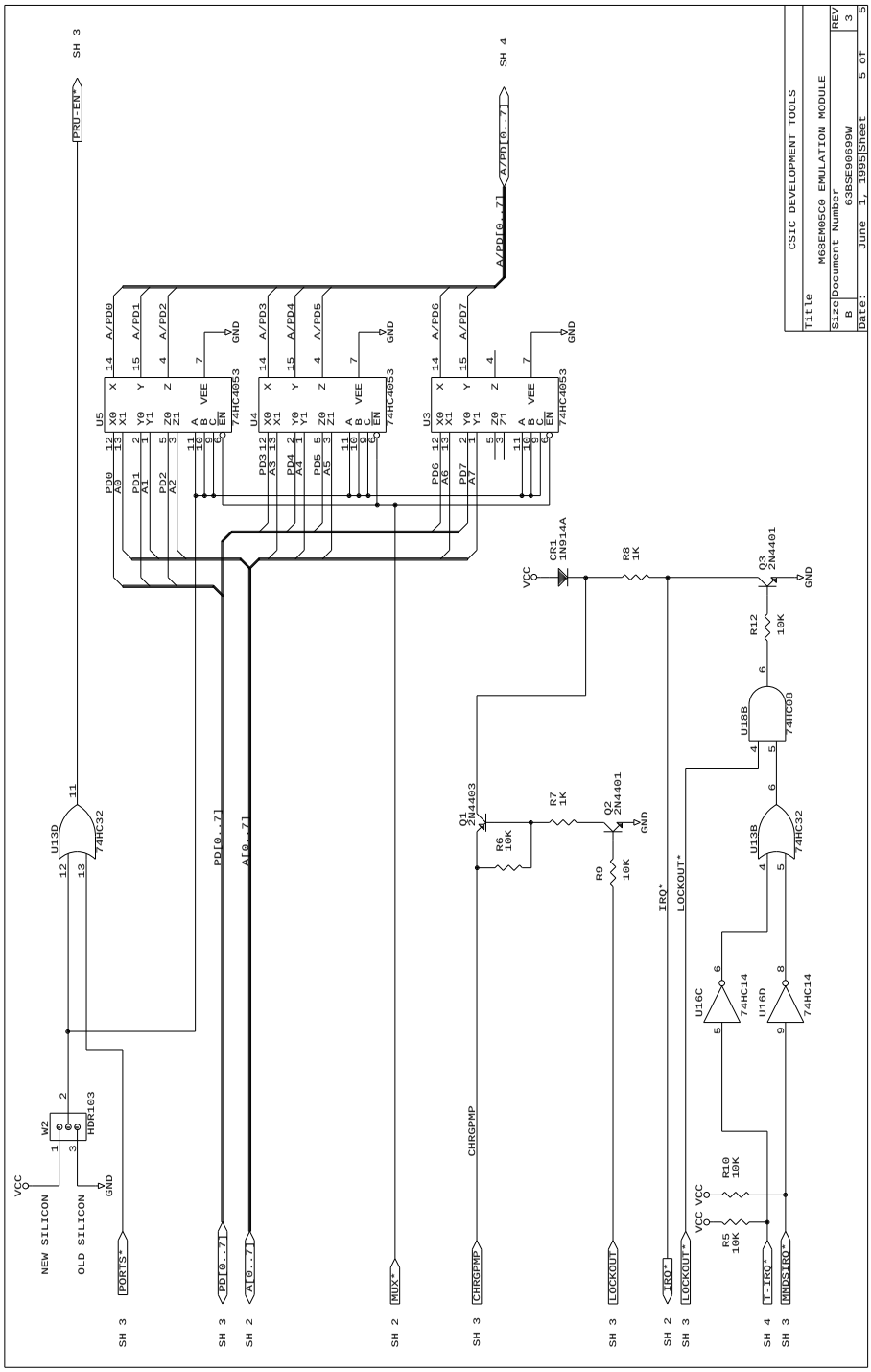
M68EM05C0 Schematics (Sheet 3 of 5)



M68EM05C0 Schematics (Sheet 4 of 5)



M68EM05C0 Schematics (Sheet 5 of 5)



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INTERNET: http://Design-NET.com

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