M68EM05E5

Emulation Module
User's Manual

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Revision History

This table summarizes differences between this revision and the previous revision of this emulation module user's manual.

Previous Revision	None
Current Revision	Original Release
Date	09/96

Revision History

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General Description

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Introduction

The M68EM05E5 gives your Motorola development tool the ability to emulate target systems based on MC68HC(7)05E5 and MC68HC(7)05E1 microcontroller units (MCUs). By substituting a different emulation module (EM), the Motorola development tool can be enabled to emulate other MCUs. Refer to *Motorola's Development Tool Selector Guide*, Motorola order number SG173/D, for a complete list of available EMs.

This hardware user's manual explains connection, configuration, and operation information specific to the M68EM05E5 emulation module. The module can be installed in two Motorola development systems. To configure your M68EM05E5 for either an MMDS or an MMEVS, follow the instructions given in **MMDS/MMEVS Configuration and Operation** on page 19.

Emulation Components

Motorola’s complete emulation system consists of the emulation module described in this manual as well as other separately purchased options described in the following paragraphs.

These items are included with the M68EM05E5 emulation module:

- **An M68EM05E5 emulation module (EM)** — The printed circuit board that enables system functionality for MC68HC(7)05E5 MCUs. The female connectors, on the bottom of the module, mate with male connectors on a development system platform board.
- **Configuration software** — 3 1/2-inch diskette containing personality files for this module.

Separately purchased Motorola modular development tool options include:

- **An MMEVS platform board (M68MMPFB0508)** — The MMEVS is an economical development tool that provides real-time in-circuit emulation. The unit's integrated design environment includes an editor, an assembler, a user interface, and a source-level debugging program.
- **An MMDS0508 modular development system (M68MMDS0508)** — The MMDS is a high-performance development tool that has all the capabilities of the MMEVS. In addition, it also has a bus state analyzer and real-time memory windows.
- **Flex cable target assembly** — Refer to **Target Cable Assemblies** on page 12 for more information.

User-supplied components include:

- **Host computer** — See the appropriate development tool user’s manual for minimum requirements.
- **Power supply** — +5 Vdc is required for the MMEVS.

Emulation Module Layout

Figure 1 shows the layout of the M68EM05E5. Jumper header J1 lets you select the clock-signal source.

Target connector P4 is the interface to a target system; this connector uses a separately purchased cable assembly. When the M68EM05E5 is installed in the MMDS, the target cable passes through the slit in the station module enclosure. Connector P1 connects to an optional logic analyzer.

The resident MCU, an MC68HC705E5, is installed in the socket at U5. DIN connectors P2 and P3 connect the EM and a development system platform board.

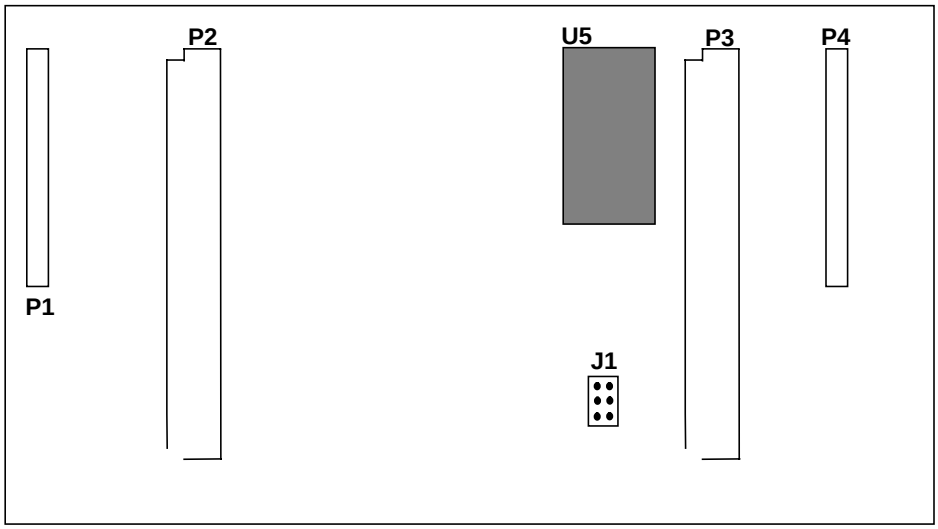


Figure 1. M68EM05E5 Emulation Module

Target Cable Assemblies

To connect the M68EM05E5 to a target system, you need a separately purchased target cable assembly. Cable assemblies support MC68HC(7)05E5 and MC68HC(7)05E1 emulation and are available for two MCU packages: plastic dual in-line (DIP) and small outline integrated circuit (SOIC).

The target cable connects to the emulator via connector P4 on the M68EM05E5 emulation module. Pin assignments and signal descriptions for connector P4 can be found in **Target Cable Connector Pin Assignments** on page 14.

Figure 2 represents a target cable assembly. An assembly for 28-pin DIP packages consists of a flex cable and a target head adapter. The assembly for 28-pin SOIC packages requires an additional SOIC adapter. One end of the flex cable plugs onto M68EM05E5 connector P4 with orientation shown in **Figure 2**. The other end of the flex cable plugs into the target head adapter. The target head adapter then inserts into either a DIP footprint in a target system or into the SOIC adapter.

The MCU package in the target system determines the target cable assembly components required:

- For a 28-pin DIP package, use flex cable M68CBL05A and target head adapter M68TA05P9P28.
- For a 28-pin SOIC package, use the flex cable assembly for the 28-pin DIP in conjunction with SOIC adapter M68DIP28SOIC.

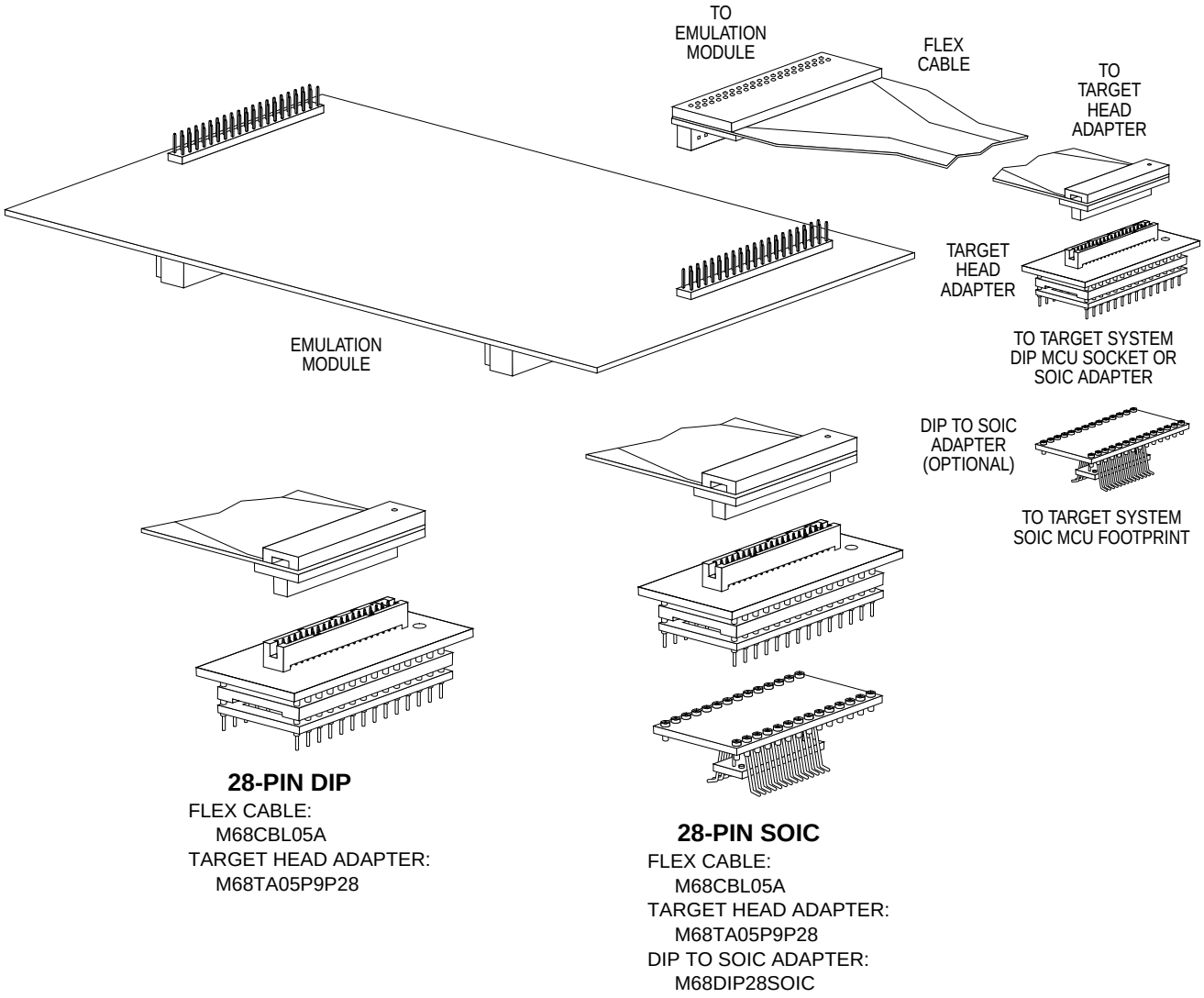


Figure 2. Target Cable Assembly

Connector Information

The connectors on the M68EM05E5 module provide access to the user mode emulation signals (P4) as well as select internal signals (P1). Connector P4 is used for a cable interface to a user's target system, while connector P1 is used to connect a logic analyzer.

Target Cable Connector Pin Assignments

Figure 3 shows the pin assignments for connector P4. **Table 1** lists signal descriptions for connector P4.

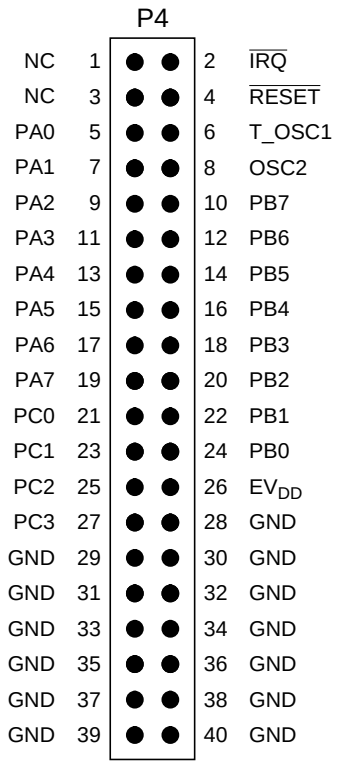


Figure 3. Target Connector Pin Assignment

Table 1. Connector P4 Signal Descriptions

Pin	Mnemonic	Signal
1, 3	NC	No connection
2	$\overline{\text{IRQ}}$	TARGET INTERRUPT REQUEST – Active-low input signal from the target that asynchronously applies an MCU interrupt
4	$\overline{\text{RESET}}$	Active-low bidirectional signal to/from the target system driven low to pull the MCU into reset.
5, 7, 9, 11, 13, 15, 17, 19	PA0–PA7	PORT A (Bits 0–7) – General-purpose I/O lines controlled by software via data direction and data registers
6	T_OSC1	OSCILLATOR 1 – A possible clock source input for the M68EM05E5 module. Use of this signal is controlled by jumper header J1.
8	OSC2	OSCILLATOR 2 – Inverted/Buffered output of the OSC1 clock source selected via jumper header J1
10, 12	PB7, PB6	PORT B (Bits 7 and 6) – General-purpose I/O lines controlled by software via data direction and data registers Becomes the serial clock line (SCL) and serial data line (SDA) connections to the MCU when the M-bus subsystem is enabled
14, 16, 18	PB5, PB4, PB3	PORT B (Bits 5, 4, 3) – General-purpose I/O lines controlled by software via data direction and data registers Pins become the SDIO, SCK, and TIPL lines respectively when the synchronous serial interface subsystem is enabled.
20, 22, 24	PB2, PB1, PB0	PORT B (Bits 2, 1, 0) – General-purpose I/O lines controlled by software via data direction and data registers
21, 23, 25, 27	PC0–PC3	PORT C (Bits 3–0) – General-purpose I/O lines controlled by software via data direction and data registers
28-40	GND	GROUND

Logic Analyzer Connector Pin Assignments

Figure 4 shows the pin assignments for logic analyzer connector P1. This connector provides the emulator easy access to many of the signals used internally. **Table 2** lists signal descriptions for this connector.

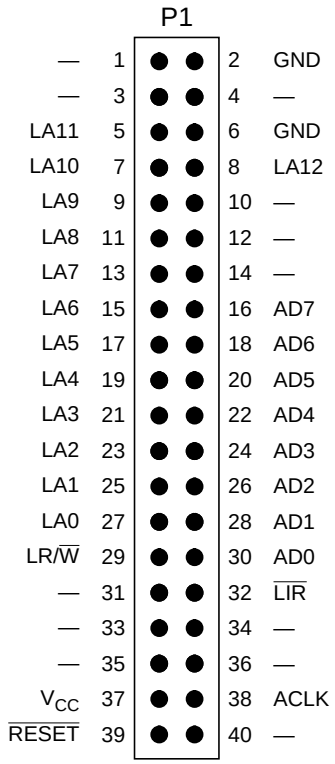


Figure 4. Connector P1 Pin Assignments

Table 2. Logic Analyzer Connector P1 Signal Descriptions

Pin	Mnemonic	Signal
1, 3, 4, 10, 12, 14, 31, 33, 34, 35, 36, 40	NC	No connection
2, 6	GND	GROUND
8	LA12	LATCHED ADDRESSES (Bit 12) — MCU latched output address bus
5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27	LA11–LA0	LATCHED ADDRESSES (Bits 11–0) — MCU latched output address bus
16, 18, 20, 22, 24, 26, 28, 30	AD7–AD0	DATA BUS (Bits 7–0) — MCU multiplexed I/O bus
29	LR/$\overline{W}$	LATCHED READ/WRITE — The MCU's write signal is latched and used on the emulator to control emulator memory accesses.
32	$\overline{LIR}$	LOAD INSTRUCTION REGISTER — Active-low signal indicating an opcode fetch cycle is in process
37	V_{CC}	+5 Vdc POWER — Connection to the system voltage V_{CC}
38	ACLK	ANALYZER CLOCK — The latched addresses are valid on the latched address bus at the rising edge of ACLK. Also, data is valid on the AD bus at ACLK's rising edge.
39	$\overline{RESET}$	RESET — Active-low signal; will be asserted during internally or externally caused resets

General Description

MMDS/MMEVS Configuration and Operation

Contents

Introduction

The following paragraphs explain how to configure and use the M68EM05E5 as part of an MMDS or MMEVS system. For other parts of system installation and configuration, see either the *MMEVS05/MMEVS08 Operations Manual* (MMEVS0508OM/D) or *MMDS0508 Operations Manual* (MMDS0508OM/D).

The topics covered in this chapter are:

- **Setting M68EM05E5 Jumper Headers** on page 21 explains how to set the M68EM05E5 jumper headers.
- **Remaining System Installation** on page 23 covers the final steps to system installation.
- **Personality Files Usage** on page 24 discusses the personality file used on the M68EM05E5 board.
- **Emulation Specifics** on page 25 explains special considerations for emulating with this module.

NOTE: *You can configure an M68EM05E5 already installed in the system platform board. To do so, remove system power and then follow the guidance of this chapter.*

CAUTION: *Be sure to switch off power before you reconfigure an installed EM. Reconfiguring EM jumper headers with the power on can damage emulation circuits.*

Setting M68EM05E5 Jumper Headers

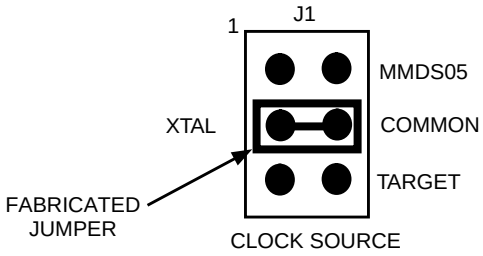
The M68EM05E5 has one jumper header – W1. **Table 3** provides a quick reference for configuration options. Refer to the paragraphs that follow for a more detailed explanation.

Table 3. Jumper Header Positions

Jumper Header	Position	Description	Factory Setting
Clock Source Select, J1		Select a user-supplied clock source. The clock is input to connector P4 through a target cable assembly.	
		Select the clock originating from the development system platform board. The frequency is controlled by the OSC command and is 2 MHz on power-up.	
		Select the 32.768-kHz crystal located on the EM board at Y1.	X

Clock Source Select Header – J1

Jumper header J1 determines the clock signal source. The diagram below illustrates the jumper header where the pin marked COMMON is always connected to one of the three clock source pins via the fabricated jumper. The default configuration, between XTAL and COMMON, selects the 32.768-kHz crystal clock source at board location Y1.



There are two other possible clock sources. To use the one originating from the development system platform, reposition the J1 jumper header between the MMDS05 and COMMON pins. Then use the system's OSC command to select a frequency.

For a user-supplied clock source, coming through the target cable connected to P4, reposition the J1 jumper header between the TARGET and COMMON pins.

NOTE: *The user-supplied source through the target cable should be a CMOS-level square wave.*

Remaining System Installation

When header J1 has been configured, M68EM05E5 configuration is complete.

- Ensure that the power to the development tool is off.
- If installing the M68EM05E5 in an MMDS station module, remove the panel from the station module top.
- Fit together EM connectors P2 and P3 on the bottom of the board and platform board DIN connectors. Snap the corners of the EM onto the plastic standoffs.
- Connect the target cable, if appropriate.
- If installing in an MMDS, replace the panel.

At this point, you are ready to make remaining cable connections, as necessary, and restore power.

For instructions, consult either the *MMEVS05/MMEVS08 Operations Manual* (MMEVS0508OM/D) or *MMDS0508 Operations Manual* (MMDS0508OM/D).

Personality Files Usage

The personality files needed for the M68EM05E5 module are on an individual disk included with the EM board. The development system uses a specific personality file to emulate an MC68HC(7)05E5 MCU: file 00027Vxx.MEM. The debugger software loads this personality file upon power up.

NOTE: *Personality file names follow the pattern 00ZZZVxx.MEM, where ZZZ is the EM identifier or MCU name and xx is the version of the file.*

To emulate MC68HC(7)05E1 MCUs, another personality file needs to be loaded after the debugger software is running. To emulate the MC68HC(7)05E1, use the system's LOADMEM command to load file 005E1Vxx.MEM.

Emulation Specifics

NOTE: *Be aware that if the computer operating properly (COP) mask option has been selected as enabled, your code must clear the COP watchdog timer counter to avoid a COP reset. The counter is cleared by writing a logic 0 to bit 0 at location $1FF0. This should be the first check when code is not operating as expected.*

Selecting mask options for emulation requires programming using a dedicated programmer.

Also note that the two pins associated with the Motorola bus (M bus) interface subsystem, the serial data line (SDA) and serial clock line (SCL), require that all devices connected to these pins be open-drain or open-collector outputs. Your target system should also have external pullup resistors for each pin. You can populate these pullup resistors on the M68EM05E5 emulation module at locations R2 and R3. R2 is the SCL pullup resistor and R3 is the SDA pullup resistor.

The following information details known differences between the performance of an MC68HC705E5 MCU run in single-chip operation versus the way certain features will perform during emulation.

$\overline{\text{IRQ}}/V_{PP}$ $\overline{\text{Input Pin}}$

In single-chip mode operation:

The $\overline{\text{IRQ}}/V_{PP}$ pin drives the asynchronous IRQ interrupt function of the CPU. The pin also is used for programming voltage when programming the user EPROM or the MOR.

In emulation:

The $\overline{\text{IRQ}}/V_{PP}$ signal supplied to connector P4 through a target cable drives only the asynchronous IRQ interrupt function. A V_{PP} voltage should not be supplied to the $\overline{\text{IRQ}}/V_{PP}$ pin in a target application while the emulator is connected.

Pullup on $\overline{IRQ}$

In single-chip mode operation:

There is no pullup on the $\overline{IRQ}$ pin. Your application must pull the $\overline{IRQ}$ pin to V_{DD} level to prevent interrupts.

In emulation:

The $\overline{IRQ}$ pin is pulled up on the module. Be aware that an application without the $\overline{IRQ}$ pin pulled high will emulate correctly but will fail in the application because of a floating IRQ line. The $\overline{IRQ}$ pin pulled high on the module causes these results.

Illegal Address Operation

In single-chip mode operation:

An opcode fetch from an illegal address (not RAM or ROM) will generate a system reset.

In emulation:

An opcode fetch from an illegal address (not RAM or ROM) does **not** generate a system reset. While code is executed in an illegal range, bit 3 of reserved location $001F will be set. Once the opcode address is no longer in an illegal range, the bit will be cleared.

Schematics

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M68EM05E5 Schematics

The following pages contain four sheets of schematics for the M68EM05E5 emulation module.

Schematics

M68EM05E5 Schematics (Sheet 1 of 4)

M68EM05E5
EMULATION MODULE

REVISIONS				
ECN #	PCB REV	SCH REV	DESCRIPTION	DATE

NOTES, UNLESS OTHERWISE SPECIFIED

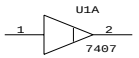
1. VCC PIN LOCATIONS :

   VCC IS APPLIED TO PIN 8 OF ALL 8-PIN IC's, PIN 14 OF ALL 14-PIN IC's, PIN 16 OF ALL 16-PIN IC's, PIN 20 OF ALL 20-PIN IC's, ETC.

2. GROUND PIN LOCATIONS :

   GROUND IS APPLIED TO PIN 4 OF ALL 8-PIN IC's, PIN 7 OF ALL 14-PIN IC's, PIN 8 OF ALL 16-PIN IC's, PIN 10 OF ALL 20-PIN IC's, ETC.

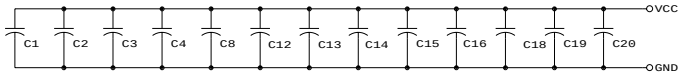
3. DEVICE TYPE, PIN NUMBERS, AND REFERENCE DESIGNATOR OF GATES ARE SHOWN AS FOLLOWS :



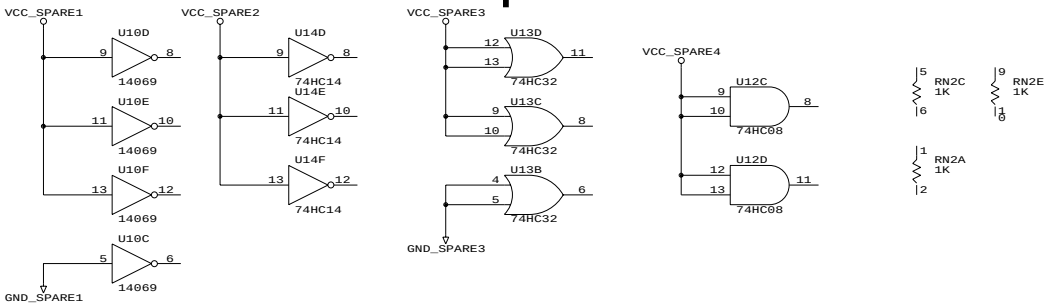
7407 = DEVICE TYPE
1 AND 2 = PIN NUMBERS
U1A = REFERENCE DESIGNATORS

4. RESISTANCE VALUES ARE IN OHMS.
5. RESISTORS ARE 1/4 WATT, 5%, UNLESS OTHERWISE SPECIFIED.
6. CAPACITANCE VALUES ARE IN MICROFARADS, 10%.

Decouple Caps for ICs as labeled.
All caps are 0.1 uF @ 50 V



Spare Gates



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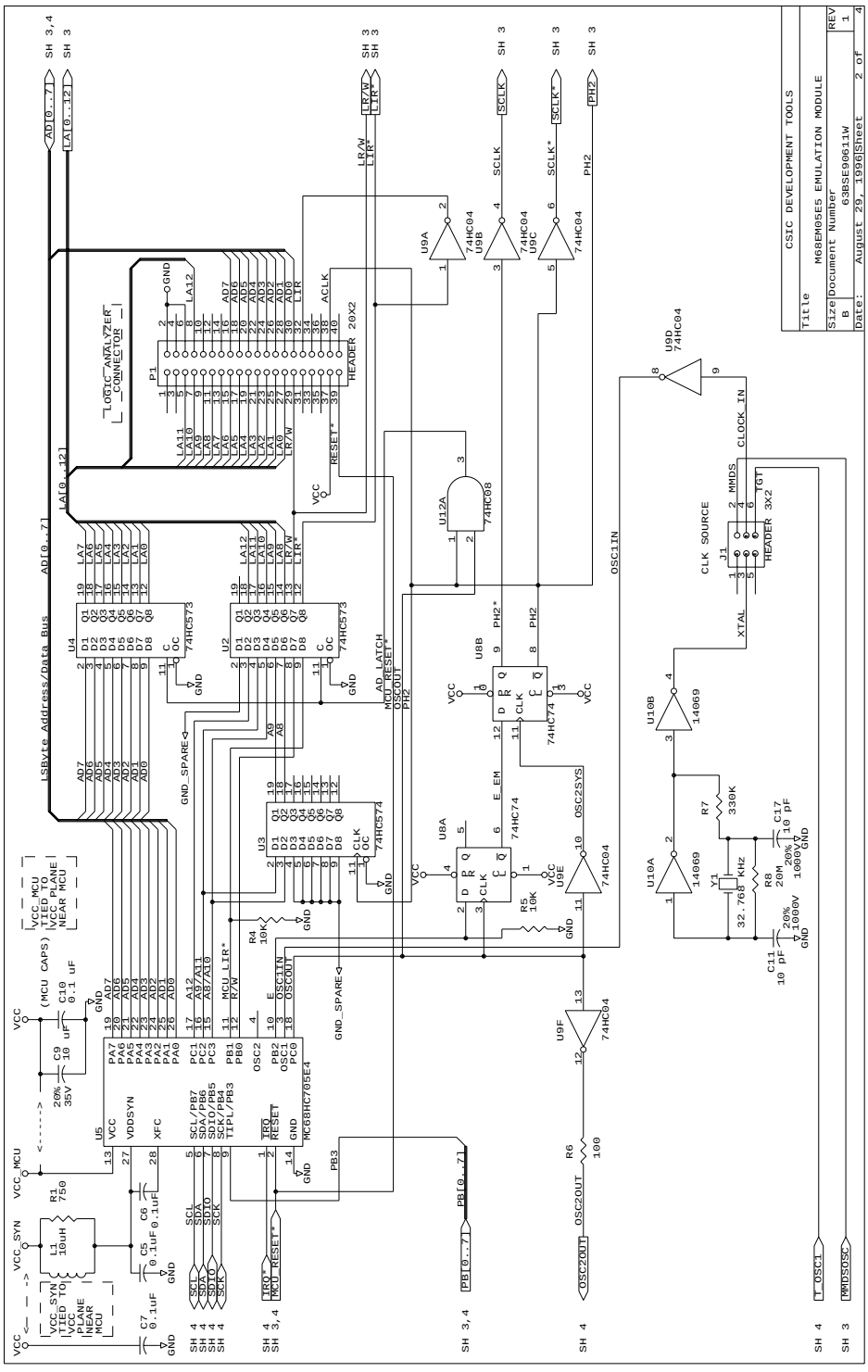
LINK
05E5R1S2.SCH
05E5R1S3.SCH
05E5R1S4.SCH

COMPUTER GENERATED DRAWING : DO NOT REVISE MANUALLY

CSIC DEVELOPMENT TOOLS		
Title: M68EM05E5 EMULATION MODULE		
Size: B	Document Number: 63BSE90611W	REV: 1
Date: August 29, 1996	Sheet 1 of 4	

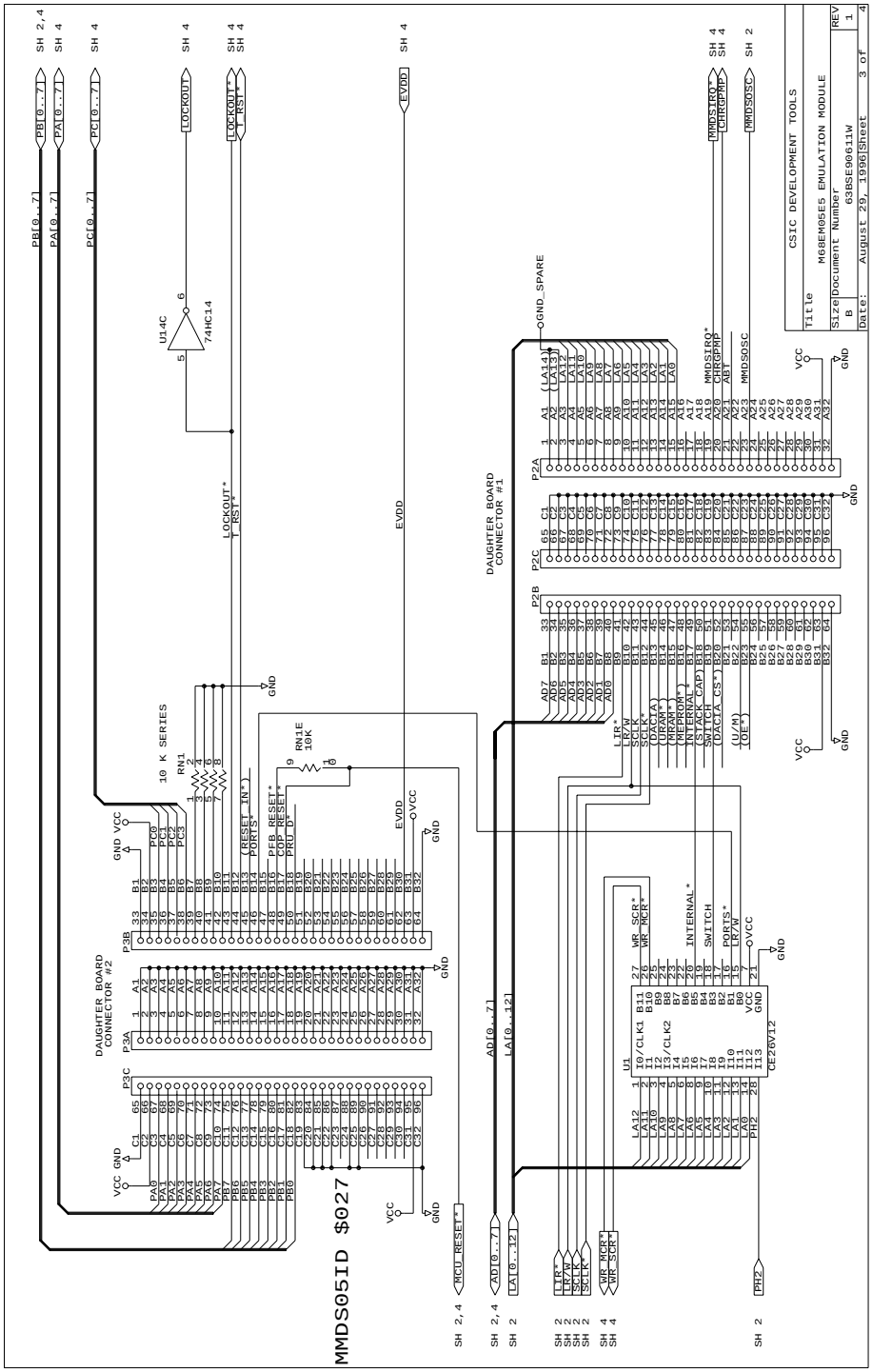
Schematics

M68EM05E5 Schematics (Sheet 2 of 4)



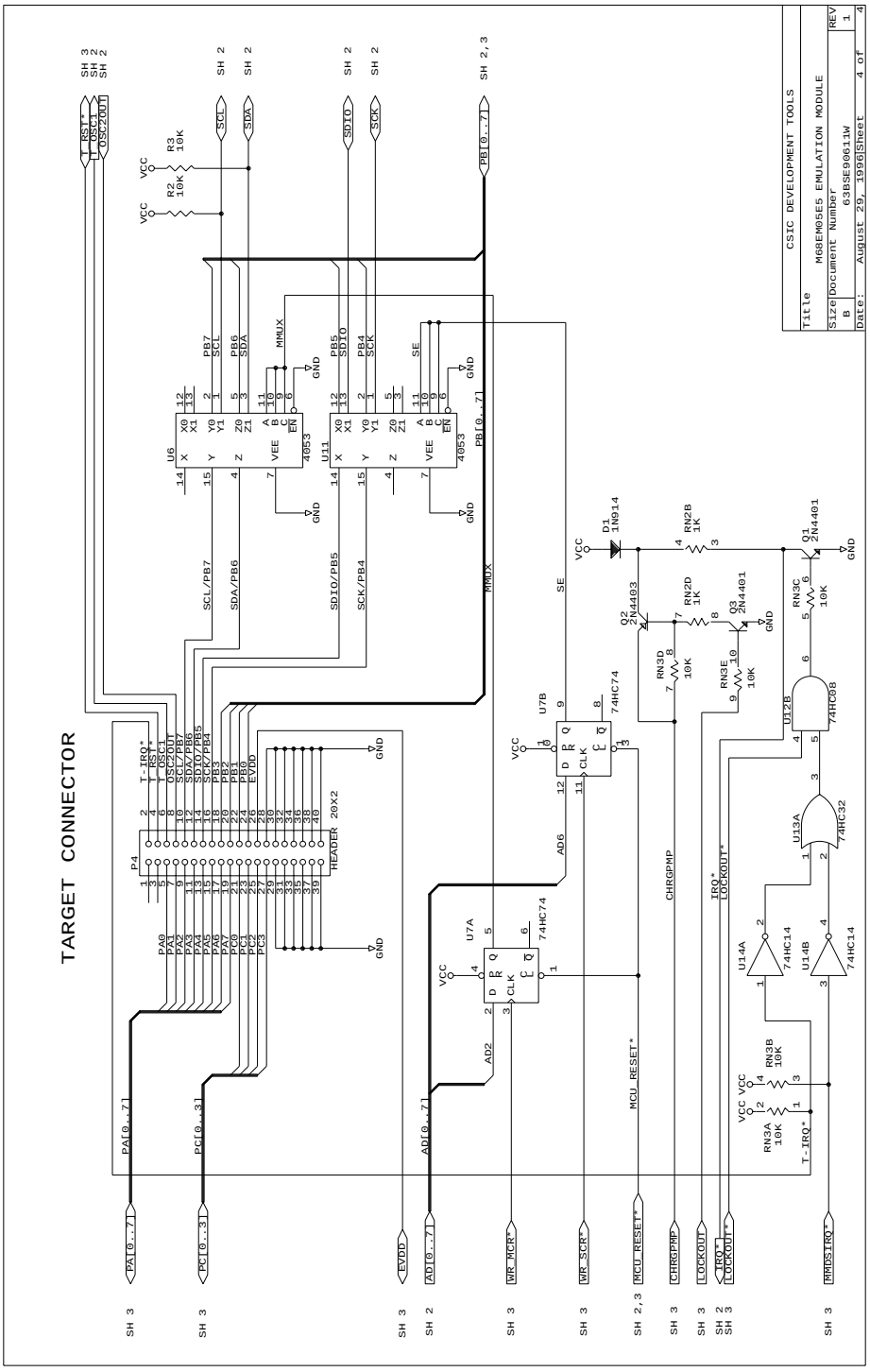
Schematics

M68EM05E5 Schematics (Sheet 3 of 4)



Schematics

M68EM05E5 Schematics (Sheet 4 of 4)



Schematics