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RAM Data Retention Considerations for Motorola Microcontrollers

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Introduction

This engineering bulletin discusses some of the design considerations and techniques for implementing a non-battery RAM (random-access memory) data retention scheme for Motorola microcontrollers (MCU) that do not have separate RAM standby power pins, such as some of the devices in the 68HC(7)05 and 68HC11 MCU Families.

Background

Some MCU-based system designs require RAM data retention for transient power outages, possibly during the changing of batteries, or for brownout conditions.

The simple solution to the challenge is to detect the occurrence of the power failure, write RAM data into an external EEPROM (electrically erasable programmable read-only memory), and read the saved RAM data from the EEPROM when power is restored.

However, cost-sensitive systems may not be able to afford the luxury of an EEPROM. Applying creative design techniques to the system may be an inexpensive solution to the issue.

From a Hardware Point of View

The hardware design for RAM data retention is likely the most difficult part of the challenge. When using Motorola MCUs, some basic issues need to be considered when saving RAM data during a power outage.

For example, the user must make provisions in hardware for these functions:

- Power failure detection circuitry
- Power restoration $\overline{\text{RESET}}$ circuitry
- An energy storage device, for instance, a capacitor
- Power supply isolation (MCU power isolated from the rest of analog and digital circuitry)

Figure 1 shows a possible hardware configuration to accomplish RAM retention during a power outage. The circuit provides two basic functions:

1. First, it must momentarily assert the $\overline{\text{RESET}}$ input to the MCU when system power is restored or powered-up the first time.
2. Second, the circuit must interrupt the MCU when the power fails so immediate action can be taken.

Figure 2 shows a timing sequence for the assertion of $\overline{\text{RESET}}$ at the initiation or resumption of power and the assertion of $\overline{\text{IRQ}}$ upon the detection of a power failure.

NOTE: *The power restoration $\overline{\text{RESET}}$ circuit must be designed such that it resets the MCU as power is restored, but does not assert the $\overline{\text{RESET}}$ input to the MCU during the power outage. Asserting the MCU's $\overline{\text{RESET}}$ during the duration of a power outage allows its oscillator to run, consuming valuable power from the RAM retention capacitor.*

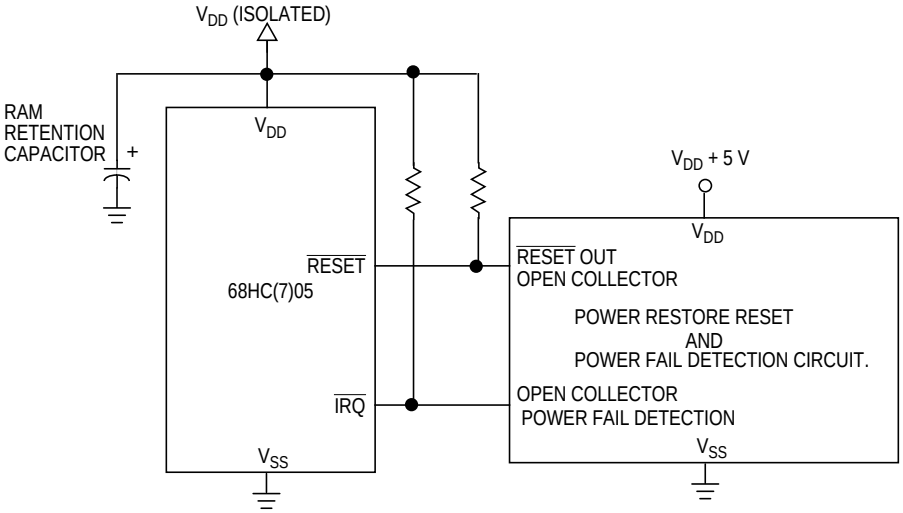

Figure 1. Power Fail and Power Restore Detection Block Diagram

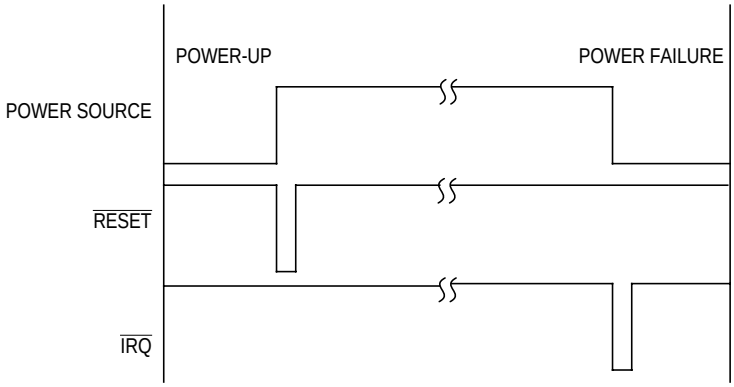

Figure 2. Power Restore Detection and Power Fail Timing Diagram

The power failure circuit will inform the MCU via its $\overline{IRQ}$ input that a power failure is imminent and some action will be required. Most likely, the action will be to calculate a RAM checksum, set up some of the input/output (I/O) ports, and finally place the MCU in stop mode.

Stop mode will place the MCU in its lowest possible power mode. It will remain in that state until one of two events occurs.

An external interrupt is asserted or the $\overline{RESET}$ input is asserted. Never leave inputs to the MCU floating because they can cause excessive current consumption. If any of the MCU's bidirectional I/O ports are not

terminated, make sure the data direction register bits for the I/O port are set as outputs. If the port is an input-only port, make sure its input is terminated. Set the output ports to ensure that they do not drive or sink current during the power outage.

An energy storage device will be needed to power the MCU during the power outage. In this case, it will be a capacitor.

It is important to segregate the microcontroller's power source from that of other logic and analog circuitry in the system. Power supply isolation is necessary to ensure that the RAM retention capacitor will power only the microcontroller and other minimal circuitry.

The circuitry powered by the RAM retention capacitor must be designed with minimum leakage in mind.

Some of the not-so-obvious sources of printed circuit board leakage are:

- High leakage decoupling capacitors
- Forward-biased junctions through non-powered devices connected to the MCU's I/O
- PC boards that have flux remaining from the soldering process
- PC boards that reside in high humidity environments and are not conformally coated.

Sizing the Capacitor

To size the capacitor, some basic information about the system must be known, specifically:

1. What is the minimum time RAM data must be retained during the power failure?
2. What is the minimum RAM retention voltage specification of the MCU of choice?
3. What is the nominal MCU's power supply voltage?

4. What is the STOP current of the MCU plus the current requirements of any other circuitry powered by the RAM retention capacitor?

The formula for sizing a capacitor to retain RAM data is

$$C_{Retention} = (I_{Micro} / V_{Delta}) * t_{Retention}$$

Where:

$C_{Retention}$ is the RAM retention capacitor in microfarads.

I_{Micro} is the average STOP current, in microamperes, of the MCU plus any additional circuits powered from the RAM retention capacitor.

V_{Delta} is the nominal power supply voltage minus the minimum RAM retention specification of the MCU.

$t_{Retention}$ is the RAM retention in seconds.

As an example, consider a system with these specifications:

1. RAM data must be retained for five minutes. ($t_{Retention}$ = 300 seconds)
2. The minimum RAM retention voltage specification from the MCU's documentation is 2 volts.
3. The nominal system power supply voltage is 5 volts. (V_{Delta} = 3 volts = (5 volts – 2 volts))
4. The average STOP current of the MCU is 1 μA plus 2 μA for additional circuitry, etc. (I_{Micro} = 3 μA)

$$C_{Retention} = (3 \times 10^{-6} / 3) \times 300 = 300\ \mu F$$

The I_{Micro} is the average current draw over the RAM retention time. This is because the current of most semiconductor devices is linear with respect to its applied voltage.

When choosing the RAM retention capacitor, an aluminum electrolytic with low dielectric leakage will be the best choice. Choosing an aluminum electrolytic capacitor for a 5-volt system of 16 Vdc working voltage or greater generally will provide the lowest leakage.

From a Software Point of View

A number of issues need to be addressed when power is lost and then once it has been restored.

The design of the system power supply will dictate how the power failure detection is handled. In any event, circuitry that will detect an impending power failure is necessary. It may be a comparator circuit, monitoring some dc voltage in the system, or possibly a circuit that detects lost ac cycles.

The job of the software, upon the occurrence of the power failure, is:

- Calculate and save a checksum of the RAM area being saved
- Set I/O ports to ensure that ports do not drive or sink current or are left floating during the power outage
- Then execute a STOP instruction

Upon restoration of power, the software will:

- Check the current RAM checksum against the previously calculated checksum
- If the checksums match, normal system activity can be resumed with the saved data.
- If the checksums do not agree, the software must assume power had been lost for an excessive length of time, resulting in corrupted RAM data, and restart the system with default values.

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