

TRANSPORTATION SYSTEMS GROUP
MASK SET ERRATA AND INFORMATION SHEET
Part: HC812AV4.00H50F.A Mask Set:

HC812AV4.00H50F.A Modules
Current Module Revision
ATD8B8C.2.3
BDM256.2.2
CDL_AV4.1.0
CPU.3.2
EBI_AV4.1.0
EE4K.2.1
INT.1.2
KWU24C.1.2
LIM_AV4.1.0
MMI_AV4.1.0
MSI2C1P.2.0
MXS6X7S.1.2
OSC.2.1
PDA.2.1
PDATD.4.0
PDB.2.1
PDBK.2.1
PDC.2.0
PDD.2.0
PDE.3.1
PDF.2.0
PDG.2.0
PDH.2.0
PDJ.2.0
PDRST.2.1
PDS.3.0
PDT.2.1
PDV.3.1
PDVSB.1.0
PDXFC.3.0
RAM1K.1.3
ROC.2.0
TIM16B8C.1.3
WCR.1.1

HC12_AR_189

Customer Erratum

ATD8B8C.2.3

BRIEF DESCRIPTION:

(ATD) Access to result registers conflict with register bus pre-charge timing

DESCRIPTION:

Unknown

WORKAROUND:

Unknown

HC12_AR_107

Customer Erratum

ATD8B8C.2.3

BRIEF DESCRIPTION:

(ATD) Accuracy is off by as much as 4 counts on an 8-bit conversion

DESCRIPTION:

None

WORKAROUND:

Only rely on a 6-bit result

HC12_AR_374

Customer Erratum

ATD8B8C.2.3

BRIEF DESCRIPTION:

(ATD) Status bits not properly reset when starting a new conversion sequence

DESCRIPTION:

ATD status bits and conversion counter are not reset properly if a new conversion sequence is started while an active A/D conversion sequence is in the process of completion.

WORKAROUND:

When starting a new sequence, perform two writes to control registers 4/5 in quick succession. If the first write occurs when the status bit/conversion counter is not reset, the second write will correct ATD operation.

HC12_AR_164

Customer Erratum

ATD8B8C.2.3

BRIEF DESCRIPTION:

(ATD) Race in result register

DESCRIPTION:

ATD should be considered accurate to about 6 bits.

WORKAROUND:

None

HC12_AR_194

Customer Erratum

ATD8B8C.2.3

BRIEF DESCRIPTION:

(ATD) Low voltage write zero read one failure

DESCRIPTION:

Some registers fail to read \$0000's after a write of \$0000. Failures seen consistently at cold temperature. At room and hot temperature, failures are seen below 5.1 volts.

WORKAROUND:

Will not halt code development as long as voltage and temperature are maintained above failure points.

HC12_AR_197

Customer Erratum

ATD8B8C.2.3

BRIEF DESCRIPTION:

(ATD) Conversion failure at low temperature and high current consumption.

DESCRIPTION:

ATD won't convert at low temperatures.

WORKAROUND:

None.

HC12_AR_311

Customer Information

ATD8B8C.2.3

BRIEF DESCRIPTION:

(ATD) conversion of the $(V_{rh}-V_{rl})/2$ internal ref voltage returns \$7F not \$80

DESCRIPTION:

The (VRH-VRL)/2 internal reference conversion result may be \$7F, \$80 or \$81.

WORKAROUND:

If the (VRH-VRL)/2 internal reference is used (perhaps for system diagnostics), expected pass result may be \$7F, \$80 or \$81.

HC12_AR_184**Customer Information****BDM256.2.2****BRIEF DESCRIPTION:**

(BDM) Turning off BDMACT by serial command can cause crash.

DESCRIPTION:

There is a small chance that the BDMACT bit in the BDM STATUS register could be unintentionally changed from 1 to 0 by a WRITE_BD_BYTE serial command. This would cause a system runaway because it would disable the BDM firmware ROM while the CPU was executing BDM firmware.

WORKAROUND:

This workaround avoids most of the cases that could cause an unintended change of BDMACT from 1 to 0. To change the ENFIRM bit in STATUS, always perform a READ_BD_BYTE serial command, modify this value with OR #\$80 to set ENFIRM or AND #\$7F to clear ENFIRM, then use WRITE_BD_BYTE to write the modified result back to STATUS. This avoids most cases that could result in an unintended clearing of BDMACT. There is one case that could still occur (though it would be very rare). A BGND instruction (opcode \$00) could be encountered between the READ_BD_BYTE and the WRITE_BD_BYTE. Even if ENBDM is zero, the BDM ROM is enabled and the CPU executes a short sequence in the BDM firmware to check the state of ENFIRM - if it was zero, the firmware immediately executes an exit sequence to return to user code (user code sees this as a long NOP).

HC12_AR_287**Customer Erratum****CPU.3.2****BRIEF DESCRIPTION:**

(CPU) The ETBL instruction is dependent on the initial C-bit value

DESCRIPTION:

The ETBL instruction will provide an incorrect result under EITHER of the following 2 conditions:1) Y2 less than Y1 and C-bit = 0 before ETBL instruction executed2) Y2 greater than Y1 and C-bit = 1 before ETBL instruction executed except for the cases where $(B * (Y2 - Y1)) = 0$ (i.e. B=0 or Y2=Y1)

WORKAROUND:

If a borrow is needed from the equation, then set C-bit=1 before executing the ETBL instruction; if a borrow is not needed than clear C- bit=0 before executing the ETBL instruction. Example: LDxy (idx); initialize index register to point to the start point LDD (Y2); get value of Y2 into ACCDCPD (Y1); D-M, Y2-Y1, This updates C-bit LDAB (B); accumulator B initialized with ratio ETBL (idx); Perform instruction

HC12_AR_191**Customer Erratum****CPU.3.2****BRIEF DESCRIPTION:**

(CPU) SP value wrong after CLI-SWI instruction sequence

DESCRIPTION:

If an SWI instruction is executed immediately after a CLI instruction and an interrupt is pending, the SWI executes incorrectly. No registers are stacked, but the SP is decremented by 2. The correct SWI vector is taken. Avoid the sequence CLI-SWI. This sequence would normally only occur when using a ROM monitor for debug (this sequence would not normally occur in user code).

WORKAROUND:

Do not place the SWI instruction immediately after any instruction that clears the I bit. Put a NOP in between the SWI and the previous instruction. This is a very rare instruction sequence that would probably only occur during ROM-monitor assisted debugging, such as on an EVB.

HC12_AR_288**Customer Erratum****CPU.3.2****BRIEF DESCRIPTION:**

(CPU) REV and REVW may give incorrect results if interrupted

DESCRIPTION:

If the REV or REVW instructions are interrupted while processing a rules list, the results from the instructions may be incorrect. The Condition Code Register and Index Register Y (weight pointer for REVW) may be incorrect when the stacking occurs for the interrupt. The REV and REVW instructions produce the wrong result after returning from the interrupt because the V-bit in the CC register and IY registers (REWW) may not hold the same state as prior to the interrupt.

WORKAROUND:

Disable the interrupts prior to using the REV or REVW instruction (which could increase the interrupt latency). If a non-maskable interrupt has been enabled, there is no workaround.

HC12_AR_217

Customer Information

EBI_AV4.1.0

BRIEF DESCRIPTION:

(EBI_AV4) Pipe signals to PE[6:5] not correct during a BDMFRZ.

DESCRIPTION:

The multiplexed IPIPE(1:0) signals, which are available on PORTE(6:5) pins, do not convey the correct information for reconstruction of the internal instruction queue during a BDMFRZ. BDMFRZ occurs when a BDM access is requested and either no free cycles are found within 128 cycles or the requested access cannot be completed in one cycle (i.e.: mis-aligned word access).

WORKAROUND:

This is very minor. When using a logic analyzer, be aware that a BDMFRZ operation will not be properly identified by the pipe status bits even though the operation will function properly.

HC12_AR_253

Customer Information

EBI_AV4.1.0

BRIEF DESCRIPTION:

(EBI_AV4) During the delay coming out of STOP, E clock is output

DESCRIPTION:

When the part is in the delay phase of coming out of STOP, the E clock will be running external. Since the oscillator is just starting up, the E clock is likely to be “dirty” during the beginning of this time.

WORKAROUND:

None needed.

HC12_AR_193

Customer Information

EE4K.2.1

BRIEF DESCRIPTION:

(EE) Read from array after write

DESCRIPTION:

Read from array after latches are written could re-open the address latches.

WORKAROUND:

Customer software should not read the array once eelat has been set and the write to the array has been performed. This is not part of the normal programming sequence anyway.

HC12_AR_235

Customer Erratum

INT.1.2

BRIEF DESCRIPTION:

(INT) When IRQEN=0, IRQ pin is still able to wake up from stop.

DESCRIPTION:

If IRQEN bit is cleared, the IRQ pin is still able to wake up the part from stop mode. Once the part is out of STOP, it continues with the instruction following the STOP (IRQEN = 0 prevents the IRQ interrupt from being taken).

WORKAROUND:

Make certain IRQEN is 1 before going into STOP or make certain the level on the IRQ pin is always 1 during STOP. Third choice: set the I mask before going into STOP, but this only leaves XIRQ and reset to get out of STOP.

HC12_AR_234

Customer Erratum

INT.1.2

BRIEF DESCRIPTION:

(INT) FFC6 to FFCC interrupts can not wake up from stop

DESCRIPTION:

Phase counter and real time clock interrupts can not wake up the part from stop mode.

WORKAROUND:

No workaround.

HC12_AR_289

Customer Information

MSI2C1P.2.0

BRIEF DESCRIPTION:

(MSI2C1P) SPI general purpose I/O specification inadequate

DESCRIPTION:

Not a functional problem, but operation of general purpose I/O may be confusing when used in conjunction with SPI.

WORKAROUND:

Avoid getting a mode fault: Do not set SPE and MSTR bits with active low on SS pin when DDRS[7] is cleared. Initialize DDRS[7] to be an output before enabling SPI.

HC12_AR_222 Customer Erratum PDE.3.1

BRIEF DESCRIPTION:

(PADS_AV4) ESD results fail 2KV MC level status

DESCRIPTION:

Port E bit 1 (IRQ*) and XFC (PLL filter pin) do not meet ESD protection specs.

WORKAROUND:

Use extra care when handling parts.

HC12_AR_222 Customer Erratum PDXFC.3.0

BRIEF DESCRIPTION:

(PADS_AV4) ESD results fail 2KV MC level status

DESCRIPTION:

Port E bit 1 (IRQ*) and XFC (PLL filter pin) do not meet ESD protection specs.

WORKAROUND:

Use extra care when handling parts.

HC12_AR_273 Customer Erratum RAM1K.1.3

BRIEF DESCRIPTION:

(RAM) Peak Ivstby switch current is higher than expected.

DESCRIPTION:

On parts with a voltage standby function, the peak Ivstby switch current is approximately 280uA.

WORKAROUND:

None

HC12_AR_213 Customer Erratum RAM1K.1.3

BRIEF DESCRIPTION:

(RAM) Vstby implementation has susceptibility in “crank” mode

DESCRIPTION:

On parts with a voltage standby function, when Vdd drops below Vstby, there is a point at which Vstby draws a higher than normal current. The Vdd voltage at which this occurs depends on the Vstby voltage and whether Vdd is rising or falling.

WORKAROUND:

It will be necessary to design the Vstby circuit to tolerate higher current. This is not a problem for parts that don't have VSTBY implemented.

HC12_AR_200**Customer Erratum****RAM1K.1.3****BRIEF DESCRIPTION:**

(RAM) Vstby function draws too much current

DESCRIPTION:

On parts with a voltage standby function to maintain the RAM contents during power down, the Vstby pin draws more current than desired.

WORKAROUND:

Vstby draws less current at lower voltage, therefore; use Vstby at 2 Volts to draw less current while still maintaining the RAM contents. This is not a problem for parts that don't have VSTBY implemented.

HC12_AR_201**Customer Erratum****RAM1K.1.3****BRIEF DESCRIPTION:**

(RAM) Vstby pin not designed to also be general purpose input.

DESCRIPTION:

On parts with a V standby function, there is the possibility that due to the way this is implemented on this silicon, the RAM could quit working when Vstby = 0 volts. Experiments with silicon have not shown this to be a problem.

WORKAROUND:

It is best to only use this pin for Vstby until it is fixed. This is not a problem for parts that don't have VSTBY implemented.

HC12_AR_225

Customer Information

RAM1K.1.3

BRIEF DESCRIPTION:

(RAM) High Stop Idd

DESCRIPTION:

Process variations can cause higher than expected stop Idd.

WORKAROUND:

None. Parts are being screened.

HC12_AR_161

Customer Erratum

ROC.2.0

BRIEF DESCRIPTION:

(ROC) Reset "Brown-out" anomaly

DESCRIPTION:

If the power is dropped to approximately 1 Volt the internal clocks collapse. The part will not respond to the reset pin until VDD is brought back to 5 Volts.

WORKAROUND:

After VDD is stabilized at nominal VDD's (2.7-5 Volts), pulling the reset pin low will initiate the reset. Alternatively, if the watchdog is enabled the part will recover when it times out.

HC12_AR_196

Customer Erratum

ROC.2.0

BRIEF DESCRIPTION:

(ROC) missed vector out of STOP with DLY = 0 and free running clock

DESCRIPTION:

Coming out of STOP with DLY = 0 and a free-running external clock source (i.e. oscillator pack) could cause the interrupt vector to be missed.

WORKAROUND:

Always use DLY = 1 when using STOP.

HC12_AR_305

Customer Erratum

ROC.2.0

BRIEF DESCRIPTION:

(ROC) Intermittent failure to exit STOP mode.

DESCRIPTION:

When the clock source (i.e. crystal) has been stopped for greater than 300us there is high probability that an unstable clock will disrupt the internal tclocks. With a free running clock source (i.e. oscillator pack), asserting the wake-up signal (i.e. XIRQ, IRQ) just prior to the falling edge of external clock source can cause the part to not exit stop.

WORKAROUND:

Crystal: No workaround. Oscillator Pack: Synchronize wake-up signal to the rising edge of external clock input.

HC12_AR_400

Customer Information

ROC.2.0

BRIEF DESCRIPTION:

(ROC) STOP does not take timeout when reset is the release

DESCRIPTION:

When coming out of STOP by using reset, the crystal start-up delay time-out does not occur. This means the MCU may be attempting to run before the crystal has become stable.

WORKAROUND:

When coming out of STOP with reset hold the reset signal until the crystal has reached stable oscillation.

HC12_AR_285

Customer Erratum

TIM16B8C.1.3

BRIEF DESCRIPTION:

(TIM16B8C) Output compare flags cannot be cleared while count matches

DESCRIPTION:

The output compare flags cannot be cleared until the timer increments past the matching count. This will cause a problem when using a timer prescaler value larger than divide-by-8. The result is the output compare interrupt is asserted continuously until the timer increments past the matching count. The same result will occur when an external clock source is used to drive the timer through the pulse accumulator pin.

WORKAROUND:

It takes at least 11 cycles to get into an interrupt service routine. If the effective prescale value is greater than divide-by-8, then the user must account for the number of cycles it takes to increment the timer counter past the match point before clearing the associated output compare flag and exiting the interrupt service routine.

HC12_AR_322**Customer Erratum****WCR.1.1****BRIEF DESCRIPTION:**

(WCR_1) RTI interrupt is timed on the wrong clock edge

DESCRIPTION:

When an I-type interrupt occurs at the same time as an RTI interrupt, the program address at \$FFC0 will be fetched.

WORKAROUND:

Point the \$FFC0 vector to a return from interrupt (RTI) instruction. This will get the program returned to start processing the proper interrupt as quickly as possible.

HC12_AR_187**Customer Information****WCR.1.1****BRIEF DESCRIPTION:**

(WCR) Request to change COP reset rate on the 68HC912B32.

DESCRIPTION:

The COP reset rate was changed from the slowest to the fastest rate on the 68HC912B32. The 68HC812A4 was not affected.

WORKAROUND:

Not applicable to the 68HC812A4.

Last updated: April 2, 1998