68HC12D60MSE1 Rev 1
March 1, 2001

Mask Set Errata 1

MC68HC12D60 Microcontroller Unit

INTRODUCTION

This errata provides mask-set specific information applicable to the following MC68HC12D60 MCU mask set devices:

- 0K13J

MCU DEVICE MASK SET IDENTIFICATION

The mask set is identified by a four-character code consisting of a letter, two numerical digits, and a letter, for example F74B. Slight variations to the mask set identification code may result in an optional numerical digit preceding the standard four-character code, for example 0F74B.

MCU DEVICE DATE CODES

Device markings indicate the week of manufacture and the mask set used. The data is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. The date code “9115” would indicate the 15th week of the year 1991.

MCU DEVICE PART NUMBER PREFIXES

Some MCU samples and devices are marked with an SC, PC, ZC or XC prefix. An SC, PC or ZC prefix denotes special/custom device. An XC prefix denotes device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the MC prefix.

When contacting a Motorola representative for assistance, please have the MCU device mask set and date code information available.

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ATD: CONVERSION OF THE (V_{RH}–V_{RL})/2 INTERNAL REF VOLTAGE RETURNS $7F, $80 OR $81 AR311

The (V_{RH}–V_{RL})/2 internal reference conversion result may be $7F, $80 or $81.

Work-around If the (V_{RH}–V_{RL})/2 internal reference is used (perhaps for system diagnostics), expected pass result may be $7F, $80 or $81.

HC12D60 CANNOT BE PACED USING AN EXTERNAL EXTAL SQUARE WAVE OF FREQUENCY LESS THAN 500KHZ AR574

For low power consumption, the slow mode divider can be used to clock the MCU at very low frequencies.

Work-around None

CGM: CRYSTAL OPERATION AR593

The variation of operational parameters within a given crystal part number may include a distribution of parts that present impedance conditions at start-up that will not function with the current design of the CGM. While typical parts may function correctly, problems may be seen in actual production runs.

Work-around Quartz crystal operation should be restricted to maximum 8MHz.

1. Use 8MHz (or slower) oscillator and generate higher bus frequencies using the PLL module.
2. Use alternative ceramic resonator.
3. Where mimimal clock jitter is critical, use external 'brick' quartz oscillator module.

INT: WAIT CANNOT BE EXITED IF XIRQ/IRQ LEVEL DEASSERTION OCCURS WITHIN PARTICULAR WINDOW OF TIME AR600

The device can get trapped in WAIT mode if, on exiting the WAIT instruction, the deassertion timing of the XIRQ or level-sensitive IRQ occurs within a particular timeframe. Only reset will allow recovery. Noise/bounce on the pins could also cause this problem.

Work-around

1. Use edge-triggered IRQ (IRQE=1) instead of XIRQ or level-triggered IRQ.
2. Use RTI , timer interrupts, KWU or other interrupts (except level-sensitive IRQ or XIRQ) to exit WAIT. If using RTI, it must be enabled in WAIT (RSWAI=0) and the COP must be disabled (CME=0).
3. Assert XIRQ or level-sensitive IRQ until the interrupt subroutine is entered.
4. Add de-bouncing logic to prevent inadvertent highs when exiting WAIT.

INT: DISABLING INTERRUPT WITH I MASK BIT CLEAR CAN CAUSE SWI AR527

If the source of an interrupt is taken away by disabling the interrupt without setting the I mask bit in the CCR, an SWI interrupt may be fetched instead of the vector for the interrupt source that was disabled.

Work-around

Before disabling an interrupt using a local interrupt control bit, set the I mask bit in the CCR.

PLL: LIMP HOME MODE AR627

The device can prematurely indicate that the oscillator has stabilized releasing the part from Limp Home clock mode to the oscillator clock mode with an unstable oscillator. This can cause unpredictable behavior of the MCU. This situation can arise with short external power-on reset periods and / or crystal oscillator circuits that exhibit slow startup characteristics. If the PLL is not being used (Vddpll connected to Vss) Limp Home mode is disabled and this issue does not apply.

All customers should review any applications based on the referenced devices. If the crystal clock is stabilized before the external RESET line is released and the customer is not using stop mode (pseudo-stop is not affected) then there is no problem. If the clock is not stable when external RESET is released then they should contact Motorola for consultation.

Common practice for the start up mode of operation of HC12 microcontrollers is for the external RESET line to be held active until such time as the crystal has stabilized at its operating frequency. On release of the external RESET line and when the WCR (counter register) reaches a count of 4096 cycles, normal operating mode is entered with the CPU clocked from the crystal frequency (see fig. 1).

The HC12 mode of operation known as Limp-Home Mode (LHM) is enabled when the VDDPLL pin is at VDD and is entered if for any reason the external crystal ceases to oscillate. During this mode the CPU will be clocked from the free-running VCO clock of the PLL (at a nominal frequency of 1MHz). If LHM is enabled during the start-up phase (i.e. VDDPLL=5V, NOLHM bit=0) and the external RESET line is not held active until after the crystal frequency is stable then the device starts up in LHM since no crystal oscillations will be detected. This situation can arise with short reset periods and/or crystals that exhibit slow start-up characteristics.

For the first 4096 cycles i.e. during the internal reset period, Limp Home mode will be de-asserted if oscillator activity is detected by the clock monitor circuit -due to the asserted Reset signal there can be no CPU activity during the Reset phase. Following release of the external or internal POR RESET in LHM (which ever is later) the crystal oscillator is sampled by the clock monitor circuit after another 4096 VCO clock cycles and at intervals of 8192 clock cycles thereafter until the crystal is deemed to be operating. If the crystal oscillator is showing activity at the time it is checked then it will be deemed to be good, even though it may not have fully stabilized, and LHM will be de-asserted. This can cause the device to switch from LH mode to normal mode with the CPU clocked from an unstable signal from the crystal oscillator (see fig. 2) resulting in unpredictable function of the CPU.

The COP Reset doesn’t exhibit this behavior as, although the same reset sequence is followed, the oscillator isn’t stopped.

When exiting Stop mode (DLY=1) a similar 4096 cycle delay is executed and therefore this behavior could also show up at this time. In applications where this is likely to be an issue, using pseudo-stop is recommended as an alternative. Current draw will increase <100 ?A at 4MHz in pseudo stop versus stop mode.

Following a loss of external clock in normal operation, Limp Home mode will be entered successfully but if the oscillator is reconnected for some reason a similar situation may arise.

The Reset condition can be overcome by allowing the crystal oscillator circuit to stabilize before releasing the external RESET line (see fig. 3). Operation is similar to that shown in fig 2.

To determine if crystal is ’stable’ at the release of reset can be difficult and the time can vary some from board to board. If the customer has special high impedance probes, it is possible to monitor the amplitude of the voltage from XTAL to ground (<2 pF scope probes are recommended). Please note that any loading on the circuit can affect its operation. (Any resistance to ground or Vdd on the EXTAL pin can greatly attenuate the amplifier gain and cause erroneous operation.)

A second way to measure the oscillator startup time is to monitor the XFC pin. This method does not require a high impedance scope probe. The PLL will not lock until the oscillator clock feeding it is present and stable. Remove the external reset circuit and during power up watch the XFC pin. The voltage should start high (Vdd). After the part releases internal reset it will drop to some stable voltage between Vdd and Vss. If external reset (measured independent from this test) is held till this 'stable voltage' time the oscillator will be stable. Please note the filter components mounted on the XFC pin will affect this ramp (for evaluation purposes, alternative components can be selected to provide a fast lock time). More than one board should be measured because of pcb and crystal variability. It is also recommended that the test be run over the operating temperature of the device.

Lastly, an alternative and simpler approach is to just hold reset low for a substantial time (> 100 milliseconds) after Vdd has reached the operating voltage range.

In some applications it may be possible avoid this issue by delaying the connection of Vddpll to Vdd until the device has exited reset. This will sacrifice the limp home mode safety function upon startup, i.e. the part will no longer be able to start without a functioning crystal. A similar technique (disable PLL under software control) can be used to overcome the limitations of Stop mode.

Limp-Home mode start-up issue

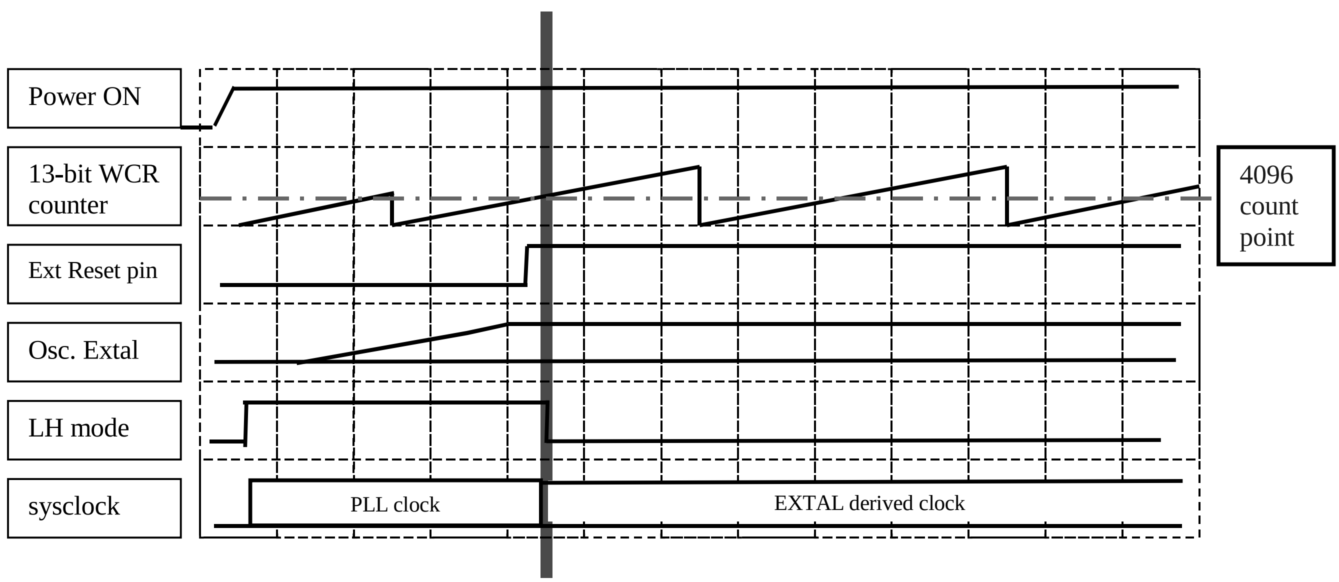

Figure 1. Representation of Normal start-up condition

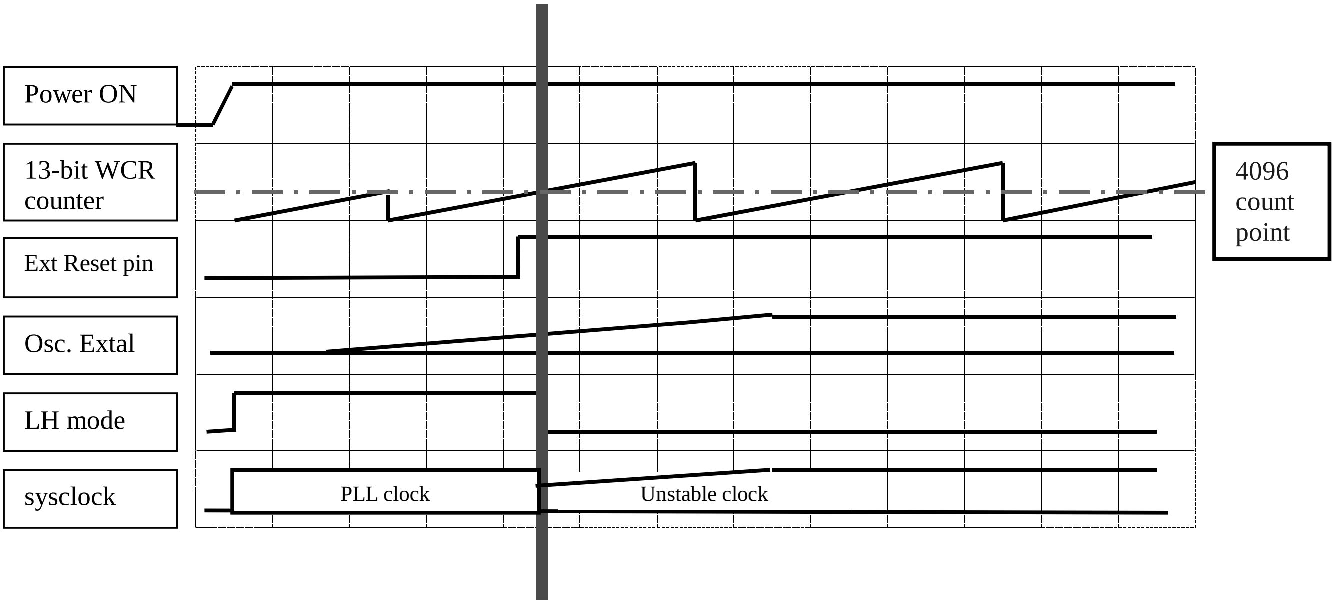

Figure 2. Representation of unreliable start-up mode with slow crystal

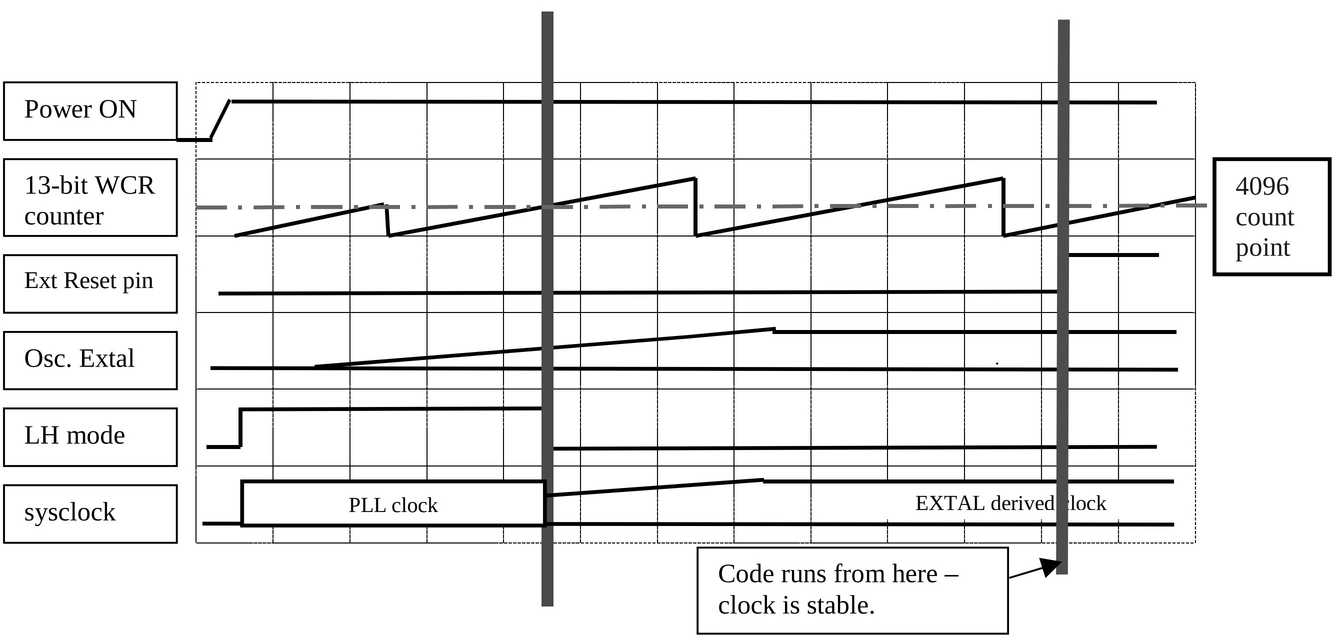

Figure 3. Representation of preferred means of overcoming issue with Figure 2

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Additional mask set errata can be found on the World Wide Web at http://www.mcu.motsps.com/documentation/index.html