Mask Set Errata 1
68HC908JB8 8-Bit Microcontroller Unit

INTRODUCTION

This mask set errata provides information pertaining to the glitch on timer buffered PWM output applicable to this 68HC908JB8 MCU mask set device:

- 3K45H

MCU DEVICE MASK SET IDENTIFICATION

The mask set is identified by a 5-character code consisting of a version number, a letter, two numerical digits, and a letter, for example 0XJ66D. Slight variations to the mask set identification code may result in an altered version number, for example 1XJ66D.

MCU DEVICE DATE CODES

Device markings indicate the week of manufacture and the mask set used. The date is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. For instance, the date code "9115" indicates the 15th week of the year 1991.

MCU DEVICE PART NUMBER PREFIXES

Some MCU samples and devices are marked with an SC or XC prefix. An SC prefix denotes special/custom device. An XC prefix denotes that the device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the MC prefix.

When contacting a Motorola representative for assistance, please have the MCU device mask set and date code information available.

MSE Published Date: 3/16/01

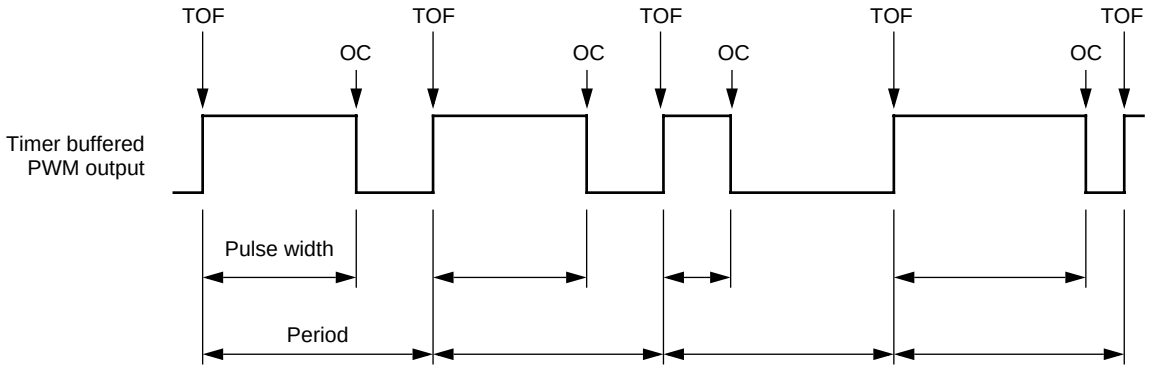
GLITCH ON TIMER BUFFERED PWM OUTPUT

In timer buffered PWM operation, when a timer overflow (TOF) event or an output compare (OC) event coincides with a write to either pair of the timer channel registers (TCHxH/L), the duty cycle at the PWM output glitches to 0% or 100% momentarily, then returns to proper operation.

To avoid the glitches when changing the PWM duty cycle, do not write to either pair of the timer channel registers at the TOF or OC.

For example, in the TOF interrupt service routine: If the OC occurs near the last TOF, write to the timer channel registers after the OC; if the OC occurs near the next TOF, write to the timer channel registers before the OC. A write to the channel register high byte (TCHxH) should immediately followed by a write to the low byte (TCHxL) to avoid TOF or OC occurring between the writes. Instruction cycle times must be included when making timing calculations.

The figure below shows a typical timer buffered PWM output waveform, indicating the TOF and OC events.



NOTES:

Do not write to either pair of timer channel registers at:
TOF (timer overflow), or
OC (timer output compare) edges.

In buffered PWM, the pulse width is defined by the last written pair of timer channel registers.
Each pair of timer channel registers consist of a high byte register (TCHxH) and a low byte register (TCHxL).

Additional mask set erratas can be found on the World Wide Web at http://mcu.motsps.com/documentation