Mask Set Errata 5
68HC08AS20 8-Bit Microcontroller Unit

INTRODUCTION

This mask set errata provides information pertaining to the TIM, ESD, Stop I_{DD}, and SPI modules applicable to these 68HC08AS20 MCU mask set devices:

- 0H94K
- 0J26H

MCU DEVICE MASK SET IDENTIFICATION

The mask set is identified by a 5-character code consisting of a version number, a letter, two numerical digits, and a letter, for example 0H94K. Slight variations to the mask set identification code may result in an altered version number, for example 1H94K.

MCU DEVICE DATE CODES

Device markings indicate the week of manufacture and the mask set used. The data is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. For instance, the date code "9115" indicates the 15th week of the year 1991.

MCU DEVICE PART NUMBER PREFIXES

Some MCU samples and devices are marked with an SC or XC prefix. An SC prefix denotes special/custom device. An XC prefix denotes that the device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the MC prefix.

When contacting a Motorola representative for assistance, please have the MCU device mask set and date code information available.

Specifications and information herein are subject to change without notice.

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TIMER MODULE ERRATA

When the TOV bit is set, writing to the TCHXH register at the point of an overflow inhibits the associated TCHX pin from toggling on an overflow until the TCHXL register is written. However, the TOF bit still gets set, thereby generating an overflow interrupt. If the pin is supposed to toggle on overflow, but the TCHXL is not yet written, that pin-toggling event is completely missed. The only condition that should inhibit a toggle on overflow and setting of the TOF bit is writing to the TMODH register.

In buffer PWM mode, if the inactive channel registers being written at this overflow point are TCH0H:L, TCH2H:L, for TCH4H:L, respectively, the problem occurs.

Software workaround:

1. Write to the TCHXH register and then to the TCHXL register four cycles prior to overflow point.

2. Always update the TCHXH:L register within the overflow interrupt routine.

ESD FAILURE AT 2000V HUMAN BODY MODEL STRESS

The ESD failure indicates a sensitivity of the $\overline{\text{IRQ}}$ pin at 2000 V, yet it passes at 1500 V.

STOP I_{DD}

The stop I_{DD} measurements exceed the maximum specifications in *68HC08AS20 Advance Information*, Motorola order number MC68HC08AS20/D.

The maximum stop I_{DD} specifications are listed below:

stop I_{DD}, LVI Enabled	Max Spec	Unit
25°C	400	μA
−40° to 105°C	500	μA

stop I_{DD}, LVI Disabled		
25°C	5	μA
−40° to 105°C	50	μA

All product is tested to the maximum specified limits listed below:

stop I_{DD}, LVI Enabled	Max Spec	Unit
25°C	1000	μA
−40° to 105°C	1000	μA

stop I_{DD}, LVI Disabled		
25°C	1000	μA
−40° to 105°C	1000	μA

SPI MODE FAULT RACE CONDITION

Clearing the SPE bit to disable the SPI can cause an error when transmitting in slave mode. In this situation, a race condition occurs, allowing an invalid mode fault to occur.

Mode faults occur on the SPI when the slave select ($\overline{SS}$) pin is toggled during a transmission. Mode faults also occur if $\overline{SS}$ is selected and then unselected before SPSCK returns to its idle level after the shift of the eighth data bit when CPHA = 0 while in slave mode.

When the SPI is disabled, the special port function associated with $\overline{SS}$ is also disabled and returns to a logic 1. In slave mode, $\overline{SS}$ must remain a logic 0 during a transmission. Thus, disabling the SPI causes the $\overline{SS}$ signal to go high internally, which sets up a race for the port logic to send in a logic 1 and the SPI to shut down mode fault detection internally.

Software workaround:

Disable mode faults by clearing the MODFEN bit of the SPSCR register before disabling the SPI in slave mode.

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Additional mask set erratas can be found on the World Wide Web at http://www.mcu.motsps.com/documentation/

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