

Mask Set Errata 4

68HC08AS32 8-Bit Microcontroller Unit

INTRODUCTION

This mask set errata provides information pertaining to the EEPROM applicable to these 68HC08AS32 MCU mask set devices:

- 0J27F
- 1J27F

MCU DEVICE MASK SET IDENTIFICATION

The mask set is identified by a 5-character code consisting of a version number, a letter, two numerical digits, and a letter, for example 0J27F. Slight variations to the mask set identification code may result in an altered version number, for example 1J27F.

MCU DEVICE DATE CODES

Device markings indicate the week of manufacture and the mask set used. The data is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. For instance, the date code "9115" indicates the 15th week of the year 1991.

MCU DEVICE PART NUMBER PREFIXES

Some MCU samples and devices are marked with an SC or XC prefix. An SC prefix denotes special/custom device. An XC prefix denotes that the device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the MC prefix.

Whenever contacting a Motorola representative for assistance, please have the MCU device mask set and date code information available.

Specifications and information herein are subject to change without notice.



EEPROM

The EEPROM module has a logic error in the block protect logic which may result in higher than normal current consumption in stop mode. The operating conditions where the extra current has been observed are $V_{DD} = 5.5\text{ V}$ and $TA > 70\text{ }^{\circ}\text{C}$. The increased current consumption ranges from $10\text{ }\mu\text{A}$ to $200\text{ }\mu\text{A}$.

Either of the following software workarounds will ensure that the EEPROM module is configured in its lowest current state during stop mode.

Workaround 1


Program bits 0 – 3 of the EEPROM non-volatile register (EEBP0 – EEBP3 of location $\$FE1C$) to 0s. Note that this also disables block protection for all four blocks of the EEPROM array.

Workaround 2

Execute this code immediately prior to executing the stop instruction:

```
lda #$0c
sta $feld
lda #$ff
sta $felc
```

Note: *Make sure to insert code to clear the EEPROM control register (location $\$FE1D$) at the beginning of an interrupt service routine if stop mode is exited with an interrupt.*

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