Mask Set Errata 5 68HC908AZ60 8-Bit Microcontroller Unit

INTRODUCTION

This mask set errata provides information pertaining to the index mode instructions applicable to these 68HC908AZ60 MCU mask set devices:

- 2J74Y, 4J74Y
- 5J61D
- 8H62A

MCU DEVICE MASK SET IDENTIFICATION

The mask set is identified by a 5-character code consisting of a version number, a letter, two numerical digits, and a letter, for example 2J74Y. Slight variations to the mask set identification code may result in an altered version number, for example 4J74Y.

MCU DEVICE DATE CODES

Device markings indicate the week of manufacture and the mask set used. The date is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. For instance, the date code "9115" indicates the 15th week of the year 1991.

MCU DEVICE PART NUMBER PREFIXES

Some MCU samples and devices are marked with an SC or XC prefix. An SC prefix denotes special/custom device. An XC prefix denotes that the device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the MC prefix.

When contacting a Motorola representative for assistance, please have the MCU device mask set and date code information available.

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INDEX MODE INSTRUCTIONS

When unmapped locations are accessed with data from an unmapped address using indexed mode instructions, an illegal address reset occurs. For example, the location \$FE15 is not mapped for the 68HC908AZ60. When the location is read using the following instructions, an illegal address reset occurs when LDA , X is executed.

LDHX \$FE15 LDA ,X

The indexed mode instructions that cause this problem are the same instructions that originally came from the M68HC05 such as STA and ORA. However, the newer M68HC08 instructions such as MOV do not cause the illegal address reset.

To avoid this illegal address reset, do not access data from an unmapped location using an instruction with an address determined by the contents of the H:X registers. However, an opcode fetch from an unmapped address generates an illegal reset.

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