Mask Set Errata 2
PC9S12DP256 Microcontroller Unit

INTRODUCTION

This errata provides information applicable to the following MCU mask set devices:

- 0K79X and 1K79X mask of the PC9S12DP256

MCU DEVICE MASK SET IDENTIFICATION

The mask set is identified by a four-character code consisting of a letter, two numerical digits, and a letter, for example F74B. Slight variations to the mask set identification code may result in an optional numerical digit preceding the standard four-character code, for example 0F74B.

MCU DEVICE DATE CODES

Device markings indicate the week of manufacture and the mask set used. The data is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. The date code “9115” would indicate the 15th week of the year 1991.

MCU DEVICE PART NUMBER PREFIXES

Some MCU samples and devices are marked with an SC, PC, ZC or XC prefix. An SC, PC or ZC prefix denotes special/custom device. An XC prefix denotes device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the MC prefix.

ERRATA SYSTEM TRACKING NUMBERS

MUCTS00xxx is the tracking number for device errata. It can be used with the mask set and date code to identify a specific errata to a Motorola representative.

When contacting a Motorola representative for assistance, please have the MCU device mask set and date code information available.

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ERRATA SUMMARY

Errata Number	Module affected	Brief description	Workaround available?	First Issued	
				0K79X	1K79X
MUCts00398	CRG	RTI flag clearing delay when running on PLL Clock	Yes	Rev 1	Rev 2
MUCts00407	ATD	Switching from scan to single mode corrupts data registers	Yes	Rev 1	Rev 2
MUCts00424	ATD	ATD current consumption in low power modes	Yes	Rev 1	Rev 2
MUCts00426	CRG	RTI clocks Remain active if RTIF is set	Yes	Rev 1	Rev 2
MUCts00429	SPI	SPI locks if disabled during message transmission	Yes	Rev 1	Rev 2
MUCts00434	CRG	Self Clock Frequency too high	Yes	Rev 1	Rev 2
MUCts00436	BDM	BDM loses sync when using PLL at high frequencies	Yes	Rev 1	Rev 2

RTI FLAG CLEARING DELAY WHEN RUNNING ON PLL CLOCK
MUCTS00398

If the system is running on the PLL Clock at frequencies greater than 10 times the incoming oscillator clock, a RTI flag clearing sequence initiated immediately prior to executing the WAIT instruction, with the SYSWAI=1 and the PLLWAI=0, may not completely clear the RTI interrupt flag circuitry. This will result in a premature RTI flag and interrupt, if enabled.

Work-around After clearing the RTI flag add a three OSC clock cycle delay prior to entering WAIT mode.

SWITCHING FROM SCAN TO SINGLE MODE CORRUPTS DATA REGISTERS
MUCTS00407

Switching from SCAN mode conversions to SINGLE mode conversion will corrupt the data registers by shifting their values forward by a word. The problem occurs when clearing the SCAN bit in ATDCTL5 during a 8 cycle window when sm2_state[4:0] = 07 and nextState2[4:0] = 06. The end of conversion flag will get set and the register mux control will be incremented immediately (nextRegCnt) so that further single conversions are stored in the wrong register.

Work-around Use the same code with the addition of DISABLING the ATD by first clearing ADPU bit in the ATDCTL2 register, then clearing the SCAN bin in ATDCTL5 to switch to single conversion mode, and then re-enabling the ATD.

ATD CURRENT CONSUMPTION IN LOW POWER MODES MUCTS00424

If any ATD module is enabled when the CPU encounters a stop instruction or the CPU encounters a wait instruction with the ATD stop in wait bit set, ATD current consumption may be out of specification.

Work-around The ATD modules should be disabled prior to entering stop mode.

RTI CLOCKS REMAIN ACTIVE IF RTIF IS SET MUCTS00426

The RTI clock continues to run if the RTIF(RTI interrupt flag) is set, regardless of the RTICTL register setting or RTIWAI bit setting. This can lead to faulty operation in the following scenarios:

1. If WAIT mode is entered with the RTIWAI bit set, RTIE bit cleared, and the RTIF set, the RTI clock, and RTI counters will continue to operate in WAIT mode and consume current.
2. If The RTICTL register is cleared (RTICTL=$00) while the RTIF is set, the RTI clocks will continue to run until the RTIF is cleared.
3. If a new non-zero value is written to the RTICTL register when the RTIF is set, the first RTI time-out period following the write may not be the correct duration.

Work-around Clear the RTICTL register and then RTIF prior to entering WAIT mode or before writing a new non zero value to the RTICTL register.

SPI LOCKS IF DISABLED DURING MESSAGE TRANSMISSION MUCTS00429

In master mode during a transmission SPI locks if SPE bit is cleared. After re-enabling, writing to SPIDR does not result in message transmission.

Work-around Disable the SPI module only if transmission queue is empty (SPTEF=1) and transfer is complete (SPIF=1).

SELF CLOCK FREQUENCY TOO HIGH MUCTS00434

The self clock mode frequency can exceed the maximum specified value. In this case the clock quality check will always fail for EXTAL frequencies below 800kHz. This affects two additional spec values.

1. The clock quality check may fail for EXTAL frequencies below 800kHz. Therefore the crystal oscillator frequency range minimum value is 1.0MHz.
2. The PLL may not lock to the minimum specified PLL frequency of 8.0MHz. Therefore the VCO locking range minimum value is 12.0MHz, which corresponds to a 6.0MHz bus frequency.

Work-around

1. Instead of 500kHz use a 1MHz quartz, resonator or oscillator.
2. Only synthesize PLL frequencies from 12MHz to the maximum specified value. 12MHz PLL frequency corresponds to 6MHz bus frequency.

BDM LOSES SYNC WHEN USING PLL AT HIGH FREQUENCIES MUCTS00436

When using the BDM constant clock source, i.e. CLKSW=0, with the PLL engaged, PLLSEL=1, and the PLL multiplier greater than or equal to 2, the BDM can lose communication with the host system.

Work-around

Do not use the BDM constant clock source with the PLL engaged and a multiplier greater than or equal to 2. Set CLKSW=1 before engaging the PLL.

Additional mask set errata can be found on the World Wide Web at http://www.mcu.motsps.com/documentation/index.html