

Motorola Semiconductor Technical Data

CPU12 Reference Guide

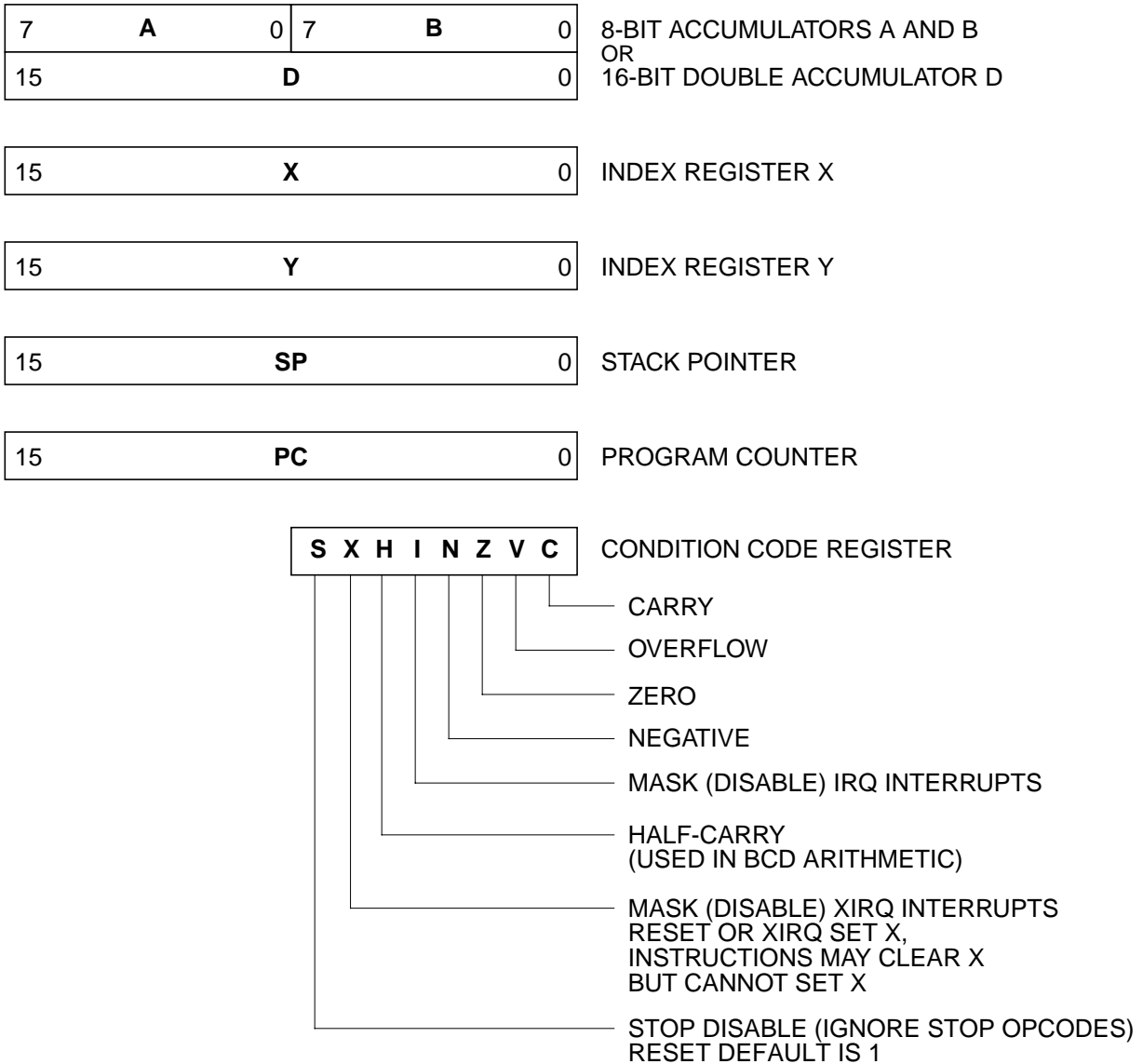
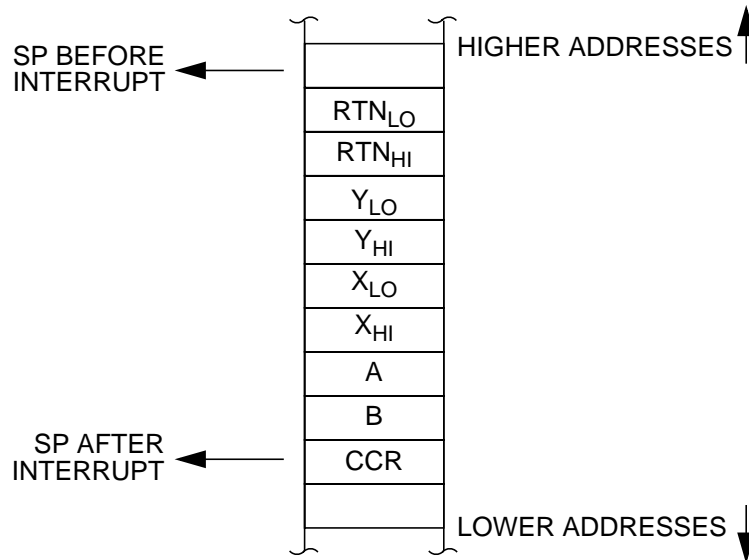


Figure 1. Programming Model

Stack and Memory Layout



STACK UPON ENTRY TO SERVICE ROUTINE
IF SP WAS ODD BEFORE INTERRUPT

SP +8	RTN _{LO}		SP +9
SP +6	Y _{LO}	RTN _{HI}	SP +7
SP +4	X _{LO}	Y _{HI}	SP +5
SP +2	A	X _{HI}	SP +3
SP	CCR	B	SP +1
SP -2			SP -1

STACK UPON ENTRY TO SERVICE ROUTINE
IF SP WAS EVEN BEFORE INTERRUPT

SP +9			SP +10
SP +7	RTN _{HI}	RTN _{LO}	SP +8
SP +5	Y _{HI}	Y _{LO}	SP +6
SP +4	X _{HI}	X _{LO}	SP +4
SP +1	B	A	SP +2
SP -1		CCR	SP

Interrupt Vector Locations

\$FFFE, \$FFFF	Power-On (POR) or External Reset
\$FFFC, \$FFFD	Clock Monitor Reset
\$FFFA, \$FFFB	Computer Operating Properly (COP Watchdog Reset)
\$FFF8, \$FFF9	Unimplemented Opcode Trap
\$FFF6, \$FFF7	Software Interrupt Instruction (SWI)
\$FFF4, \$FFF5	XIRQ
\$FFF2, \$FFF3	IRQ
\$FFC0-\$FFF1	Device-Specific Interrupt Sources

Notation Used in Instruction Set Summary

Explanation of Italic Expressions in Source Form Column

- abc* — A or B or CCR
- abcdxys* — A or B or CCR or D or X or Y or SP. Some assemblers also allow T2 or T3.
- abd* — A or B or D
- abdxys* — A or B or D or X or Y or SP
- dxys* — D or X or Y or SP
- msk8* — 8-bit mask, some assemblers require # symbol before value
- opr8i* — 8-bit immediate value
- opr16i* — 16-bit immediate value
- opr8a* — 8-bit address used with direct address mode
- opr16a* — 16-bit address value
- opr0_xysp* — Indexed addressing postbyte code:
 - opr3,-xys* Predecrement X or Y or SP by 1 . . . 8
 - opr3,+xys* Preincrement X or Y or SP by 1 . . . 8
 - opr3,xys-* Postdecrement X or Y or SP by 1 . . . 8
 - opr3,xys+* Postincrement X or Y or SP by 1 . . . 8
 - opr5,xysp* 5-bit constant offset from X or Y or SP or PC
 - abd,xysp* Accumulator A or B or D offset from X or Y or SP or PC
- opr3* — Any positive integer 1 . . . 8 for pre/post increment/decrement
- opr5* — Any value in the range -16 . . . +15
- opr9* — Any value in the range -256 . . . +255
- opr16* — Any value in the range -32,768 . . . 65,535
- page* — 8-bit value for PPAGE, some assemblers require # symbol before this value
- rel8* — Label of branch destination within -256 to +255 locations
- rel9* — Label of branch destination within -512 to +511 locations
- rel16* — Any label within 64K memory space
- trapnum* — Any 8-bit value in the range \$30-\$39 or \$40-\$FF
- xys* — X or Y or SP
- xysp* — X or Y or SP or PC

Address Modes

IMM	— Immediate
IDX	— Indexed (no extension bytes) includes: 5-bit constant offset Pre/post increment/decrement by 1 . . . 8 Accumulator A, B, or D offset
IDX1	— 9-bit signed offset (1 extension byte)
IDX2	— 16-bit signed offset (2 extension bytes)
[D, IDX]	— Indexed indirect (accumulator D offset)
[IDX2]	— Indexed indirect (16-bit offset)
INH	— Inherent (no operands in object code)
REL	— 2's complement relative offset (branches)

Machine Coding

dd	— 8-bit direct address \$0000 to \$00FF. (High byte assumed to be \$00).
ee	— High-order byte of a 16-bit constant offset for indexed addressing.
eb	— Exchange/Transfer post-byte. See Table 3 on page 23.
ff	— Low-order eight bits of a 9-bit signed constant offset for indexed addressing, or low-order byte of a 16-bit constant offset for indexed addressing.
hh	— High-order byte of a 16-bit extended address.
ii	— 8-bit immediate data value.
jj	— High-order byte of a 16-bit immediate data value.
kk	— Low-order byte of a 16-bit immediate data value.
lb	— Loop primitive (DBNE) post-byte. See Table 4 on page 24.
ll	— Low-order byte of a 16-bit extended address.
mm	— 8-bit immediate mask value for bit manipulation instructions. Set bits indicate bits to be affected.
pg	— Program page (bank) number used in CALL instruction.
qq	— High-order byte of a 16-bit relative offset for long branches.
tn	— Trap number \$30–\$39 or \$40–\$FF.
rr	— Signed relative offset \$80 (–128) to \$7F (+127). Offset relative to the byte following the relative offset byte, or low-order byte of a 16-bit relative offset for long branches.
xb	— Indexed addressing post-byte. See Table 1 on page 21 and Table 2 on page 22.

Access Detail

Each code letter equals one CPU cycle. Uppercase = 16-bit operation and lowercase = 8-bit operation. For complex sequences see the *CPU12 Reference Manual (CPU12RM/AD)*.

- f — Free cycle, CPU doesn't use bus
- g — Read PPAGE internally
- I — Read indirect pointer (indexed indirect)
- i — Read indirect PPAGE value (call indirect)
- n — Write PPAGE internally
- O — Optional program word fetch (P) if instruction is misaligned and has an odd number of bytes of object code — otherwise, appears as a free cycle (f)
- P — Program word fetch (always an aligned word read)
- r — 8-bit data read
- R — 16-bit data read
- s — 8-bit stack write
- S — 16-bit stack write
- w — 8-bit data write
- W — 16-bit data write
- u — 8-bit stack read
- U — 16-bit stack read
- V — 16-bit vector fetch
- t — 8-bit conditional read (or free cycle)
- T — 16-bit conditional read (or free cycle)
- x — 8-bit conditional write

Special Cases

- PPP/P — Short branch, PPP if branch taken, P if not
- OPPP/OPO — Long branch, OPPP if branch taken, OPO if not

Condition Codes Columns

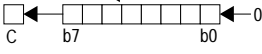
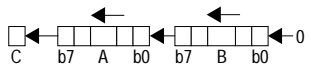
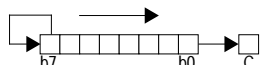
- — Status bit not affected by operation.
- 0 — Status bit cleared by operation.
- 1 — Status bit set by operation.
- Δ — Status bit affected by operation.
- ↓ — Status bit may be cleared or remain set, but is not set by operation.
- ↑ — Status bit may be set or remain cleared, but is not cleared by operation.
- ? — Status bit may be changed by operation but the final state is not defined.
- ! — Status bit used for a special purpose.

Instruction Set Summary

Source Form	Operation	Addr. Mode	Machine Coding (hex)	Access Detail	S	X	H	I	N	Z	V	C
ABA	(A) + (B) ⇒ A Add Accumulators A and B	INH	18 06	OO	-	-	Δ	-	Δ	Δ	Δ	Δ
ABX	(B) + (X) ⇒ X <i>Translates to LEAX B,X</i>	IDX	1A E5	PP ¹	-	-	-	-	-	-	-	-
ABY	(B) + (Y) ⇒ Y <i>Translates to LEAY B,Y</i>	IDX	19 ED	PP ¹	-	-	-	-	-	-	-	-
ADCA #opr8i ADCA opr8a ADCA opr16a ADCA oprx0_xysp ADCA oprx9_xysp ADCA oprx16_xysp ADCA [D,xysp] ADCA [oprx16_xysp]	(A) + (M) + C ⇒ A Add with Carry to A	IMM DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	89 ii 99 dd B9 hh ll A9 xb A9 xb ff A9 xb ee ff A9 xb ee ff	P rfP rOP rfP rPO frPP fIfrfP fIPrfP	-	-	Δ	-	Δ	Δ	Δ	Δ
ADCB #opr8i ADCB opr8a ADCB opr16a ADCB oprx0_xysp ADCB oprx9_xysp ADCB oprx16_xysp ADCB [D,xysp] ADCB [oprx16_xysp]	(B) + (M) + C ⇒ B Add with Carry to B	IMM DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	C9 ii D9 dd F9 hh ll E9 xb E9 xb ff E9 xb ee ff E9 xb ee ff	P rfP rOP rfP rPO frPP fIfrfP fIPrfP	-	-	Δ	-	Δ	Δ	Δ	Δ
ADDA #opr8i ADDA opr8a ADDA opr16a ADDA oprx0_xysp ADDA oprx9_xysp ADDA oprx16_xysp ADDA [D,xysp] ADDA [oprx16_xysp]	(A) + (M) ⇒ A Add without Carry to A	IMM DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	8B ii 9B dd BB hh ll AB xb AB xb ff AB xb ee ff AB xb ee ff	P rfP rOP rfP rPO frPP fIfrfP fIPrfP	-	-	Δ	-	Δ	Δ	Δ	Δ
ADDB #opr8i ADDB opr8a ADDB opr16a ADDB oprx0_xysp ADDB oprx9_xysp ADDB oprx16_xysp ADDB [D,xysp] ADDB [oprx16_xysp]	(B) + (M) ⇒ B Add without Carry to B	IMM DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	CB ii DB dd FB hh ll EB xb EB xb ff EB xb ee ff EB xb ee ff	P rfP rOP rfP rPO frPP fIfrfP fIPrfP	-	-	Δ	-	Δ	Δ	Δ	Δ
ADDD #opr16i ADDD opr8a ADDD opr16a ADDD oprx0_xysp ADDD oprx9_xysp ADDD oprx16_xysp ADDD [D,xysp] ADDD [oprx16_xysp]	(A:B) + (M:M+1) ⇒ A:B Add 16-Bit to D (A:B)	IMM DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	C3 jj kk D3 dd F3 hh ll E3 xb E3 xb ff E3 xb ee ff E3 xb ee ff	OP RfP ROP RfP RPO frPP fIfrfP fIPrfP	-	-	-	-	Δ	Δ	Δ	Δ
ANDA #opr8i ANDA opr8a ANDA opr16a ANDA oprx0_xysp ANDA oprx9_xysp ANDA oprx16_xysp ANDA [D,xysp] ANDA [oprx16_xysp]	(A) • (M) ⇒ A Logical And A with Memory	IMM DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	84 ii 94 dd B4 hh ll A4 xb A4 xb ff A4 xb ee ff A4 xb ee ff	P rfP rOP rfP rPO frPP fIfrfP fIPrfP	-	-	-	-	Δ	Δ	0	-
ANDB #opr8i ANDB opr8a ANDB opr16a ANDB oprx0_xysp ANDB oprx9_xysp ANDB oprx16_xysp ANDB [D,xysp] ANDB [oprx16_xysp]	(B) • (M) ⇒ B Logical And B with Memory	IMM DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	C4 ii D4 dd F4 hh ll E4 xb E4 xb ff E4 xb ee ff E4 xb ee ff	P rfP rOP rfP rPO frPP fIfrfP fIPrfP	-	-	-	-	Δ	Δ	0	-

Note 1. Due to internal CPU requirements, the program word fetch is performed twice to the same address during this instruction.

Instruction Set Summary (Continued)

Source Form	Operation	Addr. Mode	Machine Coding (hex)	Access Detail	S	X	H	I	N	Z	V	C
ANDCC #opr8i	(CCR) • (M) ⇒ CCR Logical And CCR with Memory	IMM	10 ii	P	↓	↓	↓	↓	↓	↓	↓	↓
ASL opr16a ASL oprx0_xysp ASL oprx9_xysp ASL oprx16_xysp ASL [D,xysp] ASL [opr16,xysp] ASLA ASLB	 Arithmetic Shift Left Arithmetic Shift Left Accumulator A Arithmetic Shift Left Accumulator B	EXT IDX IDX1 IDX2 [D,IDX] [IDX2] INH INH	78 hh ll 68 xb 68 xb ff 68 xb ee ff 68 xb 68 xb ee ff 48 58	rOPw rPw rPOw frrPPw fIfrrPw fIPrrPw O O	-	-	-	-	Δ	Δ	Δ	Δ
ASLD	 Arithmetic Shift Left Double	INH	59	O	-	-	-	-	Δ	Δ	Δ	Δ
ASR opr16a ASR oprx0_xysp ASR oprx9_xysp ASR oprx16_xysp ASR [D,xysp] ASR [opr16,xysp] ASRA ASRB	 Arithmetic Shift Right Arithmetic Shift Right Accumulator A Arithmetic Shift Right Accumulator B	EXT IDX IDX1 IDX2 [D,IDX] [IDX2] INH INH	77 hh ll 67 xb 67 xb ff 67 xb ee ff 67 xb 67 xb ee ff 47 57	rOPw rPw rPOw frrPPw fIfrrPw fIPrrPw O O	-	-	-	-	Δ	Δ	Δ	Δ
BCC rel8	Branch if Carry Clear (if C = 0)	REL	24 rr	PPP/P ⁻¹	-	-	-	-	-	-	-	-
BCLR opr8a, msk8 BCLR opr16a, msk8 BCLR oprx0_xysp, msk8 BCLR oprx9_xysp, msk8 BCLR oprx16_xysp, msk8	(M) • (mm) ⇒ M Clear Bit(s) in Memory	DIR EXT IDX IDX1 IDX2	4D dd mm 1D hh ll mm 0D xb mm 0D xb ff mm 0D xb ee ff mm	rPOw rPw rPOw rPwP frrPwOP	-	-	-	-	Δ	Δ	0	-
BCS rel8	Branch if Carry Set (if C = 1)	REL	25 rr	PPP/P ⁻¹	-	-	-	-	-	-	-	-
BEQ rel8	Branch if Equal (if Z = 1)	REL	27 rr	PPP/P ⁻¹	-	-	-	-	-	-	-	-
BGE rel8	Branch if Greater Than or Equal (if N ⊕ V = 0) (signed)	REL	2C rr	PPP/P ⁻¹	-	-	-	-	-	-	-	-
BGND	Place CPU in Background Mode see <i>CPU12 Reference Manual</i>	INH	00	VfPPP	-	-	-	-	-	-	-	-
BGT rel8	Branch if Greater Than (if Z ⊕ (N ⊕ V) = 0) (signed)	REL	2E rr	PPP/P ⁻¹	-	-	-	-	-	-	-	-
BHI rel8	Branch if Higher (if C ⊕ Z = 0) (unsigned)	REL	22 rr	PPP/P ⁻¹	-	-	-	-	-	-	-	-
BHS rel8	Branch if Higher or Same (if C = 0) (unsigned) same function as BCC	REL	24 rr	PPP/P ⁻¹	-	-	-	-	-	-	-	-
BITA #opr8i BITA opr8a BITA opr16a BITA oprx0_xysp BITA oprx9_xysp BITA oprx16_xysp BITA [D,xysp] BITA [opr16,xysp]	(A) • (M) Logical And A with Memory	IMM DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	85 ii 95 dd B5 hh ll A5 xb A5 xb ff A5 xb ee ff A5 xb A5 xb ee ff	P rfP rOP rfP rPO frrPP fIfrrfP fIPrrfP	-	-	-	-	Δ	Δ	0	-
BITB #opr8i BITB opr8a BITB opr16a BITB oprx0_xysp BITB oprx9_xysp BITB oprx16_xysp BITB [D,xysp] BITB [opr16,xysp]	(B) • (M) Logical And B with Memory	IMM DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	C5 ii D5 dd F5 hh ll E5 xb E5 xb ff E5 xb ee ff E5 xb E5 xb ee ff	P rfP rOP rfP rPO frrPP fIfrrfP fIPrrfP	-	-	-	-	Δ	Δ	0	-

Notes: 1. PPP/P indicates this instruction takes three cycles to refill the instruction queue if the branch is taken and one program fetch cycle if the branch is not taken.

Instruction Set Summary (Continued)

Source Form	Operation	Addr. Mode	Machine Coding (hex)	Access Detail	S	X	H	I	N	Z	V	C
BLE <i>rel8</i>	Branch if Less Than or Equal (if $Z \oplus (N \oplus V) = 1$) (signed)	REL	2F <i>rr</i>	PPP/P ¹	-	-	-	-	-	-	-	-
BLO <i>rel8</i>	Branch if Lower (if $C = 1$) (unsigned) same function as BCS	REL	25 <i>rr</i>	PPP/P ¹	-	-	-	-	-	-	-	-
BLS <i>rel8</i>	Branch if Lower or Same (if $C \oplus Z = 1$) (unsigned)	REL	23 <i>rr</i>	PPP/P ¹	-	-	-	-	-	-	-	-
BLT <i>rel8</i>	Branch if Less Than (if $N \oplus V = 1$) (signed)	REL	2D <i>rr</i>	PPP/P ¹	-	-	-	-	-	-	-	-
BMI <i>rel8</i>	Branch if Minus (if $N = 1$)	REL	2B <i>rr</i>	PPP/P ¹	-	-	-	-	-	-	-	-
BNE <i>rel8</i>	Branch if Not Equal (if $Z = 0$)	REL	26 <i>rr</i>	PPP/P ¹	-	-	-	-	-	-	-	-
BPL <i>rel8</i>	Branch if Plus (if $N = 0$)	REL	2A <i>rr</i>	PPP/P ¹	-	-	-	-	-	-	-	-
BRA <i>rel8</i>	Branch Always (if $1 = 1$)	REL	20 <i>rr</i>	PPP	-	-	-	-	-	-	-	-
BRCLR <i>opr8a, msk8, rel8</i> BRCLR <i>opr16a, msk8, rel8</i> BRCLR <i>opr0_xysp, msk8, rel8</i> BRCLR <i>opr9_xysp, msk8, rel8</i> BRCLR <i>opr16_xysp, msk8, rel8</i>	Branch if $(M) \bullet (mm) = 0$ (if All Selected Bit(s) Clear)	DIR EXT IDX IDX1 IDX2	4F <i>dd mm rr</i> 1F <i>hh ll mm rr</i> 0F <i>xb mm rr</i> 0F <i>xb ff mm rr</i> 0F <i>xb ee ff mm rr</i>	rPPP rfPPP rPPP rffPPP frPfPPP	-	-	-	-	-	-	-	-
BRN <i>rel8</i>	Branch Never (if $1 = 0$)	REL	21 <i>rr</i>	P	-	-	-	-	-	-	-	-
BRSET <i>opr8, msk8, rel8</i> BRSET <i>opr16a, msk8, rel8</i> BRSET <i>opr0_xysp, msk8, rel8</i> BRSET <i>opr9_xysp, msk8, rel8</i> BRSET <i>opr16_xysp, msk8, rel8</i>	Branch if $(\bar{M}) \bullet (mm) = 0$ (if All Selected Bit(s) Set)	DIR EXT IDX IDX1 IDX2	4E <i>dd mm rr</i> 1E <i>hh ll mm rr</i> 0E <i>xb mm rr</i> 0E <i>xb ff mm rr</i> 0E <i>xb ee ff mm rr</i>	rPPP rfPPP rPPP rffPPP frPfPPP	-	-	-	-	-	-	-	-
BSET <i>opr8, msk8</i> BSET <i>opr16a, msk8</i> BSET <i>opr0_xysp, msk8</i> BSET <i>opr9_xysp, msk8</i> BSET <i>opr16_xysp, msk8</i>	$(M) \oplus (mm) \Rightarrow M$ Set Bit(s) in Memory	DIR EXT IDX IDX1 IDX2	4C <i>dd mm</i> 1C <i>hh ll mm</i> 0C <i>xb mm</i> 0C <i>xb ff mm</i> 0C <i>xb ee ff mm</i>	rPOw rPPw rPOw rPwP frPwOP	-	-	-	-	Δ	Δ	0	-
BSR <i>rel8</i>	$(SP) - 2 \Rightarrow SP$; $RTN_H:RTN_L \Rightarrow M_{(SP)}:M_{(SP+1)}$ Subroutine address \Rightarrow PC Branch to Subroutine	REL	07 <i>rr</i>	PPPS	-	-	-	-	-	-	-	-
BVC <i>rel8</i>	Branch if Overflow Bit Clear (if $V = 0$)	REL	28 <i>rr</i>	PPP/P ¹	-	-	-	-	-	-	-	-
BVS <i>rel8</i>	Branch if Overflow Bit Set (if $V = 1$)	REL	29 <i>rr</i>	PPP/P ¹	-	-	-	-	-	-	-	-
CALL <i>opr16a, page</i> CALL <i>opr0_xysp, page</i> CALL <i>opr9_xysp, page</i> CALL <i>opr16_xysp, page</i> CALL <i>[D, xysp]</i> CALL <i>[opr16, xysp]</i>	$(SP) - 2 \Rightarrow SP$; $RTN_H:RTN_L \Rightarrow M_{(SP)}:M_{(SP+1)}$ $(SP) - 1 \Rightarrow SP$; $(PPG) \Rightarrow M_{(SP)}$ $pg \Rightarrow$ PPAGE register; Program address \Rightarrow PC Call subroutine in extended memory (Program may be located on another expansion memory page.) Indirect modes get program address and new <i>pg</i> value based on pointer.	EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	4A <i>hh ll pg</i> 4B <i>xb pg</i> 4B <i>xb ff pg</i> 4B <i>xb ee ff pg</i> 4B <i>xb</i> 4B <i>xb ee ff</i>	gnfSsPPP gnfSsPPP gnfSsPPP fgnfSsPPP fIignSsPPP fIignSsPPP	-	-	-	-	-	-	-	-
CBA	$(A) - (B)$ Compare 8-Bit Accumulators	INH	18 17	OO	-	-	-	-	Δ	Δ	Δ	Δ
CLC	$0 \Rightarrow C$ Translates to ANDCC #\$FE	IMM	10 FE	P	-	-	-	-	-	-	-	0
CLI	$0 \Rightarrow I$ Translates to ANDCC #\$EF (enables I-bit interrupts)	IMM	10 EF	P	-	-	-	0	-	-	-	-

Notes

1. PPP/P indicates this instruction takes three cycles to refill the instruction queue if the branch is taken and one program fetch cycle if the branch is not taken.

Instruction Set Summary (Continued)

Source Form	Operation	Addr. Mode	Machine Coding (hex)	Access Detail	S	X	H	I	N	Z	V	C
CLR <i>opr16a</i> CLR <i>opr0_xysp</i> CLR <i>opr9_xysp</i> CLR <i>opr16_xysp</i> CLR [D, <i>xysp</i>] CLR [<i>opr16_xysp</i>] CLRA CLRB	0 ⇒ M Clear Memory Location 0 ⇒ A Clear Accumulator A 0 ⇒ B Clear Accumulator B	EXT IDX IDX1 IDX2 [D,IDX] [IDX2] INH INH	79 hh ll 69 xb 69 xb ff 69 xb ee ff 69 xb 69 xb ee ff 87 C7	wOP Pw PwO PwP PIfPw PIPPw O O	-	-	-	-	0	1	0	0
CLV	0 ⇒ V <i>Translates to ANDCC #\$FD</i>	IMM	10 FD	P	-	-	-	-	-	-	0	-
CMPA # <i>opr8i</i> CMPA <i>opr8a</i> CMPA <i>opr16a</i> CMPA <i>opr0_xysp</i> CMPA <i>opr9_xysp</i> CMPA <i>opr16_xysp</i> CMPA [D, <i>xysp</i>] CMPA [<i>opr16_xysp</i>]	(A) – (M) Compare Accumulator A with Memory	IMM DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	81 ii 91 dd B1 hh ll A1 xb A1 xb ff A1 xb ee ff A1 xb A1 xb ee ff	P rfP rOP rfP rPO frPP fIfrfP fIPrfP	-	-	-	-	Δ	Δ	Δ	Δ
CMPB # <i>opr8i</i> CMPB <i>opr8a</i> CMPB <i>opr16a</i> CMPB <i>opr0_xysp</i> CMPB <i>opr9_xysp</i> CMPB <i>opr16_xysp</i> CMPB [D, <i>xysp</i>] CMPB [<i>opr16_xysp</i>]	(B) – (M) Compare Accumulator B with Memory	IMM DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	C1 ii D1 dd F1 hh ll E1 xb E1 xb ff E1 xb ee ff E1 xb E1 xb ee ff	P rfP rOP rfP rPO frPP fIfrfP fIPrfP	-	-	-	-	Δ	Δ	Δ	Δ
COM <i>opr16a</i> COM <i>opr0_xysp</i> COM <i>opr9_xysp</i> COM <i>opr16_xysp</i> COM [D, <i>xysp</i>] COM [<i>opr16_xysp</i>] COMA COMB	(M) ⇒ M equivalent to \$FF – (M) ⇒ M 1's Complement Memory Location (A) ⇒ A Complement Accumulator A (B) ⇒ B Complement Accumulator B	EXT IDX IDX1 IDX2 [D,IDX] [IDX2] INH INH	71 hh ll 61 xb 61 xb ff 61 xb ee ff 61 xb 61 xb ee ff 41 51	rOPw rPw rPOw frPPw fIfrPw fIPrPw O O	-	-	-	-	Δ	Δ	0	1
CPD # <i>opr16i</i> CPD <i>opr8a</i> CPD <i>opr16a</i> CPD <i>opr0_xysp</i> CPD <i>opr9_xysp</i> CPD <i>opr16_xysp</i> CPD [D, <i>xysp</i>] CPD [<i>opr16_xysp</i>]	(A:B) – (M:M+1) Compare D to Memory (16-Bit)	IMM DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	8C jj kk 9C dd BC hh ll AC xb AC xb ff AC xb ee ff AC xb AC xb ee ff	OP RfP ROP RfP RPO frPP fIfrfP fIPrfP	-	-	-	-	Δ	Δ	Δ	Δ
CPS # <i>opr16i</i> CPS <i>opr8a</i> CPS <i>opr16a</i> CPS <i>opr0_xysp</i> CPS <i>opr9_xysp</i> CPS <i>opr16_xysp</i> CPS [D, <i>xysp</i>] CPS [<i>opr16_xysp</i>]	(SP) – (M:M+1) Compare SP to Memory (16-Bit)	IMM DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	8F jj kk 9F dd BF hh ll AF xb AF xb ff AF xb ee ff AF xb AF xb ee ff	OP RfP ROP RfP RPO frPP fIfrfP fIPrfP	-	-	-	-	Δ	Δ	Δ	Δ
CPX # <i>opr16i</i> CPX <i>opr8a</i> CPX <i>opr16a</i> CPX <i>opr0_xysp</i> CPX <i>opr9_xysp</i> CPX <i>opr16_xysp</i> CPX [D, <i>xysp</i>] CPX [<i>opr16_xysp</i>]	(X) – (M:M+1) Compare X to Memory (16-Bit)	IMM DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	8E jj kk 9E dd BE hh ll AE xb AE xb ff AE xb ee ff AE xb AE xb ee ff	OP RfP ROP RfP RPO frPP fIfrfP fIPrfP	-	-	-	-	Δ	Δ	Δ	Δ
CPY # <i>opr16i</i> CPY <i>opr8a</i> CPY <i>opr16a</i> CPY <i>opr0_xysp</i> CPY <i>opr9_xysp</i> CPY <i>opr16_xysp</i> CPY [D, <i>xysp</i>] CPY [<i>opr16_xysp</i>]	(Y) – (M:M+1) Compare Y to Memory (16-Bit)	IMM DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	8D jj kk 9D dd BD hh ll AD xb AD xb ff AD xb ee ff AD xb AD xb ee ff	OP RfP ROP RfP RPO frPP fIfrfP fIPrfP	-	-	-	-	Δ	Δ	Δ	Δ

Instruction Set Summary (Continued)

Source Form	Operation	Addr. Mode	Machine Coding (hex)	Access Detail	S	X	H	I	N	Z	V	C
DAA	Adjust Sum to BCD Decimal Adjust Accumulator A	INH	18 07	0f0	-	-	-	-	Δ	Δ	?	Δ
DBEQ <i>abdxys, rel9</i>	(cntr) - 1 ⇒ cntr if (cntr) = 0, then Branch else Continue to next instruction Decrement Counter and Branch if = 0 (cntr = A, B, D, X, Y, or SP)	REL (9-bit)	04 1b rr	PPP	-	-	-	-	-	-	-	-
DBNE <i>abdxys, rel9</i>	(cntr) - 1 ⇒ cntr If (cntr) not = 0, then Branch; else Continue to next instruction Decrement Counter and Branch if ≠ 0 (cntr = A, B, D, X, Y, or SP)	REL (9-bit)	04 1b rr	PPP	-	-	-	-	-	-	-	-
DEC <i>opr16a</i> DEC <i>opr0_xysp</i> DEC <i>opr9_xysp</i> DEC <i>opr16_xysp</i> DEC [D, <i>xysp</i>] DEC [<i>opr16_xysp</i>] DECA DECB	(M) - \$01 ⇒ M Decrement Memory Location (A) - \$01 ⇒ A Decrement A (B) - \$01 ⇒ B Decrement B	EXT IDX IDX1 IDX2 [D,IDX] [IDX2] INH INH	73 hh 1l 63 xb 63 xb ff 63 xb ee ff 63 xb 63 xb ee ff 43 53	rOPw rPw rPOw frPPw fIfrPw fIPrPw O O	-	-	-	-	Δ	Δ	Δ	-
DES	(SP) - \$0001 ⇒ SP <i>Translates to LEAS -1,SP</i>	IDX	1B 9F	pp ¹	-	-	-	-	-	-	-	-
DEX	(X) - \$0001 ⇒ X Decrement Index Register X	INH	09	o	-	-	-	-	-	Δ	-	-
DEY	(Y) - \$0001 ⇒ Y Decrement Index Register Y	INH	03	o	-	-	-	-	-	Δ	-	-
EDIV	(Y:D) ÷ (X) ⇒ Y Remainder ⇒ D 32 × 16 Bit ⇒ 16 Bit Divide (unsigned)	INH	11	ffffffefffo	-	-	-	-	Δ	Δ	Δ	Δ
EDIVS	(Y:D) ÷ (X) ⇒ Y Remainder ⇒ D 32 × 16 Bit ⇒ 16 Bit Divide (signed)	INH	18 14	Ofeffeffefffo	-	-	-	-	Δ	Δ	Δ	Δ
EMACS <i>opr16a</i> ²	(M _(X) :M _(X+1)) × (M _(Y) :M _(Y+1)) + (M-M+3) ⇒ M-M+3 16 × 16 Bit ⇒ 32 Bit Multiply and Accumulate (signed)	Special	18 12 hh 1l	ORROffRRRfWwP	-	-	-	-	Δ	Δ	Δ	Δ
EMAXD <i>opr0_xysp</i> EMAXD <i>opr9_xysp</i> EMAXD <i>opr16_xysp</i> EMAXD [D, <i>xysp</i>] EMAXD [<i>opr16_xysp</i>]	MAX((D), (M:M+1)) ⇒ D MAX of 2 Unsigned 16-Bit Values N, Z, V and C status bits reflect result of internal compare ((D) - (M:M+1))	IDX IDX1 IDX2 [D,IDX] [IDX2]	18 1A xb 18 1A xb ff 18 1A xb ee ff 18 1A xb 18 1A xb ee ff	ORfP ORPO OfRPP OfIfrfP OfIPRfP	-	-	-	-	Δ	Δ	Δ	Δ
EMAXM <i>opr0_xysp</i> EMAXM <i>opr9_xysp</i> EMAXM <i>opr16_xysp</i> EMAXM [D, <i>xysp</i>] EMAXM [<i>opr16_xysp</i>]	MAX((D), (M:M+1)) ⇒ M:M+1 MAX of 2 Unsigned 16-Bit Values N, Z, V and C status bits reflect result of internal compare ((D) - (M:M+1))	IDX IDX1 IDX2 [D,IDX] [IDX2]	18 1E xb 18 1E xb ff 18 1E xb ee ff 18 1E xb 18 1E xb ee ff	ORPw ORPwO OfRPwP OfIfrPwP OfIPRwP	-	-	-	-	Δ	Δ	Δ	Δ
EMIND <i>opr0_xysp</i> EMIND <i>opr9_xysp</i> EMIND <i>opr16_xysp</i> EMIND [D, <i>xysp</i>] EMIND [<i>opr16_xysp</i>]	MIN((D), (M:M+1)) ⇒ D MIN of 2 Unsigned 16-Bit Values N, Z, V and C status bits reflect result of internal compare ((D) - (M:M+1))	IDX IDX1 IDX2 [D,IDX] [IDX2]	18 1B xb 18 1B xb ff 18 1B xb ee ff 18 1B xb 18 1B xb ee ff	ORfP ORPO OfRPP OfIfrfP OfIPRfP	-	-	-	-	Δ	Δ	Δ	Δ
EMINM <i>opr0_xysp</i> EMINM <i>opr9_xysp</i> EMINM <i>opr16_xysp</i> EMINM [D, <i>xysp</i>] EMINM [<i>opr16_xysp</i>]	MIN((D), (M:M+1)) ⇒ M:M+1 MIN of 2 Unsigned 16-Bit Values N, Z, V and C status bits reflect result of internal compare ((D) - (M:M+1))	IDX IDX1 IDX2 [D,IDX] [IDX2]	18 1F xb 18 1F xb ff 18 1F xb ee ff 18 1F xb 18 1F xb ee ff	ORPw ORPwO OfRPwP OfIfrPwP OfIPRwP	-	-	-	-	Δ	Δ	Δ	Δ
EMUL	(D) × (Y) ⇒ Y:D 16 × 16 Bit Multiply (unsigned)	INH	13	ffo	-	-	-	-	Δ	Δ	-	Δ

Notes

1. Due to internal CPU requirements, the program word fetch is performed twice to the same address during this instruction.
2. *opr16a* is an extended address specification. Both X and Y point to source operands.

Instruction Set Summary (Continued)

Source Form	Operation	Addr. Mode	Machine Coding (hex)	Access Detail	S	X	H	I	N	Z	V	C
EMULS	(D) × (Y) ⇒ Y:D 16 × 16 Bit Multiply (signed)	INH	18 13	0f0	-	-	-	-	Δ	Δ	-	Δ
EORA #opr8i EORA opr8a EORA opr16a EORA oprx0_xysp EORA oprx9_xysp EORA oprx16_xysp EORA [D,xysp] EORA [opr16,xysp]	(A) ⊕ (M) ⇒ A Exclusive-OR A with Memory	IMM DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	88 ii 98 dd B8 hh ll A8 xb A8 xb ff A8 xb ee ff A8 xb A8 xb ee ff	P rFP rOP rFP rPO frPP fIFrFP fIPrFP	-	-	-	-	Δ	Δ	0	-
EORB #opr8i EORB opr8a EORB opr16a EORB oprx0_xysp EORB oprx9_xysp EORB oprx16_xysp EORB [D,xysp] EORB [opr16,xysp]	(B) ⊕ (M) ⇒ B Exclusive-OR B with Memory	IMM DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	C8 ii D8 dd F8 hh ll E8 xb E8 xb ff E8 xb ee ff E8 xb E8 xb ee ff	P rFP rOP rFP rPO frPP fIFrFP fIPrFP	-	-	-	-	Δ	Δ	0	-
ETBL oprx0_xysp	(M:M+1)+ [(B)×((M+2:M+3) - (M:M+1))] ⇒ D 16-Bit Table Lookup and Interpolate Initialize B, and index before ETBL. <ea> points at first table entry (M:M+1) and B is fractional part of lookup value (no indirect addr. modes or extensions allowed)	IDX	18 3F xb	ORRffffff	-	-	-	-	Δ	Δ	-	?
EXG abcdxys,abcdxys	(r1) ⇔ (r2) (if r1 and r2 same size) or \$00:(r1) ⇒ r2 (if r1=8-bit; r2=16-bit) or (r1 _{low}) ⇔ (r2) (if r1=16-bit; r2=8-bit) r1 and r2 may be A, B, CCR, D, X, Y, or SP	INH	B7 eb	P	-	-	-	-	-	-	-	-
FDIV	(D) ÷ (X) ⇒ X; Remainder ⇒ D 16 × 16 Bit Fractional Divide	INH	18 11	0fffffffff0	-	-	-	-	-	Δ	Δ	Δ
IBEQ abdxys,rel9	(cntr) + 1 ⇒ cntr If (cntr) = 0, then Branch else Continue to next instruction Increment Counter and Branch if = 0 (cntr = A, B, D, X, Y, or SP)	REL (9-bit)	04 lb rr	PPP	-	-	-	-	-	-	-	-
IBNE abdxys,rel9	(cntr) + 1 ⇒ cntr if (cntr) not = 0, then Branch; else Continue to next instruction Increment Counter and Branch if ≠ 0 (cntr = A, B, D, X, Y, or SP)	REL (9-bit)	04 lb rr	PPP	-	-	-	-	-	-	-	-
IDIV	(D) ÷ (X) ⇒ X; Remainder ⇒ D 16 × 16 Bit Integer Divide (unsigned)	INH	18 10	0fffffffff0	-	-	-	-	-	Δ	0	Δ
IDIVS	(D) ÷ (X) ⇒ X; Remainder ⇒ D 16 × 16 Bit Integer Divide (signed)	INH	18 15	0fffffffff0	-	-	-	-	Δ	Δ	Δ	Δ
INC opr16a INC oprx0_xysp INC oprx9_xysp INC oprx16_xysp INC [D,xysp] INC [opr16,xysp] INCA INCB	(M) + \$01 ⇒ M Increment Memory Byte (A) + \$01 ⇒ A Increment Acc. A (B) + \$01 ⇒ B Increment Acc. B	EXT IDX IDX1 IDX2 [D,IDX] [IDX2] INH INH	72 hh ll 62 xb 62 xb ff 62 xb ee ff 62 xb 62 xb ee ff 42 52	rOPw rPw rPOw frPPw fIFrPw fIPrPw O O	-	-	-	-	Δ	Δ	Δ	-
INS	(SP) + \$0001 ⇒ SP Translates to LEAS 1,SP	IDX	1B 81	PP ¹	-	-	-	-	-	-	-	-
INX	(X) + \$0001 ⇒ X Increment Index Register X	INH	08	O	-	-	-	-	-	Δ	-	-
INY	(Y) + \$0001 ⇒ Y Increment Index Register Y	INH	02	O	-	-	-	-	-	Δ	-	-

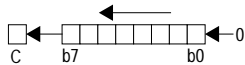
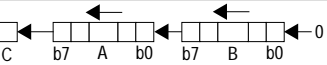
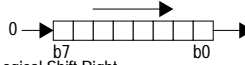
Note 1. Due to internal CPU requirements, the program word fetch is performed twice to the same address during this instruction.

Instruction Set Summary (Continued)

Source Form	Operation	Addr. Mode	Machine Coding (hex)	Access Detail	S	X	H	I	N	Z	V	C
JMP <i>opr16a</i> JMP <i>opr0_xysp</i> JMP <i>opr9_xysp</i> JMP <i>opr16_xysp</i> JMP [D, <i>xysp</i>] JMP [<i>opr16_xysp</i>]	Subroutine address ⇒ PC Jump	EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	06 hh ll 05 xb 05 xb ff 05 xb ee ff 05 xb 05 xb ee ff	PPP PPP PPP fPPP fIfPPP fIfPPP	-	-	-	-	-	-	-	-
JSR <i>opr8a</i> JSR <i>opr16a</i> JSR <i>opr0_xysp</i> JSR <i>opr9_xysp</i> JSR <i>opr16_xysp</i> JSR [D, <i>xysp</i>] JSR [<i>opr16_xysp</i>]	(SP) - 2 ⇒ SP; RTN _H :RTN _L ⇒ M _(SP) :M _(SP+1) ; Subroutine address ⇒ PC Jump to Subroutine	DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	17 dd 16 hh ll 15 xb 15 xb ff 15 xb ee ff 15 xb 15 xb ee ff	PPPS PPPS PPPS PPPS fPPPS fIfPPPS fIfPPPS	-	-	-	-	-	-	-	-
LBCC <i>rel16</i>	Long Branch if Carry Clear (if C = 0)	REL	18 24 qq rr	OPPP/OPO ¹	-	-	-	-	-	-	-	-
LBSC <i>rel16</i>	Long Branch if Carry Set (if C = 1)	REL	18 25 qq rr	OPPP/OPO ¹	-	-	-	-	-	-	-	-
LBEC <i>rel16</i>	Long Branch if Equal (if Z = 1)	REL	18 27 qq rr	OPPP/OPO ¹	-	-	-	-	-	-	-	-
LBGE <i>rel16</i>	Long Branch Greater Than or Equal (if N ⊕ V = 0) (signed)	REL	18 2C qq rr	OPPP/OPO ¹	-	-	-	-	-	-	-	-
LBGT <i>rel16</i>	Long Branch if Greater Than (if Z ⊕ (N ⊕ V) = 0) (signed)	REL	18 2E qq rr	OPPP/OPO ¹	-	-	-	-	-	-	-	-
LBHI <i>rel16</i>	Long Branch if Higher (if C ⊕ Z = 0) (unsigned)	REL	18 22 qq rr	OPPP/OPO ¹	-	-	-	-	-	-	-	-
LBHS <i>rel16</i>	Long Branch if Higher or Same (if C = 0) (unsigned) same function as LBCC	REL	18 24 qq rr	OPPP/OPO ¹	-	-	-	-	-	-	-	-
LBLE <i>rel16</i>	Long Branch if Less Than or Equal (if Z ⊕ (N ⊕ V) = 1) (signed)	REL	18 2F qq rr	OPPP/OPO ¹	-	-	-	-	-	-	-	-
LBLO <i>rel16</i>	Long Branch if Lower (if C = 1) (unsigned) same function as LBSC	REL	18 25 qq rr	OPPP/OPO ¹	-	-	-	-	-	-	-	-
LBLS <i>rel16</i>	Long Branch if Lower or Same (if C ⊕ Z = 1) (unsigned)	REL	18 23 qq rr	OPPP/OPO ¹	-	-	-	-	-	-	-	-
LBLT <i>rel16</i>	Long Branch if Less Than (if N ⊕ V = 1) (signed)	REL	18 2D qq rr	OPPP/OPO ¹	-	-	-	-	-	-	-	-
LBMI <i>rel16</i>	Long Branch if Minus (if N = 1)	REL	18 2B qq rr	OPPP/OPO ¹	-	-	-	-	-	-	-	-
LBNE <i>rel16</i>	Long Branch if Not Equal (if Z = 0)	REL	18 26 qq rr	OPPP/OPO ¹	-	-	-	-	-	-	-	-
LBPL <i>rel16</i>	Long Branch if Plus (if N = 0)	REL	18 2A qq rr	OPPP/OPO ¹	-	-	-	-	-	-	-	-
LBRA <i>rel16</i>	Long Branch Always (if 1 = 1)	REL	18 20 qq rr	OPPP	-	-	-	-	-	-	-	-
LB RN <i>rel16</i>	Long Branch Never (if 1 = 0)	REL	18 21 qq rr	OPO	-	-	-	-	-	-	-	-
LBVC <i>rel16</i>	Long Branch if Overflow Bit Clear (if V = 0)	REL	18 28 qq rr	OPPP/OPO ¹	-	-	-	-	-	-	-	-
LBVS <i>rel16</i>	Long Branch if Overflow Bit Set (if V = 1)	REL	18 29 qq rr	OPPP/OPO ¹	-	-	-	-	-	-	-	-
LDAA # <i>opr8i</i> LDAA <i>opr8a</i> LDAA <i>opr16a</i> LDAA <i>opr0_xysp</i> LDAA <i>opr9_xysp</i> LDAA <i>opr16_xysp</i> LDAA [D, <i>xysp</i>] LDAA [<i>opr16_xysp</i>]	(M) ⇒ A Load Accumulator A	IMM DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	86 ii 96 dd B6 hh ll A6 xb A6 xb ff A6 xb ee ff A6 xb A6 xb ee ff	P rfP rOP rfP rPO frPP fIfrfP fIfrfP	-	-	-	-	Δ	Δ	0	-
LDAB # <i>opr8i</i> LDAB <i>opr8a</i> LDAB <i>opr16a</i> LDAB <i>opr0_xysp</i> LDAB <i>opr9_xysp</i> LDAB <i>opr16_xysp</i> LDAB [D, <i>xysp</i>] LDAB [<i>opr16_xysp</i>]	(M) ⇒ B Load Accumulator B	IMM DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	C6 ii D6 dd F6 hh ll E6 xb E6 xb ff E6 xb ee ff E6 xb E6 xb ee ff	P rfP rOP rfP rPO frPP fIfrfP fIfrfP	-	-	-	-	Δ	Δ	0	-

Note 1. OPPP/OPO indicates this instruction takes four cycles to refill the instruction queue if the branch is taken and three cycles if the branch is not taken.

Instruction Set Summary (Continued)

Source Form	Operation	Addr. Mode	Machine Coding (hex)	Access Detail	S	X	H	I	N	Z	V	C
LDD #opr16i LDD opr8a LDD opr16a LDD oprx0_xysp LDD oprx9_xysp LDD oprx16_xysp LDD [D,xysp] LDD [opr16,xysp]	(M:M+1) ⇒ A:B Load Double Accumulator D (A:B)	IMM DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	CC jj kk DC dd FC hh ll EC xb EC xb ff EC xb ee ff EC xb EC xb ee ff	OP RfP ROP RfP RPO fRPP fIFRfP fIPRfP	-	-	-	-	Δ	Δ	0	-
LDS #opr16i LDS opr8a LDS opr16a LDS oprx0_xysp LDS oprx9_xysp LDS oprx16_xysp LDS [D,xysp] LDS [opr16,xysp]	(M:M+1) ⇒ SP Load Stack Pointer	IMM DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	CF jj kk DF dd FF hh ll EF xb EF xb ff EF xb ee ff EF xb EF xb ee ff	OP RfP ROP RfP RPO fRPP fIFRfP fIPRfP	-	-	-	-	Δ	Δ	0	-
LDX #opr16i LDX opr8a LDX opr16a LDX oprx0_xysp LDX oprx9_xysp LDX oprx16_xysp LDX [D,xysp] LDX [opr16,xysp]	(M:M+1) ⇒ X Load Index Register X	IMM DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	CE jj kk DE dd FE hh ll EE xb EE xb ff EE xb ee ff EE xb EE xb ee ff	OP RfP ROP RfP RPO fRPP fIFRfP fIPRfP	-	-	-	-	Δ	Δ	0	-
LDY #opr16i LDY opr8a LDY opr16a LDY oprx0_xysp LDY oprx9_xysp LDY oprx16_xysp LDY [D,xysp] LDY [opr16,xysp]	(M:M+1) ⇒ Y Load Index Register Y	IMM DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	CD jj kk DD dd FD hh ll ED xb ED xb ff ED xb ee ff ED xb ED xb ee ff	OP RfP ROP RfP RPO fRPP fIFRfP fIPRfP	-	-	-	-	Δ	Δ	0	-
LEAS oprx0_xysp LEAS oprx9_xysp LEAS oprx16_xysp	Effective Address ⇒ SP Load Effective Address into SP	IDX IDX1 IDX2	1B xb 1B xb ff 1B xb ee ff	PP ¹ PO PP	-	-	-	-	-	-	-	-
LEAX oprx0_xysp LEAX oprx9_xysp LEAX oprx16_xysp	Effective Address ⇒ X Load Effective Address into X	IDX IDX1 IDX2	1A xb 1A xb ff 1A xb ee ff	PP ¹ PO PP	-	-	-	-	-	-	-	-
LEAY oprx0_xysp LEAY oprx9_xysp LEAY oprx16_xysp	Effective Address ⇒ Y Load Effective Address into Y	IDX IDX1 IDX2	19 xb 19 xb ff 19 xb ee ff	PP ¹ PO PP	-	-	-	-	-	-	-	-
LSL opr16a LSL oprx0_xysp LSL oprx9_xysp LSL oprx16_xysp LSL [D,xysp] LSL [opr16,xysp] LSLA LSLB	 Logical Shift Left same function as ASL	EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	78 hh ll 68 xb 68 xb ff 68 xb ee ff 68 xb 68 xb ee ff	rOPw rPw rPOw fRPPw fIFrPw fIPrPw	-	-	-	-	Δ	Δ	Δ	Δ
LSLD	 Logical Shift Left D Accumulator same function as ASLD	INH	59	O	-	-	-	-	Δ	Δ	Δ	Δ
LSR opr16a LSR oprx0_xysp LSR oprx9_xysp LSR oprx16_xysp LSR [D,xysp] LSR [opr16_xysp] LSRA LSRB	 Logical Shift Right	EXT IDX IDX1 IDX2 [D,IDX] [IDX2] INH INH	74 hh ll 64 xb 64 xb ff 64 xb ee ff 64 xb 64 xb ee ff 44 54	rOPw rPw rPOw fRPPw fIFrPw fIPrPw O O	-	-	-	-	0	Δ	Δ	Δ

Note 1. Due to internal CPU requirements, the program word fetch is performed twice to the same address during this instruction.

Instruction Set Summary (Continued)

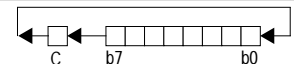
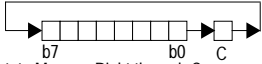
Source Form	Operation	Addr. Mode	Machine Coding (hex)	Access Detail	S	X	H	I	N	Z	V	C
LSRD	<p>Logical Shift Right D Accumulator</p>	INH	49	0	-	-	-	-	0	Δ	Δ	Δ
MAXA <i>opr</i> x0_ysp MAXA <i>opr</i> x9_ysp MAXA <i>opr</i> x16_ysp MAXA [D,ysp] MAXA [<i>opr</i> x16,ysp]	$\text{MAX}((A), (M)) \Rightarrow A$ MAX of 2 Unsigned 8-Bit Values N, Z, V and C status bits reflect result of internal compare $((A) - (M))$.	IDX IDX1 IDX2 [D,IDX] [IDX2]	18 18 xb 18 18 xb ff 18 18 xb ee ff 18 18 xb 18 18 xb ee ff	OrfP OrPO OfrrPP OfIfrrFP OfIPrrFP	-	-	-	-	Δ	Δ	Δ	Δ
MAXM <i>opr</i> x0_ysp MAXM <i>opr</i> x9_ysp MAXM <i>opr</i> x16_ysp MAXM [D,ysp] MAXM [<i>opr</i> x16,ysp]	$\text{MAX}((A), (M)) \Rightarrow M$ MAX of 2 Unsigned 8-Bit Values N, Z, V and C status bits reflect result of internal compare $((A) - (M))$.	IDX IDX1 IDX2 [D,IDX] [IDX2]	18 1C xb 18 1C xb ff 18 1C xb ee ff 18 1C xb 18 1C xb ee ff	OrPw OrPwO OfrrPwP OfIfrrPw OfIPrrPw	-	-	-	-	Δ	Δ	Δ	Δ
MEM	$\mu(\text{grade}) \Rightarrow M_{(y)}$ $(X) + 4 \Rightarrow X; (Y) + 1 \Rightarrow Y; A$ unchanged if $(A) < P1$ or $(A) > P2$ then $\mu = 0$, else $\mu = \text{MIN}(((A) - P1) \times S1, (P2 - (A)) \times S2, \$FF)$ where: A = current crisp input value; X points at 4-byte data structure that describes a trapezoidal membership function (P1, P2, S1, S2); Y points at fuzzy input (RAM location). See <i>CPU12 Reference Manual</i> for special cases.	Special	01	RRfOw	-	-	?	-	?	?	?	?
MINA <i>opr</i> x0_ysp MINA <i>opr</i> x9_ysp MINA <i>opr</i> x16_ysp MINA [D,ysp] MINA [<i>opr</i> x16,ysp]	$\text{MIN}((A), (M)) \Rightarrow A$ MIN of 2 Unsigned 8-Bit Values N, Z, V and C status bits reflect result of internal compare $((A) - (M))$.	IDX IDX1 IDX2 [D,IDX] [IDX2]	18 19 xb 18 19 xb ff 18 19 xb ee ff 18 19 xb 18 19 xb ee ff	OrfP OrPO OfrrPP OfIfrrFP OfIPrrFP	-	-	-	-	Δ	Δ	Δ	Δ
MINM <i>opr</i> x0_ysp MINM <i>opr</i> x9_ysp MINM <i>opr</i> x16_ysp MINM [D,ysp] MINM [<i>opr</i> x16,ysp]	$\text{MIN}((A), (M)) \Rightarrow M$ MIN of 2 Unsigned 8-Bit Values N, Z, V and C status bits reflect result of internal compare $((A) - (M))$.	IDX IDX1 IDX2 [D,IDX] [IDX2]	18 1D xb 18 1D xb ff 18 1D xb ee ff 18 1D xb 18 1D xb ee ff	OrPw OrPwO OfrrPwP OfIfrrPw OfIPrrPw	-	-	-	-	Δ	Δ	Δ	Δ
MOVB # <i>opr</i> 8, <i>opr</i> 16a ¹ MOVB # <i>opr</i> 8i, <i>opr</i> x0_ysp ¹ MOVB <i>opr</i> 16a, <i>opr</i> 16a ¹ MOVB <i>opr</i> 16a, <i>opr</i> x0_ysp ¹ MOVB <i>opr</i> x0_ysp, <i>opr</i> 16a ¹ MOVB <i>opr</i> x0_ysp, <i>opr</i> x0_ysp ¹	$(M_1) \Rightarrow M_2$ Memory to Memory Byte-Move (8-Bit)	IMM-EXT IMM-IDX EXT-EXT EXT-IDX IDX-EXT IDX-IDX	18 0B ii hh ll 18 08 xb ii 18 0C hh ll hh ll 18 09 xb hh ll 18 0D xb hh ll 18 0A xb xb	OPwP OPwO OrPwPO OPrrPw OrPwP OrPwO	-	-	-	-	-	-	-	-
MOVW # <i>opr</i> x16, <i>opr</i> 16a ¹ MOVW # <i>opr</i> 16i, <i>opr</i> x0_ysp ¹ MOVW <i>opr</i> 16a, <i>opr</i> 16a ¹ MOVW <i>opr</i> 16a, <i>opr</i> x0_ysp ¹ MOVW <i>opr</i> x0_ysp, <i>opr</i> 16a ¹ MOVW <i>opr</i> x0_ysp, <i>opr</i> x0_ysp ¹	$(M:M+1_1) \Rightarrow M:M+1_2$ Memory to Memory Word-Move (16-Bit)	IMM-EXT IMM-IDX EXT-EXT EXT-IDX IDX-EXT IDX-IDX	18 03 jj kk hh ll 18 00 xb jj kk 18 04 hh ll hh ll 18 01 xb hh ll 18 05 xb hh ll 18 02 xb xb	OPwPO OPwP ORPwPO ORPwP ORPwO	-	-	-	-	-	-	-	-
MUL	$(A) \times (B) \Rightarrow A:B$ 8 × 8 Unsigned Multiply	INH	12	fFO	-	-	-	-	-	-	-	Δ
NEG <i>opr</i> 16a NEG <i>opr</i> x0_ysp NEG <i>opr</i> x9_ysp NEG <i>opr</i> x16_ysp NEG [D,ysp] NEG [<i>opr</i> x16,ysp] NEGA NEGB	$0 - (M) \Rightarrow M$ or $(\bar{M}) + 1 \Rightarrow M$ Two's Complement Negate $0 - (A) \Rightarrow A$ equivalent to $(\bar{A}) + 1 \Rightarrow A$ Negate Accumulator A $0 - (B) \Rightarrow B$ equivalent to $(\bar{B}) + 1 \Rightarrow B$ Negate Accumulator B	EXT IDX IDX1 IDX2 [D,IDX] [IDX2] INH	70 hh ll 60 xb 60 xb ff 60 xb ee ff 60 xb 60 xb ee ff 40	rOPw rPw rPOw frrPPw fIfrrPw fIPrrPw O	-	-	-	-	Δ	Δ	Δ	Δ
NOP	No Operation	INH	A7	0	-	-	-	-	-	-	-	-

Note 1. The first operand in the source code statement specifies the source for the move.

Instruction Set Summary (Continued)

Source Form	Operation	Addr. Mode	Machine Coding (hex)	Access Detail	S	X	H	I	N	Z	V	C
ORAA #opr8i ORAA opr8a ORAA opr16a ORAA oprx0_xysp ORAA oprx9_xysp ORAA oprx16_xysp ORAA [D,xysp] ORAA [oprx16,xysp]	(A) ← (M) ⇒ A Logical OR A with Memory	IMM DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	8A ii 9A dd BA hh ll AA xb AA xb ff AA xb ee ff AA xb AA xb ee ff	P rFP rOP rFP rPO frPP fIFrFP fIPrFP	-	-	-	-	Δ	Δ	0	-
ORAB #opr8i ORAB opr8a ORAB opr16a ORAB oprx0_xysp ORAB oprx9_xysp ORAB oprx16_xysp ORAB [D,xysp] ORAB [oprx16,xysp]	(B) ← (M) ⇒ B Logical OR B with Memory	IMM DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	CA ii DA dd FA hh ll EA xb EA xb ff EA xb ee ff EA xb EA xb ee ff	P rFP rOP rFP rPO frPP fIFrFP fIPrFP	-	-	-	-	Δ	Δ	0	-
ORCC #opr8i	(CCR) ← M ⇒ CCR Logical OR CCR with Memory	IMM	14 ii	P	↑	-	↑	↑	↑	↑	↑	↑
PSHA	(SP) - 1 ⇒ SP; (A) ⇒ M _(SP) Push Accumulator A onto Stack	INH	36	OS	-	-	-	-	-	-	-	-
PSHB	(SP) - 1 ⇒ SP; (B) ⇒ M _(SP) Push Accumulator B onto Stack	INH	37	OS	-	-	-	-	-	-	-	-
PSHC	(SP) - 1 ⇒ SP; (CCR) ⇒ M _(SP) Push CCR onto Stack	INH	39	OS	-	-	-	-	-	-	-	-
PSHD	(SP) - 2 ⇒ SP; (A:B) ⇒ M _(SP) :M _(SP+1) Push D Accumulator onto Stack	INH	3B	OS	-	-	-	-	-	-	-	-
PSHX	(SP) - 2 ⇒ SP; (X _H :X _L) ⇒ M _(SP) :M _(SP+1) Push Index Register X onto Stack	INH	34	OS	-	-	-	-	-	-	-	-
PSHY	(SP) - 2 ⇒ SP; (Y _H :Y _L) ⇒ M _(SP) :M _(SP+1) Push Index Register Y onto Stack	INH	35	OS	-	-	-	-	-	-	-	-
PULA	M _(SP) ⇒ A; (SP) + 1 ⇒ SP Pull Accumulator A from Stack	INH	32	uFO	-	-	-	-	-	-	-	-
PULB	M _(SP) ⇒ B; (SP) + 1 ⇒ SP Pull Accumulator B from Stack	INH	33	uFO	-	-	-	-	-	-	-	-
PULC	M _(SP) ⇒ CCR; (SP) + 1 ⇒ SP Pull CCR from Stack	INH	38	uFO	Δ	↓	Δ	Δ	Δ	Δ	Δ	Δ
PULD	M _(SP) :M _(SP+1) ⇒ A:B; (SP) + 2 ⇒ SP Pull D from Stack	INH	3A	uFO	-	-	-	-	-	-	-	-
PULX	M _(SP) :M _(SP+1) ⇒ X _H :X _L ; (SP) + 2 ⇒ SP Pull Index Register X from Stack	INH	30	uFO	-	-	-	-	-	-	-	-
PULY	M _(SP) :M _(SP+1) ⇒ Y _H :Y _L ; (SP) + 2 ⇒ SP Pull Index Register Y from Stack	INH	31	uFO	-	-	-	-	-	-	-	-

Instruction Set Summary (Continued)

Source Form	Operation	Addr. Mode	Machine Coding (hex)	Access Detail	S	X	H	I	N	Z	V	C
REV (add if interrupted)	MIN-MAX rule evaluation Find smallest rule input (MIN). Store to rule outputs unless fuzzy output is already larger (MAX). For rule weights see REVW. Each rule input is an 8-bit offset from the base address in Y. Each rule output is an 8-bit offset from the base address in Y. \$FE separates rule inputs from rule outputs. \$FF terminates the rule list. REV may be interrupted.	Special	18 3A	$Orf(tTx)o^1$ $ff + Orf$	-	-	?	-	?	?	Δ	?
REVV (add 2 at end of ins if wts) (add if interrupted)	MIN-MAX rule evaluation Find smallest rule input (MIN). Store to rule outputs unless fuzzy output is already larger (MAX). Rule weights supported, optional. Each rule input is the 16-bit address of a fuzzy input. Each rule output is the 16-bit address of a fuzzy output. The value \$FFE separates rule inputs from rule outputs. \$FFF terminates the rule list. REVV may be interrupted.	Special	18 3B	$ORf(tTx)o^2$ $(rffRf)^2$ $fff + ORf$	-	-	?	-	?	?	Δ	!
ROL <i>opr16a</i> ROL <i>opr0_xysp</i> ROL <i>opr9_xysp</i> ROL <i>opr16_xysp</i> ROL [D,xysp] ROL [opr16,xysp] ROLA ROLB	 Rotate Memory Left through Carry Rotate A Left through Carry Rotate B Left through Carry	EXT IDX IDX1 IDX2 [D,IDX] [IDX2] INH INH	75 hh ll 65 xb 65 xb ff 65 xb ee ff 65 xb 65 xb ee ff 45 55	rOPw rPw rPOw fRPPw fIFrPw fIPrPw O O	-	-	-	-	Δ	Δ	Δ	Δ
ROR <i>opr16a</i> ROR <i>opr0_xysp</i> ROR <i>opr9_xysp</i> ROR <i>opr16_xysp</i> ROR [D,xysp] ROR [opr16,xysp] RORA RORB	 Rotate Memory Right through Carry Rotate A Right through Carry Rotate B Right through Carry	EXT IDX IDX1 IDX2 [D,IDX] [IDX2] INH INH	76 hh ll 66 xb 66 xb ff 66 xb ee ff 66 xb 66 xb ee ff 46 56	rOPw rPw rPOw fRPPw fIFrPw fIPrPw O O	-	-	-	-	Δ	Δ	Δ	Δ
RTC	$(M_{(SP)} \Rightarrow PPAGE; (SP) + 1 \Rightarrow SP;$ $(M_{(SP)}:M_{(SP+1)} \Rightarrow PC_H:PC_L;$ $(SP) + 2 \Rightarrow SP$ Return from Call	INH	0A	uUnPPP	-	-	-	-	-	-	-	-
RTI (if interrupt pending)	$(M_{(SP)} \Rightarrow CCR; (SP) + 1 \Rightarrow SP$ $(M_{(SP)}:M_{(SP+1)} \Rightarrow B:A; (SP) + 2 \Rightarrow SP$ $(M_{(SP)}:M_{(SP+1)} \Rightarrow X_H:X_L; (SP) + 4 \Rightarrow SP$ $(M_{(SP)}:M_{(SP+1)} \Rightarrow PC_H:PC_L; (SP) - 2 \Rightarrow SP$ $(M_{(SP)}:M_{(SP+1)} \Rightarrow Y_H:Y_L;$ $(SP) + 4 \Rightarrow SP$ Return from Interrupt	INH	0B	uUUUUPPP uUUUUvFPpP	Δ	↓	Δ	Δ	Δ	Δ	Δ	Δ
RTS	$(M_{(SP)}:M_{(SP+1)} \Rightarrow PC_H:PC_L;$ $(SP) + 2 \Rightarrow SP$ Return from Subroutine	INH	3D	UfPPP	-	-	-	-	-	-	-	-
SBA	$(A) - (B) \Rightarrow A$ Subtract B from A	INH	18 16	oo	-	-	-	-	Δ	Δ	Δ	Δ

Notes:

- The 3-cycle loop in parentheses is executed once for each element in the rule list. When an interrupt occurs, there is a 2-cycle exit sequence, a 4-cycle re-entry sequence, then execution resumes with a prefetch of the last antecedent or consequent being processed at the time of the interrupt.
- The 3-cycle loop in parentheses expands to 5 cycles for separators when weighting is enabled. The loop is executed once for each element in the rule list. When an interrupt occurs, there is a 2-cycle exit sequence, a 4-cycle re-entry sequence, then execution resumes with a prefetch of the last antecedent or consequent being processed at the time of the interrupt.

Instruction Set Summary (Continued)

Source Form	Operation	Addr. Mode	Machine Coding (hex)	Access Detail	S	X	H	I	N	Z	V	C
SBCA #opr8i SBCA opr8a SBCA opr16a SBCA oprx0_xysp SBCA oprx9_xysp SBCA oprx16_xysp SBCA [D,xysp] SBCA [opr16,xysp]	(A) - (M) - C ⇒ A Subtract with Borrow from A	IMM DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	82 ii 92 dd B2 hh ll A2 xb A2 xb ff A2 xb ee ff A2 xb A2 xb ee ff	P rFP rOP rFP rPO frPP fIFrFP fIPrFP	-	-	-	-	Δ	Δ	Δ	Δ
SBCB #opr8i SBCB opr8a SBCB opr16a SBCB oprx0_xysp SBCB oprx9_xysp SBCB oprx16_xysp SBCB [D,xysp] SBCB [opr16,xysp]	(B) - (M) - C ⇒ B Subtract with Borrow from B	IMM DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	C2 ii D2 dd F2 hh ll E2 xb E2 xb ff E2 xb ee ff E2 xb E2 xb ee ff	P rFP rOP rFP rPO frPP fIFrFP fIPrFP	-	-	-	-	Δ	Δ	Δ	Δ
SEC	1 ⇒ C Translates to ORCC #01	IMM	14 01	P	-	-	-	-	-	-	-	1
SEI	1 ⇒ I; (inhibit I interrupts) Translates to ORCC #10	IMM	14 10	P	-	-	-	1	-	-	-	-
SEV	1 ⇒ V Translates to ORCC #02	IMM	14 02	P	-	-	-	-	-	-	1	-
SEX abc,dxys	\$00:(r1) ⇒ r2 if r1, bit 7 is 0 or \$FF:(r1) ⇒ r2 if r1, bit 7 is 1 Sign Extend 8-bit r1 to 16-bit r2 r1 may be A, B, or CCR r2 may be D, X, Y, or SP Alternate mnemonic for TFR r1, r2	INH	B7 eb	P	-	-	-	-	-	-	-	-
STAA opr8a STAA opr16a STAA oprx0_xysp STAA oprx9_xysp STAA oprx16_xysp STAA [D,xysp] STAA [opr16,xysp]	(A) ⇒ M Store Accumulator A to Memory	DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	5A dd 7A hh ll 6A xb 6A xb ff 6A xb ee ff 6A xb 6A xb ee ff	Pw wOP Pw PwO PwP PIfPw PIPPw	-	-	-	-	Δ	Δ	0	-
STAB opr8a STAB opr16a STAB oprx0_xysp STAB oprx9_xysp STAB oprx16_xysp STAB [D,xysp] STAB [opr16,xysp]	(B) ⇒ M Store Accumulator B to Memory	DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	5B dd 7B hh ll 6B xb 6B xb ff 6B xb ee ff 6B xb 6B xb ee ff	Pw wOP Pw PwO PwP PIfPw PIPPw	-	-	-	-	Δ	Δ	0	-
STD opr8a STD opr16a STD oprx0_xysp STD oprx9_xysp STD oprx16_xysp STD [D,xysp] STD [opr16,xysp]	(A) ⇒ M, (B) ⇒ M+1 Store Double Accumulator	DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	5C dd 7C hh ll 6C xb 6C xb ff 6C xb ee ff 6C xb 6C xb ee ff	PW WOP PW PWO PWP PIfPW PIPPW	-	-	-	-	Δ	Δ	0	-
STOP (entering STOP) (exiting STOP) (continue) (if STOP disabled)	(SP) - 2 ⇒ SP; RTN _H :RTN _L ⇒ M _(SP) :M _(SP+1) ; (SP) - 2 ⇒ SP; (Y _H :Y _L) ⇒ M _(SP) :M _(SP+1) ; (SP) - 2 ⇒ SP; (X _H :X _L) ⇒ M _(SP) :M _(SP+1) ; (SP) - 2 ⇒ SP; (B:A) ⇒ M _(SP) :M _(SP+1) ; (SP) - 1 ⇒ SP; (CCR) ⇒ M _(SP) ; STOP All Clocks If S control bit = 1, the STOP instruction is disabled and acts like a two-cycle NOP. Registers stacked to allow quicker recovery by interrupt.	INH	18 3E	OOSSESs fVFPPP fO OO	-	-	-	-	-	-	-	-

Instruction Set Summary (Continued)

Source Form	Operation	Addr. Mode	Machine Coding (hex)	Access Detail	S	X	H	I	N	Z	V	C
STS <i>opr8a</i> STS <i>opr16a</i> STS <i>opr0_xysp</i> STS <i>opr9_xysp</i> STS <i>opr16_xysp</i> STS [D, <i>xysp</i>] STS [<i>opr16_xysp</i>]	(SP _H :SP _L) ⇒ M:M+1 Store Stack Pointer	DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	5F dd 7F hh ll 6F xb 6F xb ff 6F xb ee ff 6F xb 6F xb ee ff	PW WOP PW PWO PWP PIfPW PIPPW	-	-	-	-	Δ	Δ	0	-
STX <i>opr8a</i> STX <i>opr16a</i> STX <i>opr0_xysp</i> STX <i>opr9_xysp</i> STX <i>opr16_xysp</i> STX [D, <i>xysp</i>] STX [<i>opr16_xysp</i>]	(X _H :X _L) ⇒ M:M+1 Store Index Register X	DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	5E dd 7E hh ll 6E xb 6E xb ff 6E xb ee ff 6E xb 6E xb ee ff	PW WOP PW PWO PWP PIfPW PIPPW	-	-	-	-	Δ	Δ	0	-
STY <i>opr8a</i> STY <i>opr16a</i> STY <i>opr0_xysp</i> STY <i>opr9_xysp</i> STY <i>opr16_xysp</i> STY [D, <i>xysp</i>] STY [<i>opr16_xysp</i>]	(Y _H :Y _L) ⇒ M:M+1 Store Index Register Y	DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	5D dd 7D hh ll 6D xb 6D xb ff 6D xb ee ff 6D xb 6D xb ee ff	PW WOP PW PWO PWP PIfPW PIPPW	-	-	-	-	Δ	Δ	0	-
SUBA # <i>opr8i</i> SUBA <i>opr8a</i> SUBA <i>opr16a</i> SUBA <i>opr0_xysp</i> SUBA <i>opr9_xysp</i> SUBA <i>opr16_xysp</i> SUBA [D, <i>xysp</i>] SUBA [<i>opr16_xysp</i>]	(A) - (M) ⇒ A Subtract Memory from Accumulator A	IMM DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	80 ii 90 dd B0 hh ll A0 xb A0 xb ff A0 xb ee ff A0 xb A0 xb ee ff	P rfP rOP rfP rPO frPP fIfrfP fIPrfP	-	-	-	-	Δ	Δ	Δ	Δ
SUBB # <i>opr8i</i> SUBB <i>opr8a</i> SUBB <i>opr16a</i> SUBB <i>opr0_xysp</i> SUBB <i>opr9_xysp</i> SUBB <i>opr16_xysp</i> SUBB [D, <i>xysp</i>] SUBB [<i>opr16_xysp</i>]	(B) - (M) ⇒ B Subtract Memory from Accumulator B	IMM DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	C0 ii D0 dd F0 hh ll E0 xb E0 xb ff E0 xb ee ff E0 xb E0 xb ee ff	P rfP rOP rfP rPO frPP fIfrfP fIPrfP	-	-	-	-	Δ	Δ	Δ	Δ
SUBD # <i>opr16i</i> SUBD <i>opr8a</i> SUBD <i>opr16a</i> SUBD <i>opr0_xysp</i> SUBD <i>opr9_xysp</i> SUBD <i>opr16_xysp</i> SUBD [D, <i>xysp</i>] SUBD [<i>opr16_xysp</i>]	(D) - (M:M+1) ⇒ D Subtract Memory from D (A:B)	IMM DIR EXT IDX IDX1 IDX2 [D,IDX] [IDX2]	83 jj kk 93 dd B3 hh ll A3 xb A3 xb ff A3 xb ee ff A3 xb A3 xb ee ff	OP RfP ROP RfP RPO fRPP fIfRfP fIPrfP	-	-	-	-	Δ	Δ	Δ	Δ
SWI	(SP) - 2 ⇒ SP; RTN _H :RTN _L ⇒ M _(SP) :M _(SP+1) ; (SP) - 2 ⇒ SP; (Y _H :Y _L) ⇒ M _(SP) :M _(SP+1) ; (SP) - 2 ⇒ SP; (X _H :X _L) ⇒ M _(SP) :M _(SP+1) ; (SP) - 2 ⇒ SP; (B:A) ⇒ M _(SP) :M _(SP+1) ; (SP) - 1 ⇒ SP; (CCR) ⇒ M _(SP) 1 ⇒ I; (SWI Vector) ⇒ PC Software Interrupt	INH	3F	VSPSSPS _{SP} ¹	-	-	-	1	-	-	-	-
TAB	(A) ⇒ B Transfer A to B	INH	18 0E	OO	-	-	-	-	Δ	Δ	0	-
TAP	(A) ⇒ CCR <i>Translates to TFR A, CCR</i>	INH	B7 02	P	Δ	↓	Δ	Δ	Δ	Δ	Δ	Δ
TBA	(B) ⇒ A Transfer B to A	INH	18 0F	OO	-	-	-	-	Δ	Δ	0	-

Note 1. The CPU also uses the SWI processing sequence for hardware interrupts and unimplemented opcode traps. A variation of the sequence (VfPPP) is used for resets.

Instruction Set Summary (Continued)

Source Form	Operation	Addr. Mode	Machine Coding (hex)	Access Detail	S	X	H	I	N	Z	V	C
TBEQ <i>abdxys,rel9</i>	If (cntr) = 0, then Branch; else Continue to next instruction Test Counter and Branch if Zero (cntr = A, B, D, X, Y, or SP)	REL (9-bit)	04 1b rr	PPP	-	-	-	-	-	-	-	-
TBL <i>opr0_xysp</i>	$(M) + [(B) \times ((M+1) - (M))] \Rightarrow A$ 8-Bit Table Lookup and Interpolate Initialize B, and index before TBL. <ea> points at first 8-bit table entry (M) and B is fractional part of lookup value. (no indirect addressing modes or extensions allowed)	IDX	18 3D xb	OrrffffP	-	-	-	-	Δ	Δ	-	?
TBNE <i>abdxys,rel9</i>	If (cntr) not = 0, then Branch; else Continue to next instruction Test Counter and Branch if Not Zero (cntr = A, B, D, X, Y, or SP)	REL (9-bit)	04 1b rr	PPP	-	-	-	-	-	-	-	-
TFR <i>abcdxys,abcdxys</i>	(r1) \Rightarrow r2 or \$00:(r1) \Rightarrow r2 or (r1[7:0]) \Rightarrow r2 Transfer Register to Register r1 and r2 may be A, B, CCR, D, X, Y, or SP	INH	B7 eb	P	- or Δ	- \downarrow	- Δ	- Δ	- Δ	- Δ	- Δ	- Δ
TPA	(CCR) \Rightarrow A <i>Translates to TFR CCR ,A</i>	INH	B7 20	P	-	-	-	-	-	-	-	-
TRAP <i>trapnum</i>	(SP) - 2 \Rightarrow SP; RTN _H :RTN _L \Rightarrow M _{(SP):M_(SP+1)} ; (SP) - 2 \Rightarrow SP; (Y _H :Y _L) \Rightarrow M _{(SP):M_(SP+1)} ; (SP) - 2 \Rightarrow SP; (X _H :X _L) \Rightarrow M _{(SP):M_(SP+1)} ; (SP) - 2 \Rightarrow SP; (B:A) \Rightarrow M _{(SP):M_(SP+1)} ; (SP) - 1 \Rightarrow SP; (CCR) \Rightarrow M _(SP) 1 \Rightarrow I; (TRAP Vector) \Rightarrow PC Unimplemented opcode trap	INH	18 tn tn = \$30-\$39 or \$40-\$FF	OfVSPSSPSsP	-	-	-	1	-	-	-	-
TST <i>opr16a</i> TST <i>opr0_xysp</i> TST <i>opr9_xysp</i> TST <i>opr16_xysp</i> TST [D, <i>xysp</i>] TST [<i>opr16_xysp</i>] TSTA TSTB	(M) - 0 Test Memory for Zero or Minus (A) - 0 Test A for Zero or Minus (B) - 0 Test B for Zero or Minus	EXT IDX IDX1 IDX2 [D,IDX] [IDX2] INH INH	F7 hh ll E7 xb E7 xb ff E7 xb ee ff E7 xb E7 xb ee ff 97 D7	rOP rfP rPO frPP fIfrfP fIPrfP O O	-	-	-	-	Δ	Δ	0	0
TSX	(SP) \Rightarrow X <i>Translates to TFR SP,X</i>	INH	B7 75	P	-	-	-	-	-	-	-	-
TSY	(SP) \Rightarrow Y <i>Translates to TFR SP,Y</i>	INH	B7 76	P	-	-	-	-	-	-	-	-
TXS	(X) \Rightarrow SP <i>Translates to TFR X,SP</i>	INH	B7 57	P	-	-	-	-	-	-	-	-
TYS	(Y) \Rightarrow SP <i>Translates to TFR Y,SP</i>	INH	B7 67	P	-	-	-	-	-	-	-	-
WAI (before interrupt) (when interrupt comes)	(SP) - 2 \Rightarrow SP; RTN _H :RTN _L \Rightarrow M _{(SP):M_(SP+1)} ; (SP) - 2 \Rightarrow SP; (Y _H :Y _L) \Rightarrow M _{(SP):M_(SP+1)} ; (SP) - 2 \Rightarrow SP; (X _H :X _L) \Rightarrow M _{(SP):M_(SP+1)} ; (SP) - 2 \Rightarrow SP; (B:A) \Rightarrow M _{(SP):M_(SP+1)} ; (SP) - 1 \Rightarrow SP; (CCR) \Rightarrow M _(SP) WAIT for interrupt	INH	3E	OSSSfSsF VfPPP	- or - or -	- - - 1	- - - 1	- - - 1	- - - -	- - - -	- - - -	- - - -

Instruction Set Summary (Continued)

Source Form	Operation	Addr. Mode	Machine Coding (hex)	Access Detail	S	X	H	I	N	Z	V	C
WAV (add if interrupt)	$B \sum_{i=1} S_i F_i \Rightarrow Y:D$ $B \sum_{i=1} F_i \Rightarrow X$ <p>Calculate Sum of Products and Sum of Weights for Weighted Average Calculation</p> <p>Initialize B, X, and Y before WAV. B specifies number of elements. X points at first element in S_i list. Y points at first element in F_i list.</p> <p>All S_i and F_i elements are 8-bits.</p> <p>If interrupted, six extra bytes of stack used for intermediate values</p>	Special	18 3C	OfF(fxxxxxxx)O SSS + UUUrr	-	-	?	-	?	Δ	?	?
wavr	see WAV	Special	3C		-	-	?	-	?	Δ	?	?
pseudo-instruction	Resume executing an interrupted WAV instruction (recover intermediate results from stack rather than initializing them to zero)											
XGDY	(D) ⇔ (X) <i>Translates to EXG D, X</i>	INH	B7 C5	P	-	-	-	-	-	-	-	-
XGDY	(D) ⇔ (Y) <i>Translates to EXG D, Y</i>	INH	B7 C6	P	-	-	-	-	-	-	-	-

Table 1. Indexed Addressing Mode Postbyte Encoding (xb)

00 0,X 5b const	10 -16,X 5b const	20 1,+X pre-inc	30 1,X+ post-inc	40 0,Y 5b const	50 -16,Y 5b const	60 1,+Y pre-inc	70 1,Y+ post-inc	80 0,SP 5b const	90 -16,SP 5b const	A0 1,+SP pre-inc	B0 1,SP+ post-inc	C0 0,PC 5b const	D0 -16,PC 5b const	E0 n,X 9b const	F0 n,SP 9b const
01 1,X 5b const	11 -15,X 5b const	21 2,+X pre-inc	31 2,X+ post-inc	41 1,Y 5b const	51 -15,Y 5b const	61 2,+Y pre-inc	71 2,Y+ post-inc	81 1,SP 5b const	91 -15,SP 5b const	A1 2,+SP pre-inc	B1 2,SP+ post-inc	C1 1,PC 5b const	D1 -15,PC 5b const	E1 -n,X 9b const	F1 -n,SP 9b const
02 2,X 5b const	12 -14,X 5b const	22 3,+X pre-inc	32 3,X+ post-inc	42 2,Y 5b const	52 -14,Y 5b const	62 3,+Y pre-inc	72 3,Y+ post-inc	82 2,SP 5b const	92 -14,SP 5b const	A2 3,+SP pre-inc	B2 3,SP+ post-inc	C2 2,PC 5b const	D2 -14,PC 5b const	E2 n,X 16b const	F2 n,SP 16b const
03 3,X 5b const	13 -13,X 5b const	23 4,+X pre-inc	33 4,X+ post-inc	43 3,Y 5b const	53 -13,Y 5b const	63 4,+Y pre-inc	73 4,Y+ post-inc	83 3,SP 5b const	93 -13,SP 5b const	A3 4,+SP pre-inc	B3 4,SP+ post-inc	C3 3,PC 5b const	D3 -13,PC 5b const	E3 [n,X] 16b indir	F3 [n,SP] 16b indir
04 4,X 5b const	14 -12,X 5b const	24 5,+X pre-inc	34 5,X+ post-inc	44 4,Y 5b const	54 -12,Y 5b const	64 5,+Y pre-inc	74 5,Y+ post-inc	84 4,SP 5b const	94 -12,SP 5b const	A4 5,+SP pre-inc	B4 5,SP+ post-inc	C4 4,PC 5b const	D4 -12,PC 5b const	E4 A,X A offset	F4 A,SP A offset
05 5,X 5b const	15 -11,X 5b const	25 6,+X pre-inc	35 6,X+ post-inc	45 5,Y 5b const	55 -11,Y 5b const	65 6,+Y pre-inc	75 6,Y+ post-inc	85 5,SP 5b const	95 -11,SP 5b const	A5 6,+SP pre-inc	B5 6,SP+ post-inc	C5 5,PC 5b const	D5 -11,PC 5b const	E5 B,X B offset	F5 B,SP B offset
06 6,X 5b const	16 -10,X 5b const	26 7,+X pre-inc	36 7,X+ post-inc	46 6,Y 5b const	56 -10,Y 5b const	66 7,+Y pre-inc	76 7,Y+ post-inc	86 6,SP 5b const	96 -10,SP 5b const	A6 7,+SP pre-inc	B6 7,SP+ post-inc	C6 6,PC 5b const	D6 -10,PC 5b const	E6 D,X D offset	F6 D,SP D offset
07 7,X 5b const	17 -9,X 5b const	27 8,+X pre-inc	37 8,X+ post-inc	47 7,Y 5b const	57 -9,Y 5b const	67 8,+Y pre-inc	77 8,Y+ post-inc	87 7,SP 5b const	97 -9,SP 5b const	A7 8,+SP pre-inc	B7 8,SP+ post-inc	C7 7,PC 5b const	D7 -9,PC 5b const	E7 [D,X] D indirect	F7 [D,SP] D indirect
08 8,X 5b const	18 -8,X 5b const	28 8,-X pre-dec	38 8,X- post-dec	48 8,Y 5b const	58 -8,Y 5b const	68 8,-Y pre-dec	78 8,Y- post-dec	88 8,SP 5b const	98 -8,SP 5b const	A8 8,-SP pre-dec	B8 8,SP- post-dec	C8 8,PC 5b const	D8 -8,PC 5b const	E8 n,Y 9b const	F8 n,PC 9b const
09 9,X 5b const	19 -7,X 5b const	29 7,-X pre-dec	39 7,X- post-dec	49 9,Y 5b const	59 -7,Y 5b const	69 7,-Y pre-dec	79 7,Y- post-dec	89 9,SP 5b const	99 -7,SP 5b const	A9 7,-SP pre-dec	B9 7,SP- post-dec	C9 9,PC 5b const	D9 -7,PC 5b const	E9 -n,Y 9b const	F9 -n,PC 9b const
0A 10,X 5b const	1A -6,X 5b const	2A 6,-X pre-dec	3A 6,X- post-dec	4A 10,Y 5b const	5A -6,Y 5b const	6A 6,-Y pre-dec	7A 6,Y- post-dec	8A 10,SP 5b const	9A -6,SP 5b const	AA 6,-SP pre-dec	BA 6,SP- post-dec	CA 10,PC 5b const	DA -6,PC 5b const	EA n,Y 16b const	FA n,PC 16b const
0B 11,X 5b const	1B -5,X 5b const	2B 5,-X pre-dec	3B 5,X- post-dec	4B 11,Y 5b const	5B -5,Y 5b const	6B 5,-Y pre-dec	7B 5,Y- post-dec	8B 11,SP 5b const	9B -5,SP 5b const	AB 5,-SP pre-dec	BB 5,SP- post-dec	CB 11,PC 5b const	DB -5,PC 5b const	EB [n,Y] 16b indir	FB [n,PC] 16b indir
0C 12,X 5b const	1C -4,X 5b const	2C 4,-X pre-dec	3C 4,X- post-dec	4C 12,Y 5b const	5C -4,Y 5b const	6C 4,-Y pre-dec	7C 4,Y- post-dec	8C 12,SP 5b const	9C -4,SP 5b const	AC 4,-SP pre-dec	BC 4,SP- post-dec	CC 12,PC 5b const	DC -4,PC 5b const	EC A,Y A offset	FC A,PC A offset
0D 13,X 5b const	1D -3,X 5b const	2D 3,-X pre-dec	3D 3,X- post-dec	4D 13,Y 5b const	5D -3,Y 5b const	6D 3,-Y pre-dec	7D 3,Y- post-dec	8D 13,SP 5b const	9D -3,SP 5b const	AD 3,-SP pre-dec	BD 3,SP- post-dec	CD 13,PC 5b const	DD -3,PC 5b const	ED B,Y B offset	FD B,PC B offset
0E 14,X 5b const	1E -2,X 5b const	2E 2,-X pre-dec	3E 2,X- post-dec	4E 14,Y 5b const	5E -2,Y 5b const	6E 2,-Y pre-dec	7E 2,Y- post-dec	8E 14,SP 5b const	9E -2,SP 5b const	AE 2,-SP pre-dec	BE 2,SP- post-dec	CE 14,PC 5b const	DE -2,PC 5b const	EE D,Y D offset	FE D,PC D offset
0F 15,X 5b const	1F -1,X 5b const	2F 1,-X pre-dec	3F 1,X- post-dec	4F 15,Y 5b const	5F -1,Y 5b const	6F 1,-Y pre-dec	7F 1,Y- post-dec	8F 15,SP 5b const	9F -1,SP 5b const	AF 1,-SP pre-dec	BF 1,SP- post-dec	CF 15,PC 5b const	DF -1,PC 5b const	EF [D,Y] D indirect	FF [D,PC] D indirect

Key to Table 1

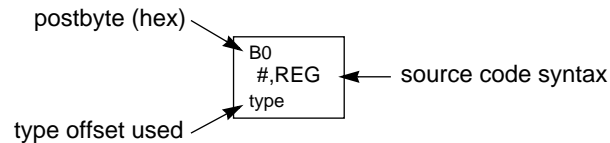


Table 2. Indexed Addressing Mode Summary

Postbyte Code (xb)	Operand Syntax	Comments
rr0nnnnn	,r n,r -n,r	5-bit constant offset n = -16 to +15 rr can specify X, Y, SP, or PC
111rr0zs	n,r -n,r	Constant offset (9- or 16-bit signed) z- 0 = 9-bit with sign in LSB of postbyte (s) 1 = 16-bit if z = s = 1, 16-bit offset indexed-indirect (see below) rr can specify X, Y, SP, or PC
rr1pnnnn	n,-r n,+r n,r- n,r+	Auto pre-decrement /increment or Auto post-decrement/increment; p = pre-(0) or post-(1), n = -8 to -1, +1 to +8 rr can specify X, Y, or SP (PC not a valid choice)
111rr1aa	A,r B,r D,r	Accumulator offset (unsigned 8-bit or 16-bit) aa - 00 = A 01 = B 10 = D (16-bit) 11 = see accumulator D offset indexed-indirect rr can specify X, Y, SP, or PC
111rr011	[n,r]	16-bit offset indexed-indirect rr can specify X, Y, SP, or PC
111rr111	[D,r]	Accumulator D offset indexed-indirect rr can specify X, Y, SP, or PC

Table 3. Transfer and Exchange Postbyte Encoding

TRANSFERS									
↓ LS	MS⇒	0	1	2	3	4	5	6	7
0		A ⇒ A	B ⇒ A	CCR ⇒ A	TMP3 _L ⇒ A	B ⇒ A	X _L ⇒ A	Y _L ⇒ A	SP _L ⇒ A
1		A ⇒ B	B ⇒ B	CCR ⇒ B	TMP3 _L ⇒ B	B ⇒ B	X _L ⇒ B	Y _L ⇒ B	SP _L ⇒ B
2		A ⇒ CCR	B ⇒ CCR	CCR ⇒ CCR	TMP3 _L ⇒ CCR	B ⇒ CCR	X _L ⇒ CCR	Y _L ⇒ CCR	SP _L ⇒ CCR
3		sex:A ⇒ TMP2	sex:B ⇒ TMP2	sex:CCR ⇒ TMP2	TMP3 ⇒ TMP2	D ⇒ TMP2	X ⇒ TMP2	Y ⇒ TMP2	SP ⇒ TMP2
4		sex:A ⇒ D SEX A,D	sex:B ⇒ D SEX B,D	sex:CCR ⇒ D SEX CCR,D	TMP3 ⇒ D	D ⇒ D	X ⇒ D	Y ⇒ D	SP ⇒ D
5		sex:A ⇒ X SEX A,X	sex:B ⇒ X SEX B,X	sex:CCR ⇒ X SEX CCR,X	TMP3 ⇒ X	D ⇒ X	X ⇒ X	Y ⇒ X	SP ⇒ X
6		sex:A ⇒ Y SEX A,Y	sex:B ⇒ Y SEX B,Y	sex:CCR ⇒ Y SEX CCR,Y	TMP3 ⇒ Y	D ⇒ Y	X ⇒ Y	Y ⇒ Y	SP ⇒ Y
7		sex:A ⇒ SP SEX A,SP	sex:B ⇒ SP SEX B,SP	sex:CCR ⇒ SP SEX CCR,SP	TMP3 ⇒ SP	D ⇒ SP	X ⇒ SP	Y ⇒ SP	SP ⇒ SP
EXCHANGES									
↓ LS	MS⇒	8	9	A	B	C	D	E	F
0		A ⇔ A	B ⇔ A	CCR ⇔ A	TMP3 _L ⇔ A \$00:A ⇒ TMP3	B ⇒ A A ⇒ B	X _L ⇔ A \$00:A ⇒ X	Y _L ⇔ A \$00:A ⇒ Y	SP _L ⇔ A \$00:A ⇒ SP
1		A ⇔ B	B ⇔ B	CCR ⇔ B	TMP3 _L ⇔ B \$FF:B ⇒ TMP3	B ⇒ B \$FF ⇒ A	X _L ⇔ B \$FF:B ⇒ X	Y _L ⇔ B \$FF:B ⇒ Y	SP _L ⇔ B \$FF:B ⇒ SP
2		A ⇔ CCR	B ⇔ CCR	CCR ⇔ CCR	TMP3 _L ⇔ CCR \$FF:CCR ⇒ TMP3	B ⇒ CCR \$FF:CCR ⇒ D	X _L ⇔ CCR \$FF:CCR ⇒ X	Y _L ⇔ CCR \$FF:CCR ⇒ Y	SP _L ⇔ CCR \$FF:CCR ⇒ SP
3		\$00:A ⇒ TMP2 TMP2 _L ⇒ A	\$00:B ⇒ TMP2 TMP2 _L ⇒ B	\$00:CCR ⇒ TMP2 TMP2 _L ⇒ CCR	TMP3 ⇔ TMP2	D ⇔ TMP2	X ⇔ TMP2	Y ⇔ TMP2	SP ⇔ TMP2
4		\$00:A ⇒ D	\$00:B ⇒ D	\$00:CCR ⇒ D B ⇒ CCR	TMP3 ⇔ D	D ⇔ D	X ⇔ D	Y ⇔ D	SP ⇔ D
5		\$00:A ⇒ X X _L ⇒ A	\$00:B ⇒ X X _L ⇒ B	\$00:CCR ⇒ X X _L ⇒ CCR	TMP3 ⇔ X	D ⇔ X	X ⇔ X	Y ⇔ X	SP ⇔ X
6		\$00:A ⇒ Y Y _L ⇒ A	\$00:B ⇒ Y Y _L ⇒ B	\$00:CCR ⇒ Y Y _L ⇒ CCR	TMP3 ⇔ Y	D ⇔ Y	X ⇔ Y	Y ⇔ Y	SP ⇔ Y
7		\$00:A ⇒ SP SP _L ⇒ A	\$00:B ⇒ SP SP _L ⇒ B	\$00:CCR ⇒ SP SP _L ⇒ CCR	TMP3 ⇔ SP	D ⇔ SP	X ⇔ SP	Y ⇔ SP	SP ⇔ SP

TMP2 and TMP3 registers are for factory use only.

Table 4. Loop Primitive Postbyte Encoding (Ib)

00	A	10	A	20	A	30	A	40	A	50	A	60	A	70	A	80	A	90	A	A0	A	B0	A
DBEQ		DBEQ		DBNE		DBNE		TBEQ		TBEQ		TBNE		TBNE		IBEQ		IBEQ		IBNE		IBNE	
(+)		(-)		(+)		(-)		(+)		(-)		(+)		(-)		(+)		(-)		(+)		(-)	
01	B	11	B	21	B	31	B	41	B	51	B	61	B	71	B	81	B	91	B	A1	B	B1	B
DBEQ		DBEQ		DBNE		DBNE		TBEQ		TBEQ		TBNE		TBNE		IBEQ		IBEQ		IBNE		IBNE	
(+)		(-)		(+)		(-)		(+)		(-)		(+)		(-)		(+)		(-)		(+)		(-)	
02		12		22		32		42		52		62		72		82		92		A2		B2	
—		—		—		—		—		—		—		—		—		—		—		—	
03		13		23		33		43		53		63		73		83		93		A3		B3	
—		—		—		—		—		—		—		—		—		—		—		—	
04	D	14	D	24	D	34	D	44	D	54	D	64	D	74	D	84	D	94	D	A4	D	B4	D
DBEQ		DBEQ		DBNE		DBNE		TBEQ		TBEQ		TBNE		TBNE		IBEQ		IBEQ		IBNE		IBNE	
(+)		(-)		(+)		(-)		(+)		(-)		(+)		(-)		(+)		(-)		(+)		(-)	
05	X	15	X	25	X	35	X	45	X	55	X	65	X	75	X	85	X	95	X	A5	X	B5	X
DBEQ		DBEQ		DBNE		DBNE		TBEQ		TBEQ		TBNE		TBNE		IBEQ		IBEQ		IBNE		IBNE	
(+)		(-)		(+)		(-)		(+)		(-)		(+)		(-)		(+)		(-)		(+)		(-)	
06	Y	16	Y	26	Y	36	Y	46	Y	56	Y	66	Y	76	Y	86	Y	96	Y	A6	Y	B6	Y
DBEQ		DBEQ		DBNE		DBNE		TBEQ		TBEQ		TBNE		TBNE		IBEQ		IBEQ		IBNE		IBNE	
(+)		(-)		(+)		(-)		(+)		(-)		(+)		(-)		(+)		(-)		(+)		(-)	
07	SP	17	SP	27	SP	37	SP	47	SP	57	SP	67	SP	77	SP	87	SP	97	SP	A7	SP	B7	SP
DBEQ		DBEQ		DBNE		DBNE		TBEQ		TBEQ		TBNE		TBNE		IBEQ		IBEQ		IBNE		IBNE	
(+)		(-)		(+)		(-)		(+)		(-)		(+)		(-)		(+)		(-)		(+)		(-)	

Key to Table 4

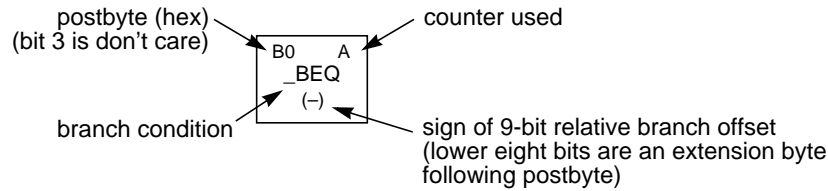


Table 5. Branch/Complementary Branch

Branch				Complementary Branch			
Test	Mnemonic	Opcode	Boolean	Test	Mnemonic	Opcode	Comment
r>m	BGT	2E	$Z + (N \oplus V) = 0$	r≤m	BLE	2F	Signed
r≥m	BGE	2C	$N \oplus V = 0$	r<m	BLT	2D	Signed
r=m	BEQ	27	$Z = 1$	r≠m	BNE	26	Signed
r≤m	BLE	2F	$Z + (N \oplus V) = 1$	r>m	BGT	2E	Signed
r<m	BLT	2D	$N \oplus V = 1$	r≥m	BGE	2C	Signed
r>m	BHI	22	$C + Z = 0$	r≤m	BLS	23	Unsigned
r≥m	BHS/BCC	24	$C = 0$	r<m	BLO/BCS	25	Unsigned
r=m	BEQ	27	$Z = 1$	r≠m	BNE	26	Unsigned
r≤m	BLS	23	$C + Z = 1$	r>m	BHI	22	Unsigned
r<m	BLO/BCS	25	$C = 1$	r≥m	BHS/BCC	24	Unsigned
Carry	BCS	25	$C = 1$	No Carry	BCC	24	Simple
Negative	BMI	2B	$N = 1$	Plus	BPL	2A	Simple
Overflow	BVS	29	$V = 1$	No Overflow	BVC	28	Simple
r=0	BEQ	27	$Z = 1$	r≠0	BNE	26	Simple
Always	BRA	20	—	Never	BRN	21	Unconditional

For 16-bit offset long branches precede opcode with a \$18 page prebyte.

Memory Expansion

Some M68HC12 derivatives support >4 megabytes of program memory.

Memory precedence

— Highest —

On-chip registers (usually \$0000 or \$1000)

BDM ROM (only when BDM active)

On-chip RAM

On-chip EEPROM

On-chip program memory (FLASH or ROM)

Expansion windows (on MCUs with expanded memory)

Other external memory

— Lowest —

CPU sees 64 Kbytes of address space (CPU_ADDR [15:0])

PPAGE 8-bit register to select 1 of 256 —16 Kbyte program pages

DPAGE 8-bit register to select 1 of 256 — 4 Kbyte data pages

EPAGE 8-bit register to select 1 of 256 — 1 Kbyte extra pages

Extended address is 22 bits (EXT_ADDR [21:0])

Program expansion window works with CALL and RTC instructions to simplify program access to extended memory space. Data and extra expansion windows (when present) use traditional banked expansion memory techniques.

Program window

If CPU_ADDR [15:0] = \$8000–BFFF and PWEN = 1

Then EXT_ADDR [21:0] = PPAGE [7:0]:CPU_ADDR [13:0]

Program window works with CALL/RTC to automate bank switching.

256 pages (banks) of 16 Kbytes each = 4 M.

Data window

If CPU_ADDR [15:0] = \$7000–7FFF and DWEN = 1

Then EXT_ADDR [21:0] = 1:1:DPAGE [7:0]:CPU_ADDR [11:0]

User program controls DPAGE value

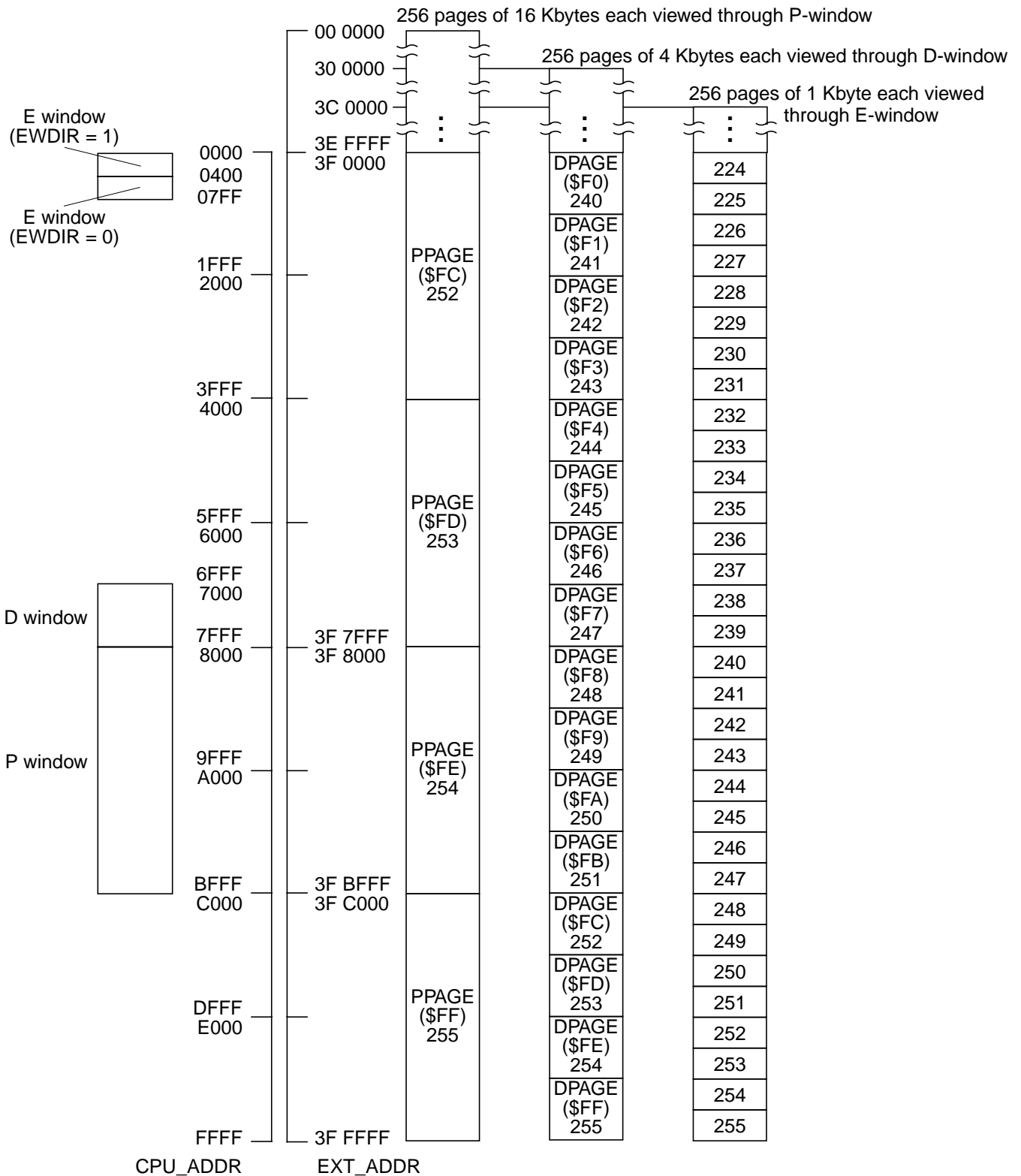


Table 6. CPU12 Opcode Map (Sheet 1 of 2)

00	*5 BGND IH 1	10	1 ANDCC IM 2	20	3 BRA RL 2	30	3 PULX IH 1	40	1 NEGA IH 1	50	1 NEGB IH 1	60	3-6 NEG ID 2-4	70	4 NEG EX 3	80	1 SUBA IM 2	90	3 SUBA DI 2	A0	3-6 SUBA ID 2-4	B0	3 SUBA EX 3	C0	1 SUBB IM 2	D0	3 SUBB DI 2	E0	3-6 SUBB ID 2-4	F0	3 SUBB EX 3
01	5 MEM IH 1	11	11 EDIV IH 1	21	1 BRN RL 2	31	3 PULY IH 1	41	1 COMA IH 1	51	1 COMB IH 1	61	3-6 COM ID 2-4	71	4 COM EX 3	81	1 CMPA IM 2	91	3 CMPA DI 2	A1	3-6 CMPA ID 2-4	B1	3 CMPA EX 3	C1	1 CMPB IM 2	D1	3 CMPB DI 2	E1	3-6 CMPB ID 2-4	F1	3 CMPB EX 3
02	1 INY IH 1	12	3 MUL IH 1	22	3/1 BHI RL 2	32	3 PULA IH 1	42	1 INCA IH 1	52	1 INCB IH 1	62	3-6 INC ID 2-4	72	4 INC EX 3	82	1 SBCA IM 2	92	3 SBCA DI 2	A2	3-6 SBCA ID 2-4	B2	3 SBCA EX 3	C2	1 SBCB IM 2	D2	3 SBCB DI 2	E2	3-6 SBCB ID 2-4	F2	3 SBCB EX 3
03	1 DEY IH 1	13	3 EMUL IH 1	23	3/1 BLS RL 2	33	3 PULB IH 1	43	1 DECA IH 1	53	1 DECB IH 1	63	3-6 DEC ID 2-4	73	4 DEC EX 3	83	2 SUBD IM 3	93	3 SUBD DI 2	A3	3-6 SUBD ID 2-4	B3	3 SUBD EX 3	C3	2 ADDD IM 3	D3	3 ADDD DI 2	E3	3-6 ADDD ID 2-4	F3	3 ADDD EX 3
04	3 loop [†] RL 3	14	1 ORCC IM 2	24	3/1 BCC RL 2	34	2 PSHX IH 1	44	1 LSRA IH 1	54	1 LSRB IH 1	64	3-6 LSR ID 2-4	74	4 LSR EX 3	84	1 ANDA IM 2	94	3 ANDA DI 2	A4	3-6 ANDA ID 2-4	B4	3 ANDA EX 3	C4	1 ANDB IM 2	D4	3 ANDB DI 2	E4	3-6 ANDB ID 2-4	F4	3 ANDB EX 3
05	3-6 JMP ID 2-4	15	4-7 JSR ID 2-4	25	3/1 BCS RL 2	35	2 PSHY IH 1	45	1 ROLA IH 1	55	1 ROLB IH 1	65	3-6 ROL ID 2-4	75	4 ROL EX 3	85	1 BITA IM 2	95	3 BITA DI 2	A5	3-6 BITA ID 2-4	B5	3 BITA EX 3	C5	1 BITB IM 2	D5	3 BITB DI 2	E5	3-6 BITB ID 2-4	F5	3 BITB EX 3
06	3 JMP EX 3	16	4 JSR EX 3	26	3/1 BNE RL 2	36	2 PSHA IH 1	46	1 RORA IH 1	56	1 RORB IH 1	66	3-6 ROR ID 2-4	76	4 ROR EX 3	86	1 LDAA IM 2	96	3 LDAA DI 2	A6	3-6 LDAA ID 2-4	B6	3 LDAA EX 3	C6	1 LDAB IM 2	D6	3 LDAB DI 2	E6	3-6 LDAB ID 2-4	F6	3 LDAB EX 3
07	4 BSR RL 2	17	4 JSR DI 2	27	3/1 BEQ RL 2	37	2 PSHB IH 1	47	1 ASRA IH 1	57	1 ASRB IH 1	67	3-6 ASR ID 2-4	77	4 ASR EX 3	87	1 CLRA IH 1	97	1 TSTA IH 1	A7	1 NOP IH 1	B7	1 TFR/EXG IH 2	C7	1 CLRB IH 1	D7	1 TSTB IH 1	E7	3-6 TST ID 2-4	F7	3 TST EX 3
08	1 INX IH 1	18	- page 2 -	28	3/1 BVC RL 2	38	3 PULC IH 1	48	1 ASLA IH 1	58	1 ASLB IH 1	68	3-6 ASL ID 2-4	78	4 ASL EX 3	88	1 EORA IM 2	98	3 EORA DI 2	A8	3-6 EORA ID 2-4	B8	3 EORA EX 3	C8	1 EORB IM 2	D8	3 EORB DI 2	E8	3-6 EORB ID 2-4	F8	3 EORB EX 3
09	1 DEX IH 1	19	2 LEAY ID 2-4	29	3/1 BVS RL 2	39	2 PSHC IH 1	49	1 LSRD IH 1	59	1 ASLD IH 1	69	2-5 CLR ID 2-4	79	3 CLR EX 3	89	1 ADCA IM 2	99	3 ADCA DI 2	A9	3-6 ADCA ID 2-4	B9	3 ADCA EX 3	C9	1 ADCB IM 2	D9	3 ADCB DI 2	E9	3-6 ADCB ID 2-4	F9	3 ADCB EX 3
0A	6 RTC IH 1	1A	2 LEAX ID 2-4	2A	3/1 BPL RL 2	3A	3 PULD IH 1	4A	8 CALL EX 4	5A	2 STAA DI 2	6A	2-5 STAA ID 2-4	7A	3 STAA EX 3	8A	1 ORAA IM 2	9A	3 ORAA DI 2	AA	3-6 ORAA ID 2-4	BA	3 ORAA EX 3	CA	1 ORAB IM 2	DA	3 ORAB DI 2	EA	3-6 ORAB ID 2-4	FA	3 ORAB EX 3
0B	8 RTI IH 1	1B	2 LEAS ID 2-4	2B	3/1 BMI RL 2	3B	2 PSHD IH 1	4B	8-10 CALL ID 2-5	5B	2 STAB DI 2	6B	2-5 STAB ID 2-4	7B	3 STAB EX 3	8B	1 ADDA IM 2	9B	3 ADDA DI 2	AB	3-6 ADDA ID 2-4	BB	3 ADDA EX 3	CB	1 ADDB IM 2	DB	3 ADDB DI 2	EB	3-6 ADDB ID 2-4	FB	3 ADDB EX 3
0C	4-6 BSET ID 3-5	1C	4 BSET EX 4	2C	3/1 BGE RL 2	3C	*+9 wavr SP 1	4C	4 BSET DI 3	5C	2 STD DI 2	6C	2-5 STD ID 2-4	7C	3 STD EX 3	8C	2 CPD IM 3	9C	3 CPD DI 2	AC	3-6 CPD ID 2-4	BC	3 CPD EX 3	CC	2 LDD IM 3	DC	3 LDD DI 2	EC	3-6 LDD ID 2-4	FC	3 LDD EX 3
0D	4-6 BCLR ID 3-5	1D	4 BCLR EX 4	2D	3/1 BLT RL 2	3D	5 RTS IH 1	4D	4 BCLR DI 3	5D	2 STY DI 2	6D	2-5 STY ID 2-4	7D	3 STY EX 3	8D	2 CPY IM 3	9D	3 CPY DI 2	AD	3-6 CPY ID 2-4	BD	3 CPY EX 3	CD	2 LDY IM 3	DD	3 LDY DI 2	ED	3-6 LDY ID 2-4	FD	3 LDY EX 3
0E	4-8 BRSET ID 4-6	1E	5 BRSET EX 5	2E	3/1 BGT RL 2	3E	*8 WAI IH 1	4E	4 BRSET DI 4	5E	2 STX DI 2	6E	2-5 STX ID 2-4	7E	3 STX EX 3	8E	2 CPX IM 3	9E	3 CPX DI 2	AE	3-6 CPX ID 2-4	BE	3 CPX EX 3	CE	2 LDX IM 3	DE	3 LDX DI 2	EE	3-6 LDX ID 2-4	FE	3 LDX EX 3
0F	4-8 BRCLR ID 4-6	1F	5 BRCLR EX 5	2F	3/1 BLE RL 2	3F	9 SWI IH 1	4F	4 BRCLR DI 4	5F	2 STS DI 2	6F	2-5 STS ID 2-4	7F	3 STS EX 3	8F	2 CPS IM 3	9F	3 CPS DI 2	AF	3-6 CPS ID 2-4	BF	3 CPS EX 3	CF	2 LDS IM 3	DF	3 LDS DI 2	EF	3-6 LDS ID 2-4	FF	3 LDS EX 3

Table 6. CPU12 Opcode Map (Sheet 2 of 2)

00	4	10	12	20	4	30	10	40	10	50	10	60	10	70	10	80	10	90	10	A0	10	B0	10	C0	10	D0	10	E0	10	F0	10
MOVW		IDIV		LBRA		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP	
IM-ID	5	IH	2	RL	4	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2
01	5	11	12	21	3	31	10	41	10	51	10	61	10	71	10	81	10	91	10	A1	10	B1	10	C1	10	D1	10	E1	10	F1	10
MOVW		FDIV		LBRN		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP	
EX-ID	5	IH	2	RL	4	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2
02	5	12	13	22	4/3	32	10	42	10	52	10	62	10	72	10	82	10	92	10	A2	10	B2	10	C2	10	D2	10	E2	10	F2	10
MOVW		EMACS		LBHI		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP	
ID-ID	4	SP	4	RL	4	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2
03	5	13	3	23	4/3	33	10	43	10	53	10	63	10	73	10	83	10	93	10	A3	10	B3	10	C3	10	D3	10	E3	10	F3	10
MOVW		EMULS		LBLS		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP	
IM-EX	6	IH	2	RL	4	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2
04	6	14	12	24	4/3	34	10	44	10	54	10	64	10	74	10	84	10	94	10	A4	10	B4	10	C4	10	D4	10	E4	10	F4	10
MOVW		EDIVS		LBCC		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP	
EX-EX	6	IH	2	RL	4	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2
05	5	15	12	25	4/3	35	10	45	10	55	10	65	10	75	10	85	10	95	10	A5	10	B5	10	C5	10	D5	10	E5	10	F5	10
MOVW		IDIVS		LBSC		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP	
ID-EX	5	IH	2	RL	4	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2
06	2	16	2	26	4/3	36	10	46	10	56	10	66	10	76	10	86	10	96	10	A6	10	B6	10	C6	10	D6	10	E6	10	F6	10
ABA		SBA		LBNE		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP	
IH	2	IH	2	RL	4	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2
07	3	17	2	27	4/3	37	10	47	10	57	10	67	10	77	10	87	10	97	10	A7	10	B7	10	C7	10	D7	10	E7	10	F7	10
DAA		CBA		LBEQ		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP	
IH	2	IH	2	RL	4	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2
08	4	18	4-7	28	4/3	38	10	48	10	58	10	68	10	78	10	88	10	98	10	A8	10	B8	10	C8	10	D8	10	E8	10	F8	10
MOVW		MAXA		LBVC		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP	
IM-ID	4	ID	3-5	RL	4	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2
09	5	19	4-7	29	4/3	39	10	49	10	59	10	69	10	79	10	89	10	99	10	A9	10	B9	10	C9	10	D9	10	E9	10	F9	10
MOVW		MINA		LBVS		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP	
EX-ID	5	ID	3-5	RL	4	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2
0A	5	1A	4-7	2A	4/3	3A	*3n	4A	10	5A	10	6A	10	7A	10	8A	10	9A	10	AA	10	BA	10	CA	10	DA	10	EA	10	FA	10
MOVW		EMAXD		LBPL		REV		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP	
ID-ID	4	ID	3-5	RL	4	SP	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2
0B	4	1B	4-7	2B	4/3	3B	*3n	4B	10	5B	10	6B	10	7B	10	8B	10	9B	10	AB	10	BB	10	CB	10	DB	10	EB	10	FB	10
MOVW		EMIND		LBMI		REVV		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP	
IM-EX	5	ID	3-5	RL	4	SP	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2
0C	6	1C	4-7	2C	4/3	3C	*8B	4C	10	5C	10	6C	10	7C	10	8C	10	9C	10	AC	10	BC	10	CC	10	DC	10	EC	10	FC	10
MOVW		MAXM		LBGE		WAV		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP	
EX-EX	6	ID	3-5	RL	4	SP	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2
0D	5	1D	4-7	2D	4/3	3D	8	4D	10	5D	10	6D	10	7D	10	8D	10	9D	10	AD	10	BD	10	CD	10	DD	10	ED	10	FD	10
MOVW		MINM		LBTL		TBL		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP	
ID-EX	5	ID	3-5	RL	4	ID	3	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2
0E	2	1E	4-7	2E	4/3	3E	*9+5	4E	10	5E	10	6E	10	7E	10	8E	10	9E	10	AE	10	BE	10	CE	10	DE	10	EE	10	FE	10
TAB		EMAXM		LBGT		STOP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP	
IH	2	ID	3-5	RL	4	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2
0F	2	1F	4-7	2F	4/3	3F	10	4F	10	5F	10	6F	10	7F	10	8F	10	9F	10	AF	10	BF	10	CF	10	DF	10	EF	10	FF	10
TBA		EMINM		LBLE		ETBL		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP		TRAP	
IH	2	ID	3-5	RL	4	ID	3	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2	IH	2

* Refer to instruction summary for more information.

‡ The opcode \$04 corresponds to one of the loop primitive instructions DBEQ, DBNE, IBEQ, IBNE, TBEQ, or TBNE.

Table 7. Hexadecimal to ASCII Conversion

Hex	ASCII	Hex	ASCII	Hex	ASCII	Hex	ASCII
\$00	NUL	\$20	SP space	\$40	@	\$60	`grave
\$01	SOH	\$21	!	\$41	A	\$61	a
\$02	STX	\$22	"quote	\$42	B	\$62	b
\$03	ETX	\$23	#	\$43	C	\$63	c
\$04	EOT	\$24	\$	\$44	D	\$64	d
\$05	ENQ	\$25	%	\$45	E	\$65	e
\$06	ACK	\$26	&	\$46	F	\$66	f
\$07	BEL <i>beep</i>	\$27	'apost.	\$47	G	\$67	g
\$08	BS <i>back sp</i>	\$28	(\$48	H	\$68	h
\$09	HT <i>tab</i>	\$29)	\$49	I	\$69	i
\$0A	LF <i>linefeed</i>	\$2A	*	\$4A	J	\$6A	j
\$0B	VT	\$2B	+	\$4B	K	\$6B	k
\$0C	FF	\$2C	, comma	\$4C	L	\$6C	l
\$0D	CR <i>return</i>	\$2D	- dash	\$4D	M	\$6D	m
\$0E	SO	\$2E	. period	\$4E	N	\$6E	n
\$0F	SI	\$2F	/	\$4F	O	\$6F	o
\$10	DLE	\$30	0	\$50	P	\$70	p
\$11	DC1	\$31	1	\$51	Q	\$71	q
\$12	DC2	\$32	2	\$52	R	\$72	r
\$13	DC3	\$33	3	\$53	S	\$73	s
\$14	DC4	\$34	4	\$54	T	\$74	t
\$15	NAK	\$35	5	\$55	U	\$75	u
\$16	SYN	\$36	6	\$56	V	\$76	v
\$17	ETB	\$37	7	\$57	W	\$77	w
\$18	CAN	\$38	8	\$58	X	\$78	x
\$19	EM	\$39	9	\$59	Y	\$79	y
\$1A	SUB	\$3A	:	\$5A	Z	\$7A	z
\$1B	ESCAPE	\$3B	;	\$5B	[\$7B	{
\$1C	FS	\$3C	<	\$5C	\	\$7C	
\$1D	GS	\$3D	=	\$5D]	\$7D	}
\$1E	RS	\$3E	>	\$5E	^	\$7E	~
\$1F	US	\$3F	?	\$5F	_ <i>under</i>	\$7F	DEL <i>delete</i>

Hexadecimal to Decimal Conversion


To convert a hexadecimal number (up to four hexadecimal digits) to decimal, look up the decimal equivalent of each hexadecimal digit in [Table 8](#). The decimal equivalent of the original hexadecimal number is the sum of the weights found in the table for all hexadecimal digits.

Table 8. Hexadecimal to/from Decimal Conversion

15		Bit		8		7		Bit		0					
15		12		11		8		7		4		3		0	
4th Hex Digit				3rd Hex Digit				2nd Hex Digit				1st Hex Digit			
Hex	Decimal	Hex	Decimal	Hex	Decimal	Hex	Decimal	Hex	Decimal	Hex	Decimal	Hex	Decimal		
0	0	0	0	0	0	0	0	0	0	0	0	0	0		
1	4,096	1	256	1	16	1	1	1	1	1	1	1	1		
2	8,192	2	512	2	32	2	2	2	2	2	2	2	2		
3	12,288	3	768	3	48	3	3	3	3	3	3	3	3		
4	16,384	4	1,024	4	64	4	4	4	4	4	4	4	4		
5	20,480	5	1,280	5	80	5	5	5	5	5	5	5	5		
6	24,576	6	1,536	6	96	6	6	6	6	6	6	6	6		
7	28,672	7	1,792	7	112	7	7	7	7	7	7	7	7		
8	32,768	8	2,048	8	128	8	8	8	8	8	8	8	8		
9	36,864	9	2,304	9	144	9	9	9	9	9	9	9	9		
A	40,960	A	2,560	A	160	A	A	A	A	A	A	A	10		
B	45,056	B	2,816	B	176	B	B	B	B	B	B	B	11		
C	49,152	C	3,072	C	192	C	C	C	C	C	C	C	12		
D	53,248	D	3,328	D	208	D	D	D	D	D	D	D	13		
E	57,344	E	3,484	E	224	E	E	E	E	E	E	E	14		
F	61,440	F	3,840	F	240	F	F	F	F	F	F	F	15		

Decimal to Hexadecimal Conversion

To convert a decimal number (up to $65,535_{10}$) to hexadecimal, find the largest decimal number in [Table 8](#) that is less than or equal to the number you are converting. The corresponding hexadecimal digit is the most significant hexadecimal digit of the result. Subtract the decimal number found from the original decimal number to get the *remaining decimal value*. Repeat the procedure using the remaining decimal value for each subsequent hexadecimal digit.

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