MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

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TIM08RMAD/AD

TIM08

Addendum to
TIM08
Timer Interface Module
Reference Manual

This addendum provides corrections to the *TIM08 Timer Interface Module Reference Manual* (Motorola document number TIM08RM/AD).

Page 1-16, correct **Figure 1-8. Buffered PWM Simplified Block Diagram** as follows:

From:

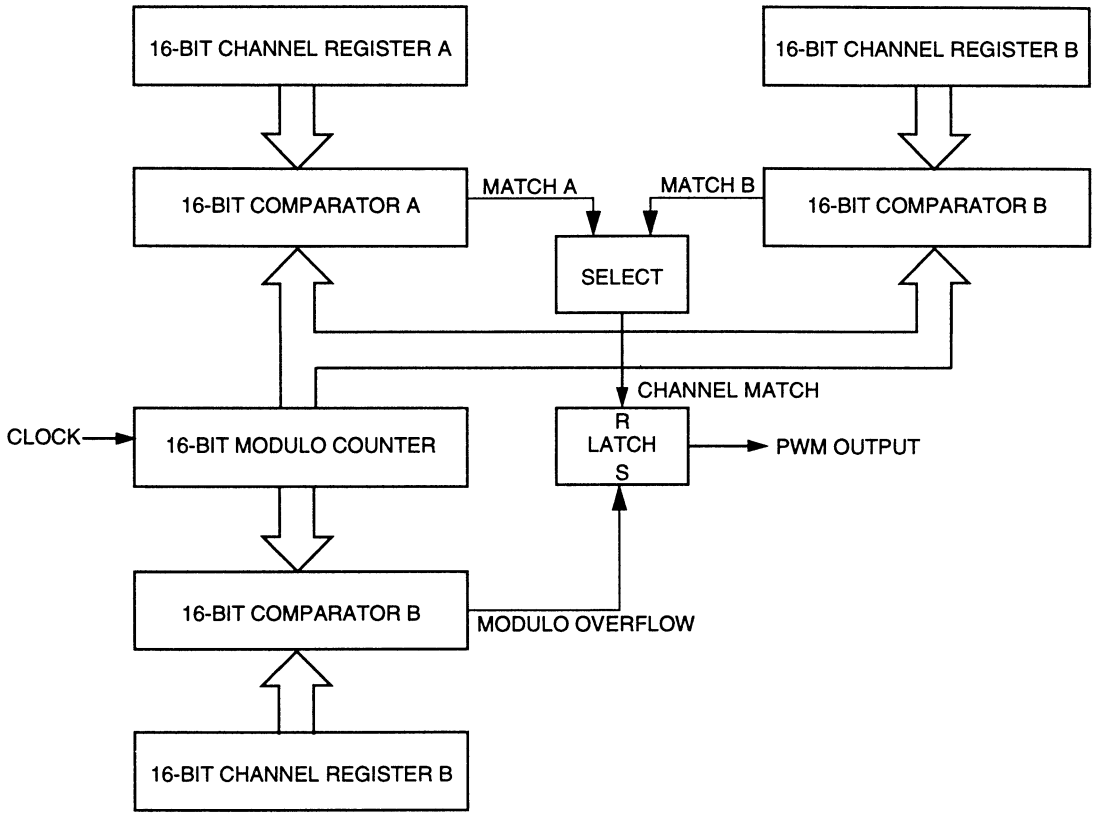


Figure 1-8. Buffered PWM Simplified Block Diagram

To:

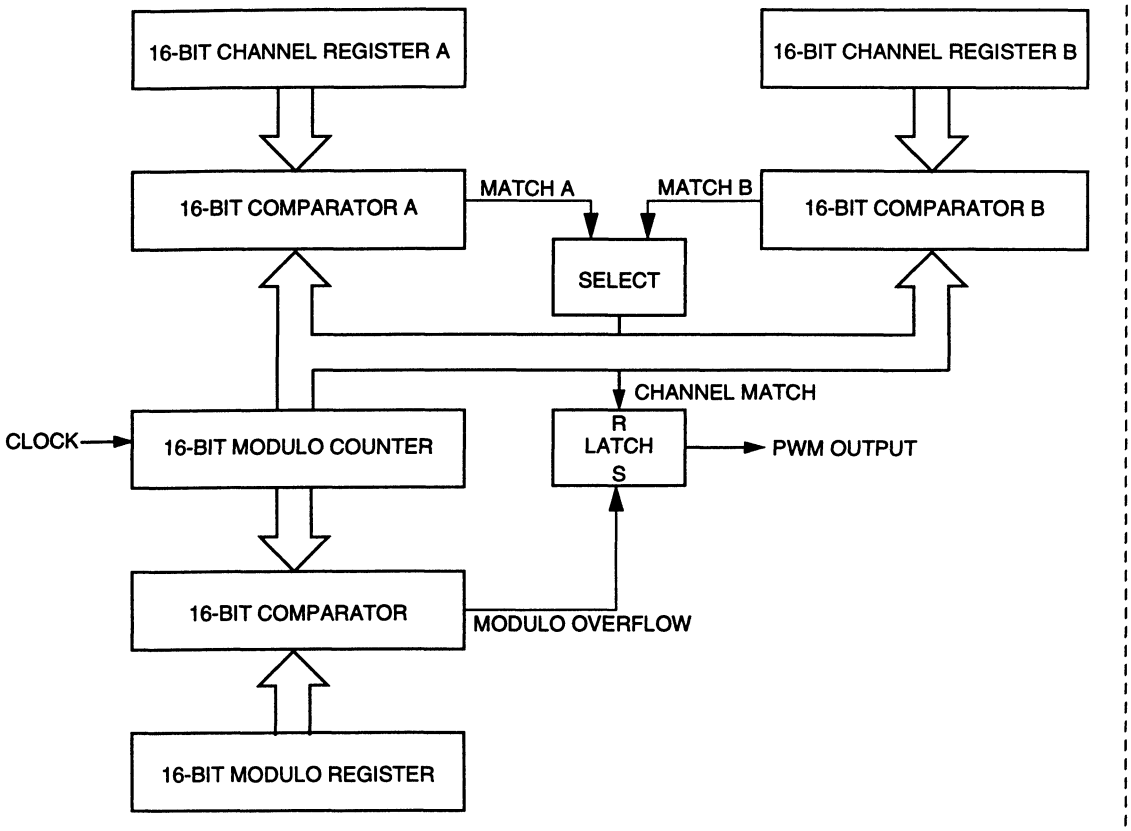


Figure 1-8. Buffered PWM Simplified Block Diagram

Cut here

(Cut out the figure labeled "To" and paste over existing figure.)

Page 2-4, correct the text as follows:

From:

If this pin is not used as a clock input, it can be used as a general purpose I/O pin. Refer to **Table 3-1. Prescaler Selection** for information on selecting the function of this pin.

To:

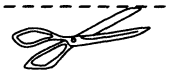
If this pin is not used as a clock input, it can be used as a general-purpose I/O pin. Refer to **Table 3-1. Prescaler Selection** for information on selecting the function of this pin. The minimum TCLK pulse width, $TCLK_{LMIN}$ or $TCLK_{HMIN}$, is:

$$\frac{1}{\text{bus frequency}} + t_{SU}$$

The maximum TCLK frequency is:

$$\frac{\text{bus frequency}}{2}$$

PTE3/TCLK is available as a general-purpose I/O pin when not used as the TIM clock input. When the PTE3/TCLK pin is the TIM clock input, it is an input regardless of the state of the DDRE3 bit in data direction register E.



(Cut out the text labeled "To" and paste over existing text.)

Page 3-2, correct the existing text with the following:

From:

TCLK is an external clock input. TCLK can be used as the clock source for the 16-bit counter instead of the bus clock or its derivative. Any pulse longer than one bus clock is guaranteed to pass. **Figure 3-2** shows the timing of TCLK and its synchronization to the bus clock. The value of TCLK at the rising edge of IT12 is passed to the prescaler at the falling edge of IT12. The maximum frequency is $f_{OP} \div 2$, and the minimum pulse width is t_{CYC}. If this pin is not used as a clock input, it can be used as a general-purpose I/O pin.

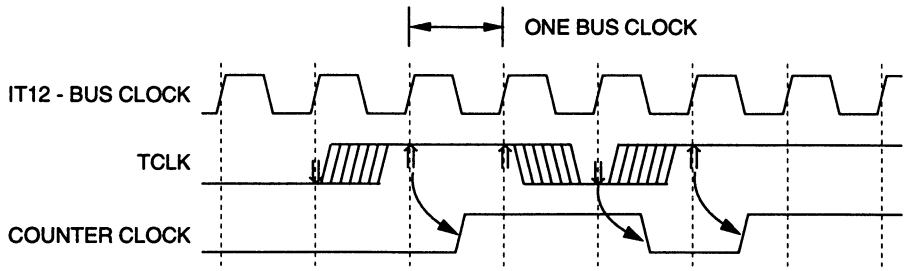


Figure 3-2. TCLK Timing

To:

TCLK is an external clock input. TCLK can be used as the clock source for the 16-bit counter instead of the bus clock or its derivative. **Figure 3-2** shows the timing of TCLK and its synchronization to the bus clock.

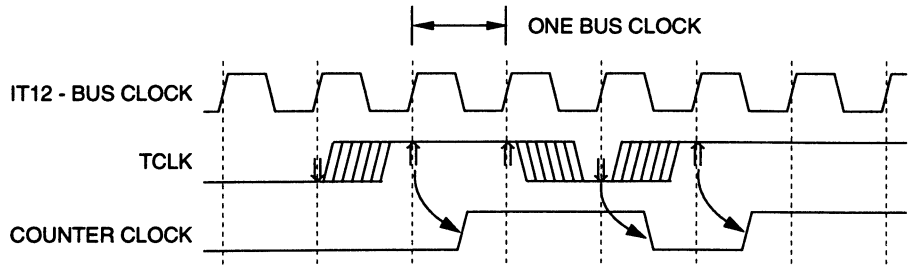


Figure 3-2. TCLK Timing

where

$$t_{CYC} = \frac{1}{bus\ frequency} + t_{SU}$$

Cut here

(Cut out the text labeled "To" and paste over existing text.)

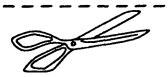
Page 5-1, correct the text as follows:

From:

Each TIM input capture pin TCH0 - TCH3, when used as an input capture function, has a 16-bit register latch (TCHxH/L), input edge-detection/selection logic, and interrupt generation logic.

To:

Each TIM input capture pin TCH0–TCH3, when used as an input capture function, has a 16-bit register latch (TCHxH/L), input edge-detection/selection logic, and interrupt synchronization/generation logic.



(Cut out the text labeled "To" and paste over existing text.)

Page 5-7, correct **Table 5-1. Input Capture Mode and Edge Selection** as follows:

From:

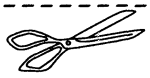
Table 5-1. Input Capture Mode and Edge Selection

MSxB: MSxA	ELSxB: ELSxA	Mode	Configuration
00	00	Input Capture	TCHx Pin under port control; set initial output level high.
00	01	Input Capture	Capture on Rising Edge Only
00	10	Input Capture	Capture on Falling Edge Only
00	11	Input Capture	Capture on Rising or Falling Edge

To:

Table 5-1. Input Capture Mode and Edge Selection

MSxB: MSxA	ELSxB: ELSxA	Mode	Configuration
00	00	Output Preset	TCHx Pin under Port Control; Not Used in IC Mode
00	01	Input Capture	Capture on Rising Edge Only
00	10	Input Capture	Capture on Falling Edge Only
00	11	Input Capture	Capture on Rising or Falling Edge



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(Cut out the table labeled "To" and paste over existing table.)

Page 7-1, correct the text as follows:

From:

7.1 Wait Mode

WAIT mode is entered by executing the WAIT instruction in the CPU08. WAIT mode is a low-power mode in which the CPU clocks are stopped, and the bus clocks to the TIM continue to run. The TIM functions are active and all TIM counters and prescalers continue counting during WAIT mode. A timer interrupt may cause the CPU08 to exit WAIT mode if interrupts are not masked.

All TIM registers retain their states in WAIT mode.

To:

7.1 Wait Mode

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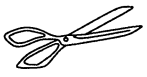
All TIM registers retain their states in WAIT mode.

If a DMA is available, it can service a TIM interrupt without causing the CPU to have to exit WAIT mode. This can be used to fill a buffer with input capture data or to transmit a buffer full of OC/PWM data. A DMA interrupt can be used to exit the CPU from WAIT and then to use or refill the buffer data as needed. This feature allows the MCU to conserve power, avoid long interrupt service latency, and potentially reduce code size due to fewer necessary interrupt service routines.



(Cut out the text labeled "To" and paste over existing text.)

Page 8-11, correct the text as follows:

From:

```
* Variables in RAM
        org $0050  ;start of RAM
track   fcb 0
```

To:

```
* Variables in RAM
        org $0050  ;start of RAM
track   rmb 1
```

Cut here

(Cut out the text labeled "To" and paste over existing text.)

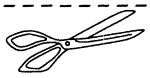
Page 8-23, correct the text as follows:

From:

```
* Variables in RAM
        org $0050       ;start of RAM
edge1h  fcb 0           ;high byte of first edge count
edge1l  fcb 0           ;low byte of first edge count
edge2h  fcb 0           ;high byte of second edge count
edge2l  fcb 0           ;low byte of second edge count
period  fcb 0           ;timer value of feedback signal
pwidth  fcb 0           ;pulsewidth for motor - must be initialized
desper  fcb 0           ;desired feedback period - must be initialized
deltnew fcb 0           ;current error value
deltold fcb 0           ;error value from last sample
deltadc fcb 0           ;rate of change compensated error
toggle  fcb 0           ;toggle for PWM buffers
```

To:

```
* Variables in RAM
        org $0050       ;start of RAM
edge1h  rmb 1           ;high byte of first edge count
edge1l  rmb 1           ;low byte of first edge count
edge2h  rmb 1           ;high byte of second edge count
edge2l  rmb 1           ;low byte of second edge count
period  rmb 1           ;timer value of feedback signal
pwidth  rmb 1           ;pulsewidth for motor - must be initialized
desper  rmb 1           ;desired feedback period - must be initialized
deltnew rmb 1           ;current error value
deltold rmb 1           ;error value from last sample
deltadc rmb 1           ;rate of change compensated error
toggle  rmb 1           ;toggle for PWM buffers
```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