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REV.3

POWER RISC CONTROL™

MPC500 Family

RISC PowerPC™ Microcontrollers

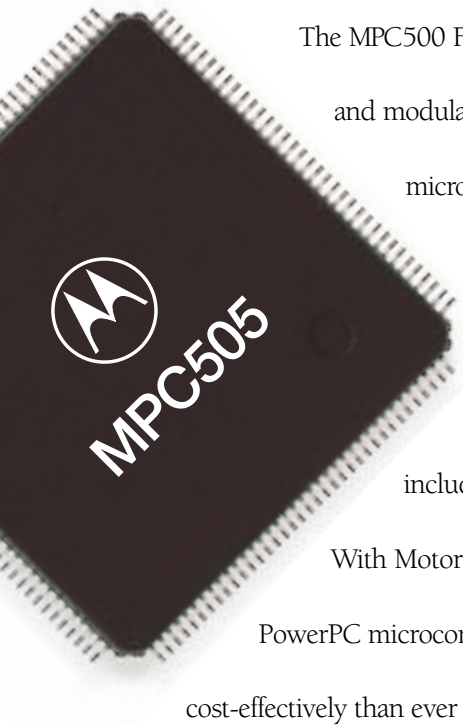
MOTOROLA
Semiconductor Products Sector

POWER RISC CONTROL

What happens when high performance and high expectations meet?

The MPC500 RISC Microcontroller (MCU) Family raises embedded control performance levels by leveraging the superior performance of a RISC processor based on the scalable PowerPC™ Architecture™.

And that's just part of the story.



The MPC500 Family also features the integration, functionality, and modularity that have become trademarks of Motorola microcontrollers.

Future MPC500 family members will enable designers to take advantage of Motorola's proven library of peripheral modules, including analog functions and non-volatile memory.

With Motorola, the power of high-performance RISC PowerPC microcontrollers can be utilized more efficiently and cost-effectively than ever before.

The MPC505 and MPC509

Performance

- *67K Dhrystone V2.1 (all data internal) @ 33 MHz*
- *16.5K Whetstone (all data internal) @ 33 MHz*

Technology

- *0.5 micron UDR II CMOS*
- *3.3 V ± 0.3 V*
- *Low-cost 160-pin Plastic QFP*

Features

- *32-bit PowerPC Architecture CPU*
- *32 32-bit General Purpose Registers*
- *Single & Double Precision Floating Point Unit*
- *32 Double Precision Floating Point Registers*
- *4 Kbytes On-chip Instruction Cache (I-Cache)*
- *4 Kbytes/28 Kbytes Static Random Access Memory (SRAM)*
- *Low-power Static Design (approx. 530 mW @ 25 MHz)*
- *Three Power-saving Modes: SLEEP, DOZE, and WAIT*
- *Dynamically Scalable Clock*
- *Software Programmable External Bus Sizing (16- or 32-bit transfers)*
- *12 Programmable Chip Selects With 0-7 Programmable Wait States*
- *Low Interrupt Latency (<1 μsec @ 25 MHz)*
- *Extensive Debug Support*
- *Testability-JTAG and Slave Mode Testing*
- *DC to 33 MHz Operation (40 MHz in future versions)*
- *–40 to 85 C Operating Range*

Central Processing Unit

The MPC500 CPU integrates four execution units: a Fixed-point Unit (FXU), a Load/Store Unit (LSU), a Branch Processing Unit (BPU), and a Floating-Point Unit (FPU). The FPU includes single- and double-precision multiply-add instructions.

PERFORMANCE RISC CONTROL

The MPC500 Family: Start your engines and follow our road map.

The 505 includes 4 Kbytes of SRAM, while the 509 includes 28 Kbytes SRAM; both feature 4 Kbytes of two-way set-associative instruction cache that is organized into 128 sets, with two lines per set and four words per line. Cache lines are aligned on four-word boundaries in memory. The cache uses a Least Recently Used (LRU) replacement algorithm.

Low pin count and a plastic package assure pin compatibility between the MPC509 and MPC505. In addition, 5V input pins provide flexibility and a greater choice of available memory devices. With 28 Kbytes on-chip SRAM, the MPC509 is well-suited for the most demanding industrial applications.

These innovative microcontrollers are software programmable to support 16- or 32-bit data buses, and can address up to 4 Gigabytes of memory. Additionally, they can function in both Big-Endian and Little-Endian modes to facilitate operation with a variety of external devices. Twelve interface-simplifying chip select signals are provided for external peripherals.

The MPC500 Family is derived from a revolutionary 32-bit RISC PowerPC microcontroller developed by Motorola specifically for use in transportation and industrial applications. Challenging automotive environmental conditions, ranging from voltage spikes to mechanical vibrations and electrical noise, have been excellent proving grounds for microcontroller quality and reliability. And, our MCUs have passed with flying colors on the test track.

The derivatives resulting from this ground-breaking development have been cost-effectively configured to meet the distinct needs of a wide variety of high-performance applications across the entire embedded control spectrum. The MPC505, MPC509, and future MPC500 family members will empower you with the performance of the PowerPC Architecture to design the most demanding embedded control applications.

The RISC factor.

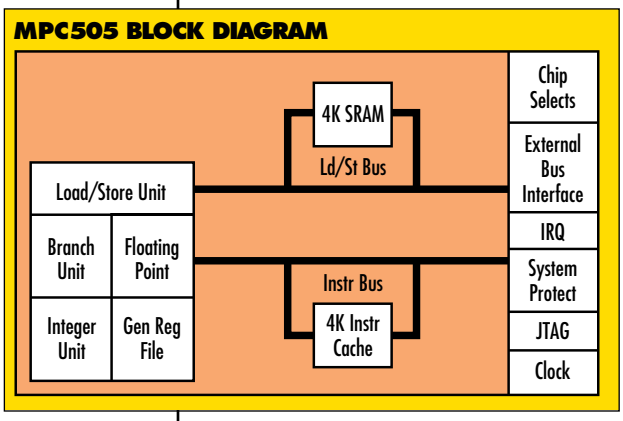
The PowerPC core, which is the foundation of the MPC500 Family, is more advanced and runs faster than its predecessors, setting performance standards for microcontrollers across a wide range of applications. As a result, Motorola customers can now enjoy the performance of RISC processors in tandem with the benefits offered by highly integrated microcontrollers. Motorola's library of on-chip peripheral modules allows re-use of code and eliminates the learning curve in using these modules, helping reduce your time-to-market. And, as more and more functions are integrated on-chip via proven peripheral modules and non-volatile memory, system costs will decrease.

CPU STRUCTURAL UNITS

Sequencer

Includes the branch processor, the instruction prefetch queue, and the interrupt-handling mechanism. Provides centralized control over data flow among execution units and the register files. Implements the basic instruction pipeline, fetches instructions from the memory system and issues them to available execution units, while maintaining a state history so it can back the machine up in the event of an exception.

MPC505 BLOCK DIAGRAM



Register

Includes all the user-visible registers, the registers' scoreboard mechanism, and keeps some history of previous operations to implement the precise interrupt model.

Load/store unit

Includes implementation of all load and store instructions, whether defined as part of the fixed-point processor or the floating-point processor.

Fixed-point unit

Includes implementation of all fixed-point instructions except load-store instructions. This module is divided into two sub-units: the IMUL-IDIV and the ALU-BFU.

Floating-point unit

Includes implementation of all floating-point instructions: Single and Double precision as outlined in the IEEE 754-1985 specification.

MIGRATION ISC CONTROL

MPC500: A powerful move.

The PowerPC Architecture definition sets forth stringent architectural standards to ensure compatibility of all PowerPC processors. And the MPC500 Family is fully compliant with all applicable standards. Consequently, software can be easily migrated across the PowerPC processor spectrum, helping save valuable development time and money. Motorola customers, of course, are no strangers to the concept of code portability. All Motorola microcontroller families were designed to provide an easy migration path, making software reusability a time and money-saving feature our customers have come to expect.

Floating Point Equation:

*Yi=b0 + (b1*x1) + (b2*x2) + (b3*x3).... (bk*xk) Real time Floating Point? No problem with the MPC500 Family.*

CPU Features

- *Four independent execution units and two register files*
- *BPU featuring static branch prediction and branch-folding capability during execution (zero-cycle branch execution time)*
- *Run-time reordering of loads and stores*

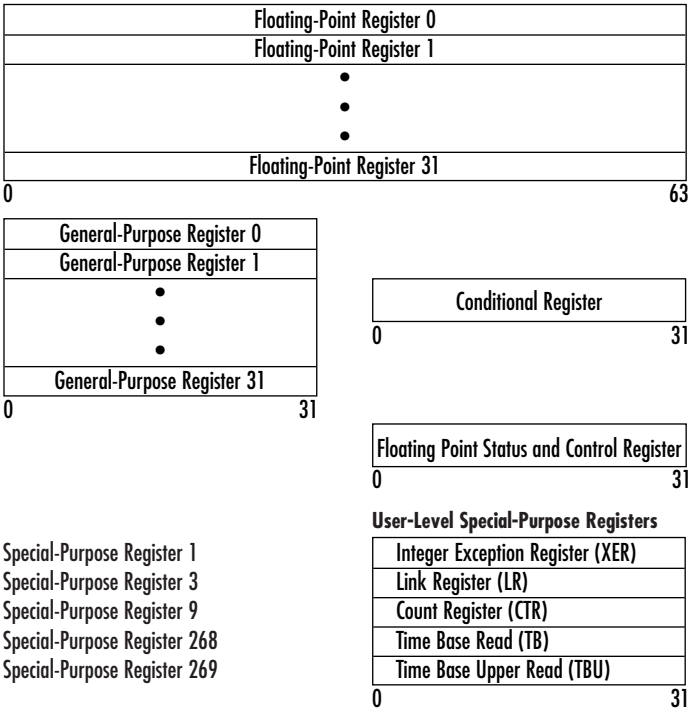
CPU Registers and Programming Model

The PowerPC Architecture defines register-to-register operations for most computation instructions. The three-register format of these instructions allows specification of a target register distinct from the two source operands. Load and store instructions transfer data between registers and memory. The device incorporates 32 GPRs, 32 FPRs, Special-Purpose Registers (SPRs), and several miscellaneous registers. PowerPC processors have two levels of privilege: supervisor mode (typically used by the operating environment) and user mode (used by the application software). Having access to privileged instructions, registers, and other resources allows the operating system to control the application environment (protecting operating-system and critical machine resources).

Instruction Set

All PowerPC instructions are encoded in single words (32-bit) that are four bytes long and word-aligned. This fixed instruction length and consistent format greatly simplify instruction pipelining. In addition, instruction formats are consistent among all instruction types, permitting efficient decoding to occur in parallel with operand accesses.

USER PROGRAMMING MODEL



Run the RISC.

What makes the MPC505 and MPC509 the ideal microcontroller entrées into the powerful realm of RISC? Low power consumption/low voltage, competitive cost/performance, modularity, and a variety of other customer-driven features.

Low power. Low voltage. High marks.

The MPC500 Family is the optimal choice for applications that require a high level of performance and low power consumption. The existing devices operate at 3.3 V with planned reductions to lower voltages. In addition to optimizing power requirements, the low-power operation helps keep heat build-up to a minimum and allows the use of low-cost plastic packaging.

Another plus for power-thrifty applications: three power down modes (SLEEP, DOZE, and WAIT) help conserve power by turning off particular peripheral modules when they are not in use.

Other features include a dynamically software-controlled clock that can be tailored to a particular task's required performance level and the clocking of modules only when their state is required to change.

The PowerPC Architecture provides for byte, half-word, and word operand loads and stores between memory and a set of 32 GPRs. Is also provides for word and double-word operand loads and stores between memory and a set of 32 Floating-Point Registers (FPRs). The instructions are divided into six categories:

- *Integer instructions, operating on byte, half-word, and word operands. These include computational and logical instructions.*

- *Floating-point instructions operate on single-precision (one word) and double-precision (one double word) floating-point operands and include status and control register instructions.*
- *Load/store instructions. These include integer and floating-point load and store instructions.*
- *Flow control instructions. These include branching instructions, condition register logical instructions, Itrap instructions, and other instructions that affect the instruction flow.*
- *Processor control instructions. These instructions are used for synchronizing memory accesses and cache management.*
- *Memory control instructions. These instructions provide control of the instruction cache.*

The higher the volume, the lower the cost.

With its automotive heritage, the MPC500 Family will live a long life. Designed to fit a wide variety of low-cost, high-volume applications, the MPC500 Family will benefit from Motorola's proven ability to produce cost-efficient microcontrollers. Through high-volume economies, low-cost packaging, innovative test procedures, and efficient assembly, Motorola continues to provide industry-leading price/performance value and to be the world's leading microcontroller supplier.*

SYSTEM INTERFACE UNIT

The System Interface Unit (SIU) consists of several blocks that control the buses of the chip, provide the clocks, and provide miscellaneous functions such as chip selects, test control, reset control, and I/O ports.

- *Internal Harvard architecture includes the Instruction bus (I-bus) and the Load/store bus (L-bus).*
- *Single External bus (E-bus)*
  - *External Bus Interface (EBI) connects internal busses with the E-bus.*
- *Chip select block provides user-programmable chip selects to select external memory or peripherals.*
- *Clock block controls the generation of the system clocks and programs the low power modes.*
- *Reset control function interfaces to the reset pins and provides a reset status register.*
- *I/O ports provide I/O functions on pins that are not used for their primary function.*

External Bus Interface

The External Bus Interface (EBI) interfaces the External bus (E-bus) with the two Internal buses (I-bus and L-bus). The E-bus is synchronous, pipelineable, and burstable. The bus has the ability to support multiple masters, but its protocol is optimized for a single-processor environment.

Modularity: A Motorola family trait.

With a second-generation Intermodule Bus (IMB2) designed for the MPC500 Family, Motorola extends the modular concept pioneered in the 68300 Family and also used in the 68HC16 Family. Both central algorithms and peripheral driver routines that are written in high level languages, such as "C", can easily be moved from the 68HC16 and 68300 families up to all existing and forthcoming 500 Family devices. Customers can work with familiar peripherals, taking advantage of Motorola's proven test suites, local field personnel who are already knowledgeable and trained, complete documentation, and the many benefits of reusing software in which significant resources have previously been invested.

These factors reduce development time which results in faster time-to-market and a competitive advantage for your product.

*Source: Dataquest and In-Stat, 1997.

Tools of the trade for embedded applications.

Motorola's software tool set for the MPC500 Family facilitates the development of embedded ROM code and operation with efficiently-sized RAM.

The tool set consists of an Optimizing C Compiler that optimizes C code and schedules the efficient use of the processor's resources, a powerful Macro Assembler that allows the conditional assembly and repeated assembly of blocks of code, a Flexible Linker that fits code to system hardware, an S-Record Generator for EPROM programming, a graphical Debugger, and an Archiver that generates library files.

Motorola has been a leading sponsor of the Embedded Application Binary Interface (EABI) Standard for embedded microcontrollers based on the PowerPC Architecture. This standard will help insure the future compatibility of interoperable PowerPC software tools offered by third-party suppliers.

There are many independent development tool suppliers who support the MPC500 Family, such as:

Compilers	Cygnus, Diab Data, GreenHills Software, Motorola, Software Development Systems
Debugger	GreenHills Software, Huntsville Microsystems, Lauterbach, Motorola, Software Development Systems, Wind River Systems
Integrated Development Environments	Avocet Systems, Microtec
RTOS	Accelerated Technology, CMX Company, ENEA Data, Integrated Systems, Kadak Products, Motorola, Wind River Systems, US Software
Emulators:	Huntsville Microsystems, iSystem, Lauterbach
Evaluation Boards:	Motorola
Adapters:	Ironwood Electronics

EBI Features

- *No external glue logic required for a simple system.*
- *Supports a variety of memory devices such as: SRAM and EEPROM.*
- *Fast (one-clock) arbitration possible.*
- *32-bit data bus, 32-bit address bus with byte enables.*
- *Protocol allows wait states to be inserted during the data phase.*
- *Supports 16- and 32-bit devices.*
- *Bus specified to minimize system power consumption.*

Basic Pipeline

- *The EBI supports pipelined accesses with up to two addresses outstanding.*

Chip Selects

Typical microcontrollers require additional hardware to provide external chip-select signals. On the 505, the chip select logic controls the system peripherals which allows the user to implement simple systems without the need for external glue logic.

Chip Select Module Features

- *No external glue logic required for typical systems when utilizing the CS module.*
- *Modular architecture for ease of expansion.*
- *12 pins programmable as Chip Enables, Output Enables, or Write Enables plus one CSBOOT pin.*
- *Supports multiple regions.*
- *Up to seven programmable wait states for slave devices.*
- *Controls the clocking of data to the slaves during write cycles.*
- *Programmable address range, block size.*

MOTOROLA RISC CONTROL

Your future is in control.

The MPC505 and MPC509 are just the beginning of Motorola's high-performance MPC500 Family of RISC PowerPC microcontrollers.

MPC500 Family members have been embedded in set top converters, advanced communications devices, speech processing systems, automotive modules, and many other applications that require high performance embedded control technology.

The standards of performance have changed. The standards of excellence, however, are the same ones that have served Motorola customers for two decades: A global design team. Worldwide manufacturing power. Dependable development support systems. And a staunch commitment to quality and total customer satisfaction. For more information about the MPC500 Family, please contact your Regional Motorola Sales Office or call (800) 795-7795, ext. 900; outside the U.S., call (512) 328-2268, ext. 900; or write to us at P.O. Box 13026, Austin, Texas, 78711-3026.

POWERED BY MOTOROLA™

Motorola's MPC500 Microcontroller Family. It's the RISC to run.

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