Modular Microcontroller Family

ADC

ANALOG-TO-DIGITAL CONVERTER
Reference Manual

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SECTION 1FUNCTIONAL OVERVIEW

The analog-to-digital converter (ADC), a module in Motorola's family of modular microcontrollers, is a unipolar, successive-approximation converter with eight modes of operation and selectable 8- or 10-bit resolution. Monotonicity is guaranteed for both 8- and 10-bit conversions. With a 16.78-MHz system clock, the ADC can perform an 8-bit single conversion in 8 microseconds or a 10-bit single conversion in 9 microseconds.

The ADC contains an analog and a digital subsystem. **Figure 1-1** is a functional block diagram of the ADC module.

1.1 Analog Subsystem

The analog subsystem consists of a multiplexer, an input sample amplifier, a resistor-capacitor digital-to-analog converter (RC DAC) array, and a high-gain comparator. The multiplexer selects one of eight internal or eight external signal sources for conversion. The sample amplifier buffers external high-impedance sources from the internal circuitry. The RC DAC array performs two functions: it acts as a sample-and-hold circuit, and it provides the digital-to-analog comparison output necessary for successive approximation conversion. The comparator indicates whether each successive output of the RC DAC array is higher or lower than the sampled input. **SECTION 4 ANALOG SUBSYSTEM** describes this subsystem in greater detail.

1.2 Digital Control Subsystem

The digital control subsystem contains registers and logic to control the conversion process. Control registers and associated logic select the conversion resolution (eight or ten bits), multiplexer input, conversion sequencing mode, sample time, and ADC clock cycle. As each input is converted, the digital control subsystem stores the result, one bit at a time, in the successive approximation register (SAR) and then transfers the result to one of eight result registers. Each result is available in three formats (right-justified unsigned, left-justified signed, and left-justified unsigned), depending on the address from which it is read. **SECTION 5 DIGITAL CONTROL SUBSYSTEM** describes the digital control functions in detail.

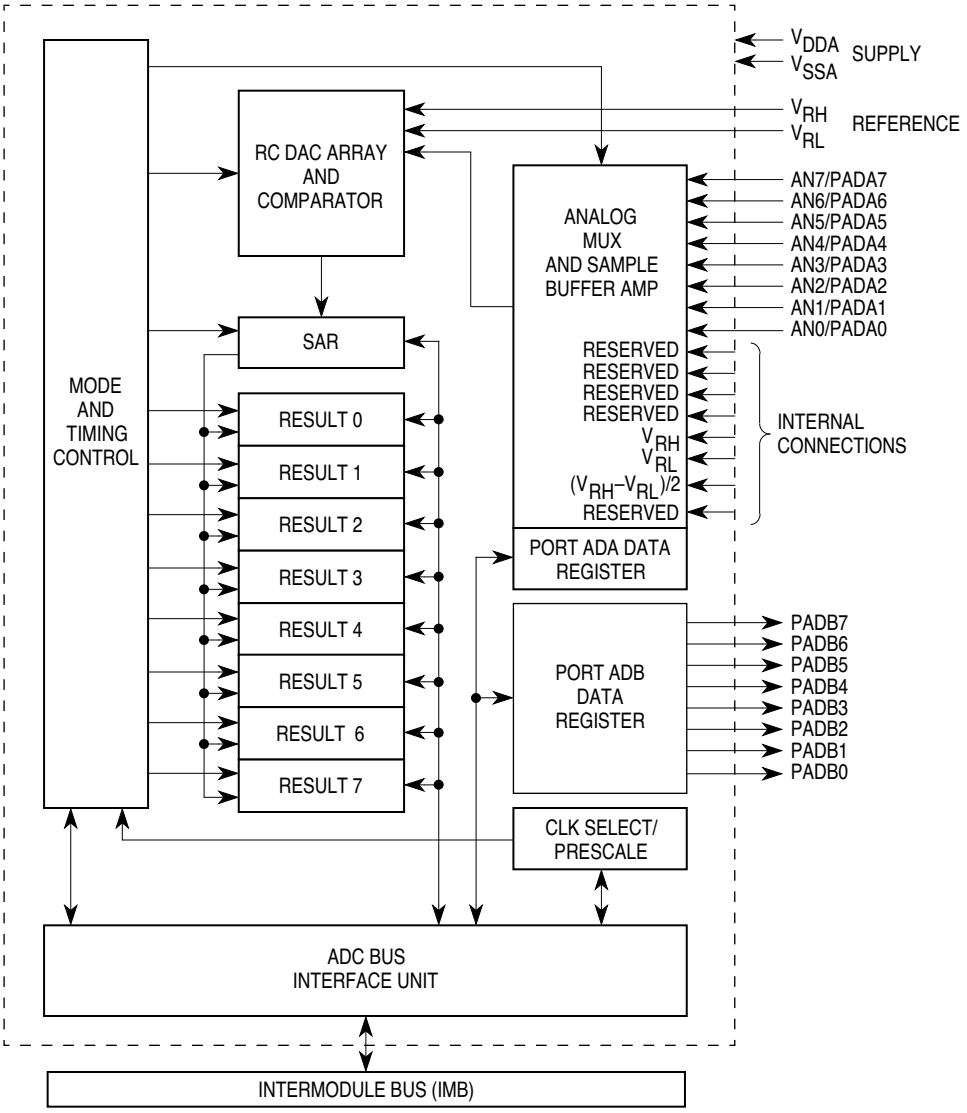


Figure 1-1 ADC Block Diagram

1.3 General-Purpose I/O

In addition to use as multiplexer inputs, the eight analog inputs can be used as a general-purpose digital input port (port ADA), provided signals are within logic level specification. Port ADB is a dedicated output port. A port data register (PDR) is used to access data from these ports. Refer to **SECTION 2 SIGNAL DESCRIPTIONS** and **3.3 General-Purpose I/O** for more information on ports ADA and ADB.

1.4 Module Configuration

The ADC module configuration register (ADCMCR) controls the interaction between the ADC and other modules. Low-power stop mode and freeze mode are ADC operating modes associated with assertion of IMB signals by other microcontroller modules

or by external sources. The ADCMCR also determines the privilege level at which most ADC registers operate. Refer to **3.2 Module Configuration** for additional information.

1.5 Bus Organization

The ADC bus interface unit (ABIU) serves as an interface between the ADC and the intermodule bus (IMB). The IMB handles communication between the ADC and other microcontroller modules and supplies timing signals to the ADC. For additional information on the ABIU, refer to **3.1 ADC Bus Interface Unit**.

1.6 Memory Map

The ADC module is mapped into 32 words of address space (see **Table 1-1**). Five words are control and status registers, one word is digital port data, and 24 words provide access to the results of A/D conversion (eight addresses for each type of converted data). Two words are reserved for expansion. The addresses provided in **Table 1-1** and elsewhere in this manual are offsets from the ADC base address. For the precise locations of these registers, consult the user's manual for the specific microcontroller unit (MCU). The column labeled “Access” in **Table 1-1** specifies which registers are supervisor only and which can be programmed to operate at either access level.

Table 1-1 ADC Module Memory Map

Address	Access	Control Registers
$XXXX00	S	Module Configuration Register (ADCMCR)
$XXXX02	S	ADC Test Register (ADCTEST)
$XXXX04	S	(Reserved)
$XXXX06	S/U	Port Data Register (PDR)
$XXXX08	S/U	(Reserved)
$XXXX0A	S/U	ADC Control Register 0 (ADCTL0)
$XXXX0C	S/U	ADC Control Register 1 (ADCTL1)
$XXXX0E	S/U	ADC Status Register (ADSTAT)
Address	**Access**	**Right-Justified Unsigned Result Registers**
$XXXX10	S/U	ADC Result Register 0 (RSLT0)
$XXXX12	S/U	ADC Result Register 1 (RSLT1)
$XXXX14	S/U	ADC Result Register 2 (RSLT2)
$XXXX16	S/U	ADC Result Register 3 (RSLT3)
$XXXX18	S/U	ADC Result Register 4 (RSLT4)
$XXXX1A	S/U	ADC Result Register 5 (RSLT5)
$XXXX1C	S/U	ADC Result Register 6 (RSLT6)
$XXXX1E	S/U	ADC Result Register 7 (RSLT7)
Address	**Access**	**Left-Justified Signed Result Registers**
$XXXX20	S/U	ADC Result Register 0 (RSLT0)
$XXXX22	S/U	ADC Result Register 1 (RSLT1)
$XXXX24	S/U	ADC Result Register 2 (RSLT2)
$XXXX26	S/U	ADC Result Register 3 (RSLT3)
$XXXX28	S/U	ADC Result Register 4 (RSLT4)
$XXXX2A	S/U	ADC Result Register 5 (RSLT5)
$XXXX2C	S/U	ADC Result Register 6 (RSLT6)
$XXXX2E	S/U	ADC Result Register 7 (RSLT7)
Address	**Access**	**Left-Justified Unsigned Result Registers**
$XXXX30	S/U	ADC Result Register 0 (RSLT0)
$XXXX32	S/U	ADC Result Register 1 (RSLT1)
$XXXX34	S/U	ADC Result Register 2 (RSLT2)
$XXXX36	S/U	ADC Result Register 3 (RSLT3)
$XXXX38	S/U	ADC Result Register 4 (RSLT4)
$XXXX3A	S/U	ADC Result Register 5 (RSLT5)
$XXXX3C	S/U	ADC Result Register 6 (RSLT6)
$XXXX3E	S/U	ADC Result Register 7 (RSLT7)

S = Supervisor-accessible only

S/U = Supervisor- or user-accessible depending on state of the SUPV bit in the ADCMCR

SECTION 2 SIGNAL DESCRIPTIONS

The ADC uses up to 20 pins. Up to eight pins are analog inputs (which can also be used as digital inputs), two pins are analog reference connections, and two pins are analog supply connections. In addition, eight pins serve as digital output pins in certain microcontroller systems. In systems not requiring these pins, they are not implemented, and the outputs from the module are not connected. Refer to the appropriate microcontroller user's manual for specific information.

2.1 Analog/Digital Input Pins (AN[7:0]/PADA[7:0])

Each of the eight analog input pins (AN[7:0]) is connected to a multiplexer in the ADC. The multiplexer selects an analog input to convert to digital data. Input voltages to the multiplexer must be between V_{RH} and V_{RL}. Refer to **SECTION 6 PIN CONNECTION CONSIDERATIONS** for recommendations on filtering the analog inputs.

The analog input pins can also be read as digital inputs, provided the applied voltage is within the limits specified in **APPENDIX A ELECTRICAL CHARACTERISTICS**.

When used as digital inputs, the pins are organized into an 8-bit port, port ADA. Data for port A is latched in the lower half of the 16-bit port data register (PDR). The digital inputs are then referred to as PADA[7:0]. When used for digital input, each of these pins is conditioned by a synchronizer with an enable feature. The synchronizer is not enabled until the actual IMB bus cycle addressing the PDR begins. This minimizes the high-current effect of mid-level signals on the inputs. This is particularly important when some of the inputs are being used as digital inputs and some as analog inputs. Refer to **3.3 General-Purpose I/O** for more information on port ADA.

2.2 Digital Output Pins (PADB[7:0])

The eight digital output pins (PADB[7:0]) make up port ADB, an output-only port. Data for port ADB is latched in the upper half of the PDR. On some MCUs, these pins are left unconnected and port ADB is not implemented.

A read of the upper byte of the port data register returns the digital value in the output register of port ADB. Refer to **3.3 General-Purpose I/O** for more information on this output port.

2.3 Analog Reference Pins

Separate high (V_{RH}) and low (V_{RL}) analog reference voltages are connected to the analog reference pins. Because they are separated from the analog power supply pins (V_{DDA} and V_{SSA}), the reference pins can be connected to regulated and filtered supplies that allow the ADC to achieve its highest degree of accuracy. Refer to **SECTION 6 PIN CONNECTION CONSIDERATIONS** for recommendations on filtering and conditioning the analog reference inputs.

The required reference voltage levels are provided in **APPENDIX A ELECTRICAL CHARACTERISTICS**.

2.4 Analog Supply Pins

Pins V_{DDA} and V_{SSA} supply power to the analog circuitry associated with the sample amplifier and RC DAC array. Other circuitry in the ADC is powered from the digital power bus (pins V_{DDI} and V_{SSI}). Dedicated power for the RC DAC array is necessary to isolate sensitive analog circuitry from noise on the digital power bus. Refer to **APPENDIX A ELECTRICAL CHARACTERISTICS** for precise electrical specifications.

SECTION 3CONFIGURATION AND CONTROL

Other microcontroller modules communicate with the ADC module via the intermodule bus (IMB). The ADC bus interface unit (ABIU) coordinates IMB activity with internal ADC bus activity. The first part of this section explains the operation of the ABIU. The second part of this section describes the ADC module configuration register (ADCMCR), which contains bits used to configure the ADC module. The final parts of this section discuss the general-purpose I/O functions of the ADC module and provide a checklist for initializing the ADC.

3.1 ADC Bus Interface Unit

The ABIU is designed to act as a slave device on the IMB. The IMB handles communication between the ADC and other microcontroller modules and supplies timing signals to the ADC. The ABIU provides IMB bus cycle termination and synchronizes internal ADC signals with IMB signals. The ABIU also manages data bus routing to accommodate the three conversion data formats and controls the interface to the ADC internal bus.

ADC registers are updated immediately when written to. However, if a conversion is in progress when a control bit is written, conversion halts and must be restarted before the new control parameter can take effect.

Communication between the IMB and the ADC is interleaved with internal ADC communication. ADC register accesses by the host system require bus cycles of three MCU clocks, so that each bus cycle contains six clock edges. Internal I/O (SAR to result registers) and I/O from the IMB occur during pre-assigned, non-conflicting times. This ensures that the ADC can access the SAR and result registers at all times.

3.2 Module Configuration

The ADCMCR contains bits that control the interaction of the ADC module with other MCU modules. These bits place the ADC in low-power or normal operation, determine the reaction of the ADC module to assertion of the CPU FREEZE command, and determine the privilege level required to access most ADC registers.

3.2.1 Low-Power Stop Operation

When the STOP bit in the ADCMCR is set, the IMB clock signal internal to the ADC is disabled. This places the module in an idle state and minimizes power consumption. The bus interface unit does not shut down and ADC registers are still accessible. Any conversion in progress when STOP is set is aborted.

Software can write to the ADCMCR to set the STOP bit. In addition, system reset (either internally or externally generated) sets this bit. Following either of these conditions, the STOP bit must be cleared before the ADC can be used. Because analog circuit bias currents are turned off when STOP is set, the ADC requires recovery time after the STOP bit is cleared.

Execution of the CPU LPSTOP command can place the entire modular microcontroller, including the ADC, in low-power stop mode by turning off the system clock. This command does not set the STOP bit in the ADCMCR. Before issuing the LPSTOP command, the user should assert the STOP bit in the ADCMCR so that the module stops in a known state.

3.2.2 Freeze Mode Operation

When the CPU enters background debugging mode, the FREEZE signal is asserted. The ADC can respond to internal assertion of FREEZE in three ways: it can ignore FREEZE assertion, finish the current conversion and then freeze, or freeze immediately. The type of response is determined by the value of the FRZ[1:0] field in the ADCMCR (see **Table 3-1**).

Table 3-1 FRZ Field Selection

FRZ	Response
00	Ignore FREEZE
01	Reserved
10	Finish conversion, then freeze
11	Freeze immediately

When the ADC freezes, the ADC clock stops and all sequential activity ceases. Contents of control and status registers remain valid while frozen. When the FREEZE signal is negated, ADC activity resumes.

If the ADC freezes during a conversion, activity resumes with the next step in the conversion sequence. However, capacitors in the analog conversion circuitry may discharge while the ADC is frozen, and conversion results may be inaccurate.

3.2.3 Privilege Levels

To protect system resources, the processor in certain MCUs can operate at either of two privilege levels: user or supervisor. In systems that support privilege levels, accesses of the ADCMCR and ADCTEST registers are permissible only when the CPU is operating at the supervisor privilege level. The remaining ADC registers are programmable to permit supervisor access only or to permit access when the CPU is operating at either privilege level.

If the SUPV bit in the ADCMCR is set, access to ADC registers is permitted only when the CPU is operating at the supervisor level. If SUPV is clear, then both user and supervisor accesses of all registers other than the ADCMCR and ADCTEST register are permitted.

The ADC does not respond to a read or write of a supervisor-access register when the CPU is operating at the user privilege level. Attempting such a read or write results in the bus access being transferred externally. Refer to the SIM or SCIM section of the appropriate MCU user's manual for details on external bus cycles to unimplemented locations.

MCUs that do not support privilege levels always operate at the supervisor level, so that ADC registers are always accessible.

3.2.4 ADC Module Configuration Register (ADCMCR)

The ADCMCR contains fields and bits that control freeze and stop modes and determine the privilege level required to access most ADC registers.

ADCMCR — ADC Module Configuration Register **$XXXX00**

15	14	13	12 … 8	7	6 … 0
STOP	FRZ		NOT USED	SUPV	NOT USED
RESET:					
1	0	0		0	

STOP — STOP Mode
- 0 = Normal operation
- 1 = Low-power operation

FRZ[1:0] — Freeze

The FRZ field determines ADC response to assertion of the FREEZE signal by the CPU.
- 00 = Ignore FREEZE
- 01 = Reserved
- 10 = Finish conversion, then freeze
- 11 = Freeze immediately

SUPV — Supervisor/User
- 0 = User access permitted to registers controlled by the SUPV bit
- 1 = Supervisor access only permitted to ADC registers

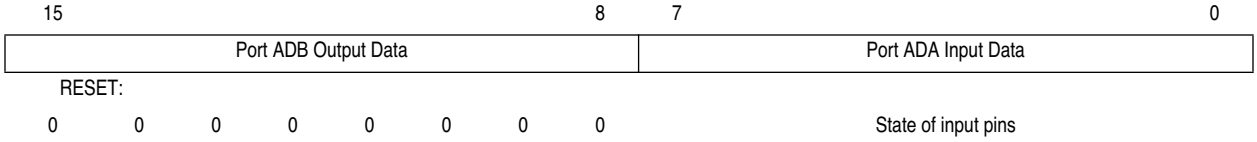
3.3 General-Purpose I/O

Two digital ports are associated with the ADC. These ports are accessed through the 16-bit port data register (PDR). Port ADA, an input-only port, uses the eight analog input pins. (Certain MCUs may provide fewer than eight analog input pins. Refer to the appropriate MCU user's manual for details.) Data for port ADA is accessed in the lower half of the PDR. The digital level of an input port pin may be read at any time. A read of the PDR does not affect an A/D conversion in progress. Use of any port A pin for digital input does not preclude the use of any other port A pin for analog input.

If the signal on the input pin is not within V_{IH} and V_{IL} specification (i.e., if the signal is in the dead band region), a read of the PDR returns an undetermined value.

Port ADB, an output-only port, uses pins PADB[7:0]. Data for Port ADB is latched in the upper half of the PDR. On some MCUs, port ADB is not implemented. On these MCUs, reads of the upper half of the PDR return whatever value was last written to the upper half of the register.

PDR — Port Data Register **$XXXX02**



3.4 ADC Test Register (ADCTEST)

ADCTEST — ADC Test Register **$XXXX06**

ADCTEST is used only during factory testing of the MCU.

3.5 Initialization Checklist

To initialize the ADC submodule and begin a conversion sequence, follow these steps:

1. Write to the ADCMCR to ensure the STOP and FREEZE bits are cleared and assign the desired value to the SUPV bit.
2. Write to ADCTL0 to select the sample time, ADC clock prescaler, and 8- or 10-bit resolution.
3. Write to ADCTL1 to select the conversion mode (SCAN, MULT, and S8CM bits) and conversion channel or channels (CD:CA) and to begin a conversion sequence.

Once a conversion sequence has begun, the type of conversion mode selected determines the programming sequence. Refer to **SECTION 5 DIGITAL CONTROL SUBSYSTEM** for additional information on conversion modes and the ADC control and status registers.

SECTION 4 ANALOG SUBSYSTEM

This section describes the operation of the analog subsystem. Understanding this subsystem is helpful in designing ADC applications and in using the digital control functions that regulate A/D conversion. Refer to **SECTION 6 PIN CONNECTION CONSIDERATIONS** for ADC design considerations and **SECTION 5 DIGITAL CONTROL SUBSYSTEM** for details concerning digital control functions.

The analog subsystem consists of a multiplexer, sample capacitors, a buffer amplifier, an RC DAC array, and a high-gain comparator. Comparator output is used to sequence the successive approximation register (SAR). Since the SAR, like the rest of the analog subsystem, is not directly accessible to user software, its description is included in this section.

4.1 Multiplexer

The multiplexer selects one of eight external or eight internal sources for conversion. The eight internal sources include V_{RH}, V_{RL}, $(V_{RH} – V_{RL}) / 2$, and five reserved channels. Multiplexer operation is controlled by channel selection field [CD:CA] in ADCTL1. Refer to **5.6 Channel Selection** for details on selecting a conversion channel.

The multiplexer contains positive clamping and negative stress protection circuitry. This circuitry prevents voltages (within certain limits) on other input channels from affecting the current conversion.

4.2 Sample Buffer Amplifier

Each of the eight external input channels is associated with a sample capacitor and share a single sample buffer amplifier. After a conversion is initiated, the multiplexer output is connected to the sample capacitor at the input of the sample buffer amplifier for the first two ADC clock cycles of the sampling period. The sample amplifier buffers the input channel from the relatively large capacitance of the RC DAC array. The input channel sees only the small sample capacitors during this period.

During the second two ADC clock cycles of the sampling period, the sample capacitor is disconnected from the multiplexer, and the stored level in the sample capacitor is transferred to the RC DAC array via the sample buffer amplifier.

During the third part of the sampling period, the sample capacitor and amplifier are bypassed, and the multiplexer input charges the RC DAC array directly. Charging the RC DAC array directly once the stored voltage level approaches the input voltage allows the ADC to achieve a high degree of accuracy. Moreover, since the voltage on the RC DAC array is nearly equal to the external voltage by the start of this third period, this RC DAC voltage presents very little loading to the external circuitry. This results in higher allowable input impedance and virtually no charge-sharing between channels.

The length of this third period is determined by the value in the STS field of ADCTL0. Refer to **5.1 Conversion Timing** for additional information on ADC conversion timing.

4.3 RC DAC Array

The RC DAC array consists of binary-weighted capacitors and a resistor-divider chain. The array performs two functions: it acts as a sample-and-hold circuit during conversion and provides each successive digital-to-analog comparison voltage to the comparator. Conversion begins with MSB comparison and ends with LSB comparison. Array switching is controlled by the digital subsystem.

4.4 Comparator

The comparator indicates whether each approximation output from the RC DAC array during resolution is higher or lower than the sampled input voltage. Comparator output is fed to the digital control logic, which sets or clears each bit in the successive approximation register in sequence, MSB first.

4.5 Successive Approximation Register (SAR)

The SAR accumulates the result of each conversion one bit at a time, starting with the most significant bit. At the start of the resolution period, the MSB of the SAR is set, and all less significant bits are cleared. Depending on the result of the first comparison, the MSB is either left set or cleared. Each successive bit is set or left cleared in descending order until all eight or ten bits have been resolved.

When conversion is complete, the content of the SAR is transferred to the appropriate result register, where it can be read by software. The SAR itself is not accessible to user software.

SECTION 5 DIGITAL CONTROL SUBSYSTEM

The digital control subsystem includes control and status registers, clock and prescaler control logic, channel and reference select logic, conversion sequence control logic, and eight result registers. The successive approximation register, which holds each conversion result before it is transferred to the appropriate result register, is discussed in **SECTION 4 ANALOG SUBSYSTEM**.

ADCTL0 and ADCTL1 (ADC control registers 0 and 1) and associated logic select the conversion resolution (8 or 10 bits), input channel, conversion mode, sample time, and ADC clock cycle. ADSTAT (the ADC status register) contains flags indicating the completion of A/D conversions. Writing to ADCTL1 initiates a conversion.

Conversion results are stored, one bit at a time, in the SAR. Results are discrete values between 0 and 255 ($2^8 – 1$) for 8-bit conversions and between 0 and 1023 ($2^{10} – 1$) for 10-bit conversions. One binary unit = $(V_{RH} – V_{RL}) / 2^n$, where n = 8 or 10. Each converted result is transferred from the SAR to bits [7:0] (for 8-bit conversion) or [9:0] (for 10-bit conversion) of the appropriate result register. Each result is available in three formats (right-justified unsigned, left-justified signed, and left-justified unsigned), depending on the address from which it is read.

The following subsections discuss control functions involving the control and status registers. Register diagrams are provided later in this section. (They are also provided in **APPENDIX B MEMORY MAP AND REGISTERS**.)

5.1 Conversion Timing

Total conversion time is made up of initial sample time, transfer time, final sample time, and resolution time. Initial sample time refers to the time during which the selected input channel is connected to the sample capacitor at the input of the sample buffer amplifier. During the transfer period, the sample capacitor is disconnected from the multiplexer, and the stored voltage is buffered and transferred to the RC DAC array. During the final sampling period, the sample capacitor and amplifier are bypassed, and the multiplexer input charges the RC DAC array directly. During the resolution period, the voltage in the RC DAC array is converted to a digital value and stored in the SAR.

Initial sample time and transfer time are fixed at 2 ADC clock cycles each. Final sample time can be 2, 4, 8, or 16 ADC clock cycles, depending on the value of the STS field in ADCTL0. (Refer to **5.3 Final Sample Time**.) Resolution time is 10 cycles for 8-bit conversion and 12 cycles for 10-bit conversion.

Transfer and resolution therefore require a minimum of 16 ADC clocks (8 µs with a 2.1-MHz ADC clock) for 8-bit resolution or 18 ADC clocks (9 µs with a 2.1-MHz ADC clock) for 10-bit resolution. If the user selects the maximum final sample time period of 16 ADC clocks, the total conversion time is 15 µs for an 8-bit conversion or 16 µs for a 10-bit conversion (with a 2.1-MHz ADC clock).

Figure 5-1 and **Figure 5-2** illustrate the timing for 8- and 10-bit conversions, respectively. These diagrams assume a final sampling period of two ADC clocks.

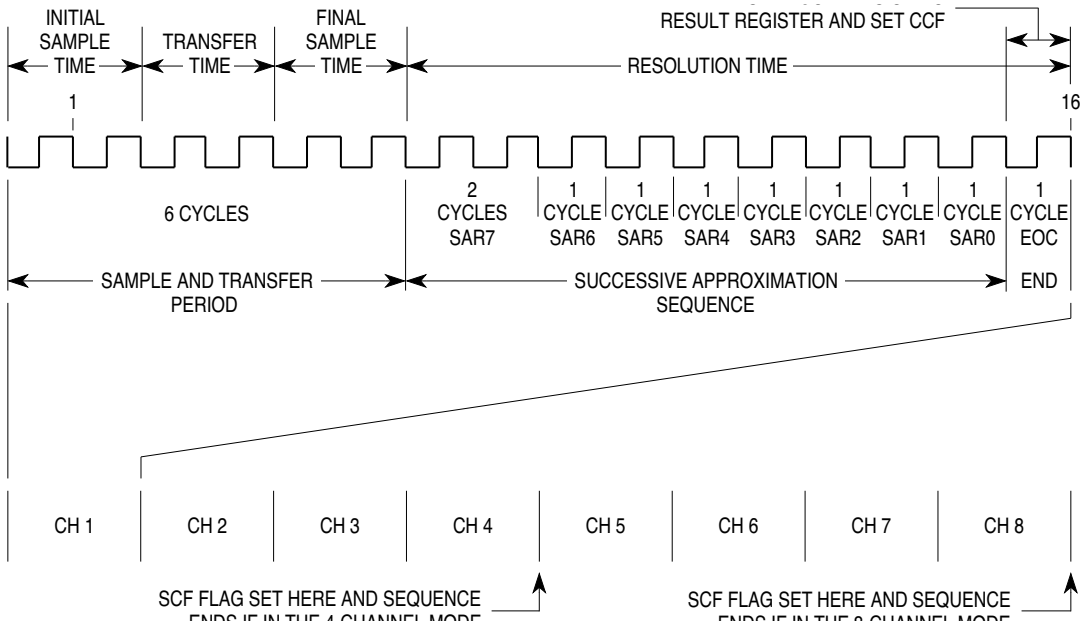


Figure 5-1 8-Bit Conversion Timing

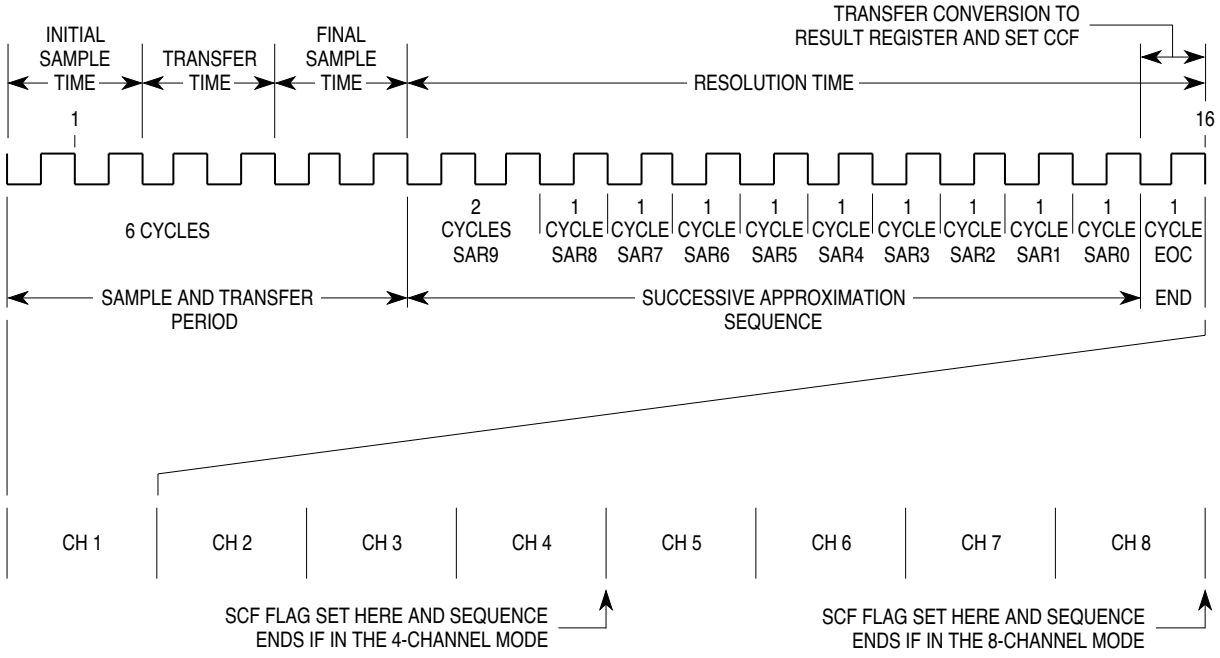


Figure 5-2 10-Bit Conversion Timing

5.2 Clock and Prescaler Control

The ADC clock is derived from the system clock by a programmable prescaler. The prescaler has two stages. The first stage is a 5-bit modulus counter contained in the PRS field in ADCTL0. The system clock is divided by this value + 1 and then fed to the second stage, a divide-by-two circuit, to generate the ADC clock. Figure 5–3 illustrates the relationship of ADC clock to system clock.

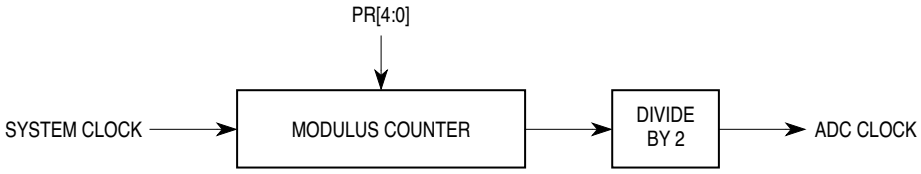


Figure 5-3 ADC Clock and Prescaler Control

ADC clock frequency must be between 0.5 and 2.1 MHz. The reset value of the PRS field is %00011, which divides a nominal 16.78 MHz system clock by eight, yielding maximum ADC clock frequency. The clock generation circuitry ensures that the ADC clock can never be faster than one fourth the system clock speed. Thus there are a minimum of four full IMB clock cycles for each ADC clock cycle.

Table 5-1 shows prescaler output values and associated minimum and maximum system clock speeds.

Table 5-1 Prescaler Output

PRS[4:0]	ADC Clock	Minimum System Clock	Maximum System Clock
%00000	Reserved	–	–
%00001	System Clock/4	2.0 MHz	8.4 MHz
%00010	System Clock/6	3.0 MHz	12.6 MHz
%00011	System Clock/8	4.0 MHz	16.8 MHz
. . .	. . .	. . .	. . .
%11101	System Clock/60	30.0 MHz	—
%11110	System Clock/62	31.0 MHz	—
%11111	System Clock/64	32.0 MHz	—

5.3 Final Sample Time

During the final sample period, the selected channel is connected directly to the RC DAC array for the specified sample time. The value of the STS (sample time select) field in ADCTL0 determines final sample time in ADC clock cycles. The sample period is thus determined by both the PRS field (which controls the ADC clock period) and the STS field. Final sample time can be 2, 4, 8, or 16 ADC clocks (see **Table 5-2**).

Table 5-2 STS Field Selection

STS[1:0]	Sample Time
00	2 A/D Clock Periods
01	4 A/D Clock Periods
10	8 A/D Clock Periods
11	16 A/D Clock Periods

5.4 Resolution

ADC resolution can be either eight or ten bits. Resolution is determined by the state of the RES10 bit in ADCTL0 (0 = 8-bit resolution, 1 = 10-bit resolution). Both 8-bit and 10-bit conversion results are automatically aligned in the result registers. Refer to **5.1 Conversion Timing** for the time required for 8- and 10-bit conversions.

5.5 Conversion Mode

Conversion mode is controlled by three bits in ADCTL1. **Table 5-3** shows the meaning of these bits.

Table 5-3 Conversion Mode Bits

Bit	Meaning
SCAN (Scan mode selection)	Conversion can be limited to a single sequence or performed continuously 0 = Single sequence 1 = Continuous conversions
MULT (Multichannel conversions)	Conversion can be run on a single channel or on a block of four or eight channels (depending on S8CM) 0 = Single channel 1 = Multiple channels
S8CM (Select 8-conversion sequence mode)	Length of a conversion sequence 0 = 4 conversions 1 = 8 conversions

The combination of these bits determines the conversion mode, as shown in **Table 5-4** and explained in the following paragraphs. Conversion begins with the multiplexer input specified by the value in the CD:CA field of ADCTL1.

Table 5-4 ADC Conversion Modes

SCAN	MULT	S8CM	Mode
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Mode 0 — A single 4-conversion sequence is performed on a single input channel specified by the value in CD:CA. Each result is stored in a separate result register (RSLT0 to RSLT3). The appropriate CCF bit in ADSTAT is set as each register is filled. The SCF bit in ADSTAT is set when the conversion sequence is complete.

Mode 1 — A single 8-conversion sequence is performed on a single input channel specified by the value in CD:CA. Each result is stored in a separate result register (RSLT0 to RSLT7). The appropriate CCF bit in ADSTAT is set as each register is filled. The SCF bit in ADSTAT is set when the conversion sequence is complete.

Mode 2 — A single conversion is performed on each of four sequential input channels, starting with the channel specified by the value in CD:CC. Each result is stored in a separate result register (RSLT0 to RSLT3). The appropriate CCF bit in ADSTAT is set as each register is filled. The SCF bit in ADSTAT is set when the last conversion is complete.

Mode 3 — A single conversion is performed on each of eight sequential input channels, starting with the channel specified by the value in CD. Each result is stored in a separate result register (RSLT0 to RSLT7). The appropriate CCF bit in ADSTAT is set as each register is filled. The SCF bit in ADSTAT is set when the last conversion is complete.

Mode 4 — Continuous 4-conversion sequences are performed on a single input channel specified by the value in CD:CA. Each result is stored in a separate result register (RSLT0 to RSLT3). Previous results are overwritten when a sequence repeats. The appropriate CCF bit in ADSTAT is set as each register is filled. The SCF bit in ADSTAT is set when the first 4-conversion sequence is complete.

Mode 5 — Continuous 8-conversion sequences are performed on a single input channel specified by the value in CD:CA. Each result is stored in a separate result register (RSLT0 to RSLT7). Previous results are overwritten when a sequence repeats. The appropriate CCF bit in ADSTAT is set as each register is filled. The SCF bit in ADSTAT is set when the first 8-conversion sequence is complete.

Mode 6 — Continuous conversions are performed on each of four sequential input channels, starting with the channel specified by the value in CD:CC. Each result is stored in a separate result register (RSLT0 to RSLT3). The appropriate CCF bit in ADSTAT is set as each register is filled. The SCF bit in ADSTAT is set when the first 4-conversion sequence is complete.

Mode 7 — Continuous conversions are performed on each of eight sequential input channels, starting with the channel specified by the value in CD. Each result is stored in a separate result register (RSLT0 to RSLT7). The appropriate CCF bit in ADSTAT is set as each register is filled. The SCF bit in ADSTAT is set when the first 8-conversion sequence is complete.

5.6 Channel Selection

The value of the channel selection field (CD:CA) in ADCTL1 determines which multiplexer input or inputs are used in a conversion sequence. There are 16 possible inputs. Eight inputs are external pins (AN[7:0]), and eight are internal.

Table 5-5 summarizes ADC operation when MULT is cleared (single-channel modes). **Table 5-6** summarizes ADC operation when MULT is set (multichannel modes). The SCAN bit determines whether single or continuous conversion sequences are performed. Channel numbers are given in order of conversion.

Table 5-5 Single-Channel Conversions

S8CM	CD	CC	CB	CA	Input	Result Register
0	0	0	0	0	AN0	RSLT0 – RSLT3
0	0	0	0	1	AN1	RSLT0 – RSLT3
0	0	0	1	0	AN2	RSLT0 – RSLT3
0	0	0	1	1	AN3	RSLT0 – RSLT3
0	0	1	0	0	AN4	RSLT0 – RSLT3
0	0	1	0	1	AN5	RSLT0 – RSLT3
0	0	1	1	0	AN6	RSLT0 – RSLT3
0	0	1	1	1	AN7	RSLT0 – RSLT3
0	1	0	0	0	Reserved	RSLT0 – RSLT3
0	1	0	0	1	Reserved	RSLT0 – RSLT3
0	1	0	1	0	Reserved	RSLT0 – RSLT3
0	1	0	1	1	Reserved	RSLT0 – RSLT3
0	1	1	0	0	V_{RH}	RSLT0 – RSLT3
0	1	1	0	1	V_{RL}	RSLT0 – RSLT3
0	1	1	1	0	$(V_{RH} – V_{RL}) / 2$	RSLT0 – RSLT3
0	1	1	1	1	Test/Reserved	RSLT0 – RSLT3
1	0	0	0	0	AN0	RSLT0 – RSLT7
1	0	0	0	1	AN1	RSLT0 – RSLT7
1	0	0	1	0	AN2	RSLT0 – RSLT7
1	0	0	1	1	AN3	RSLT0 – RSLT7
1	0	1	0	0	AN4	RSLT0 – RSLT7
1	0	1	0	1	AN5	RSLT0 – RSLT7
1	0	1	1	0	AN6	RSLT0 – RSLT7
1	0	1	1	1	AN7	RSLT0 – RSLT7
1	1	0	0	0	Reserved	RSLT0 – RSLT7
1	1	0	0	1	Reserved	RSLT0 – RSLT7
1	1	0	1	0	Reserved	RSLT0 – RSLT7
1	1	0	1	1	Reserved	RSLT0 – RSLT7
1	1	1	0	0	V_{RH}	RSLT0 – RSLT7
1	1	1	0	1	V_{RL}	RSLT0 – RSLT7
1	1	1	1	0	$(V_{RH} – V_{RL}) / 2$	RSLT0 – RSLT7
1	1	1	1	1	Test/Reserved	RSLT0 – RSLT7

Table 5-6 Multiple-Channel Conversions

S8CM	CD	CC	CB	CA	Input	Result Register
0	0	0	X	X	AN0	RSLT0
					AN1	RSLT1
					AN2	RSLT2
					AN3	RSLT3
0	0	1	X	X	AN4	RSLT0
					AN5	RSLT1
					AN6	RSLT2
					AN7	RSLT3
0	1	0	X	X	Reserved	RSLT0
					Reserved	RSLT1
					Reserved	RSLT2
					Reserved	RSLT3
0	1	1	X	X	V_{RH}	RSLT0
					V_{RL}	RSLT1
					$(V_{RH} – V_{RL}) / 2$	RSLT2
					Test/Reserved	RSLT3
1	0	X	X	X	AN0	RSLT0
					AN1	RSLT1
					AN2	RSLT2
					AN3	RSLT3
					AN4	RSLT4
					AN5	RSLT5
					AN6	RSLT6
					AN7	RSLT7
1	1	X	X	X	Reserved	RSLT0
					Reserved	RSLT1
					Reserved	RSLT2
					Reserved	RSLT3
					V_{RH}	RSLT4
					V_{RL}	RSLT5
					$(V_{RH} – V_{RL}) / 2$	RSLT6
					Test/Reserved	RSLT7

5.7 Control and Status Registers

There are two control registers and one status register. Writes to ADCTL1 initiate a conversion. If a conversion sequence is already in progress, a write to either control register aborts it and resets the SCF and CCF flags in ADSTAT.

5.7.1 ADC Control Register 0 (ADCTL0)

ADCTL0 is used to select the conversion resolution (8 or 10 bits), the sample time, and the clock/prescaler value. Writing to this register aborts any conversion in progress, and ADC activity halts until a write to ADCTL1 occurs.

ADCTL0 — ADC Control Register 0 **$XXXX0A**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOT USED								RES10	STS		PRS				
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

RES10 — 10-Bit Resolution
0 = 8-bit conversion
1 = 10-bit conversion

STS[1:0] — Sample Time Select
00 = 2 A/D Clock Periods
01 = 4 A/D Clock Periods
10 = 8 A/D Clock Periods
11 = 16 A/D Clock Periods
The STS field selects the final sample time, after the buffered sample transfer has occurred. Refer to **5.1 Conversion Timing** and **5.3 Final Sample Time** for additional information.

PRS[4:0] — Prescaler Rate Selection
%00000 = System Clock/4
%00001 = System Clock/4
%00010 = System Clock/6
%00011 = System Clock/8
.. .. . .
%11101 = System Clock/60
%11110 = System Clock/62
%11111 = System Clock/64
The system clock is divided by the PRS value plus one, then divided by two, to determine the ADC clock. (Assigning a value of zero to this field, however, has the same effect as assigning a value of one.) Refer to **5.2 Clock and Prescaler Control** for more information.

5.7.2 ADC Control Register 1 (ADCTL1)

ADCTL1 is used to select the conversion mode and the channel or channels to be converted. Writing to this register aborts any conversion in progress and initiates a new conversion. Refer to **5.5 Conversion Mode** and **5.6 Channel Selection** for additional information on these fields.

ADCTL1 — ADC Control Register 1 **$XXXX0C**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOT USED									SCAN	MULT	S8CM	CD	CC	CB	CA
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SCAN — Scan Mode Selection
0 = Single conversion sequence
1 = Continuous conversion

MULT — Multichannel Conversion

0 = Conversion sequence(s) run on a channel selected by CD:CA.

1 = Sequential conversion of four or eight channels selected by CD:CA.

S8CM — Select Eight-Conversion Sequence Mode

0 = Four-conversion sequence

1 = Eight-conversion sequence

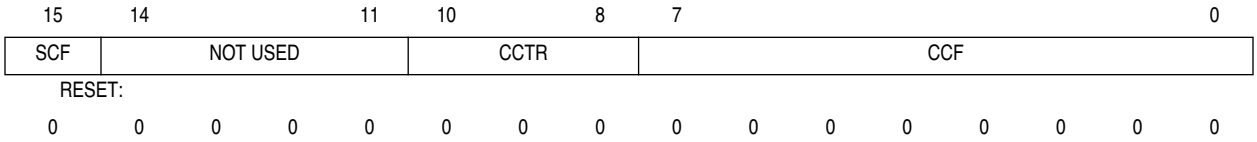
CD:CA — Channel Selection

The bits in this field are used to select an input or block of inputs for A/D conversion. **Table 5-5** and **Table 5-6** explain the operation of these fields.

5.7.3 ADC Status Register (ADSTAT)

ADSTAT is a read-only register that contains the sequence complete flag (SCF), conversion counter (CCTR), and one channel converted flag (CCF) for each of the eight channels.

ADSTAT — ADC Status Register **$XXXX0E**



SCF — Sequence Complete Flag

This bit is set at the end of the conversion sequence when SCAN = 0 in ADCTL1 and set at the end of the first conversion sequence when SCAN = 1.

0 = Sequence not complete

1 = Sequence complete

CCTR[2:0] — Conversion Counter

This field shows the content of the conversion counter pointer during a conversion sequence. The value is the number of the next result register to be written to (i.e., the channel currently being converted).

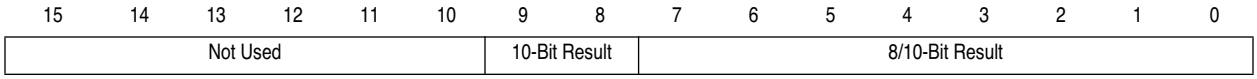
CCF[7:0] — Conversion Complete Flags

Each bit in this field corresponds to an A/D result register (CCF7 corresponds to RSLT7, etc.). A bit is set when conversion of the corresponding input is complete and is cleared when the result register containing the converted value is read.

5.8 Result Registers (RSLT0–RSLT7)

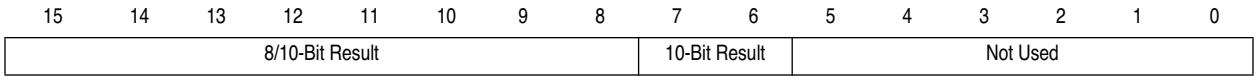
The eight read-only result registers store data after conversion is complete. Each register can be read from three different addresses in the register block. Data format depends on the address from which it is read. The result registers reside on the internal differential data bus.

Unsigned Right-Justified Format $XXXX10–$XXXX1F



The conversion result is unsigned right-justified data. Bits [9:0] are used for 10-bit resolution, bits [7:0] are used for 8-bit resolution (bits [9:8] are zero). Bits [15:10] always return zero when read.

Signed Left-Justified Format $XXXX20–$XXXX2F

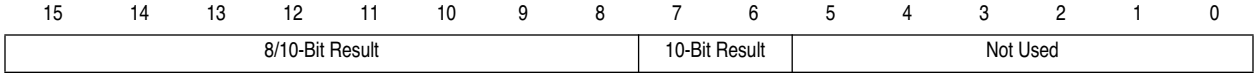


The conversion result is signed left-justified data. Bits [15:6] are used for 10-bit resolution, bits [15:8] are used for 8-bit resolution (bits [7:6] are zero).

Although the ADC is a unipolar converter, this data format is provided by assuming that the zero reference point is $(V_{RH} + V_{RL}) / 2$. When the register is read, bit 15 returns zero for a positive number and one for a negative number. For a negative number, the value read is in twos complement form. Bits [5:0] return zeros when read. For eight-bit conversions, the table below summarizes the results of a read of the upper byte of this register.

Input Voltage	Digital Result
+ Full scale (V_{RH})	$7F
Bipolar zero ((V_{RH} - V_{RH})/2)	$00
Zero - 1 count	$FF
– Full scale (V_{RL})	$80

Unsigned Left-Justified Format $XXXX30–$XXXX3F



The conversion result is unsigned left-justified data. Bits [15:6] are used for 10-bit resolution, bits [15:8] are used for 8-bit resolution (bits [7:6] are zero). Bits [5:0] always return zero when read.

SECTION 6 PIN CONNECTION CONSIDERATIONS

The ADC requires accurate, noise-free input signals for proper operation. This section discusses the design of external circuitry to maximize ADC performance.

6.1 Analog Reference Pins

No A/D converter can be more accurate than its analog reference. Any noise in the reference can result in at least that much error in a conversion. The reference for the ADC, supplied by pins V_{RH} and V_{RL}, should be low-pass filtered from its source to obtain a noise-free, clean signal. In many cases, simple capacitive bypassing may suffice. In extreme cases, inductors or ferrite beads may be necessary if noise or RF energy is present. Series resistance is not advisable since there is an effective DC current requirement from the reference voltage by the internal resistor string in the RC DAC array. External resistance may introduce error in this architecture under certain conditions. Any series devices in the filter network should contain a minimum amount of DC resistance.

For accurate conversion results, the analog reference voltages must be within the limits defined by V_{DDA} and V_{SSA}, as explained in the following subsection.

6.2 Analog Power Pins

The analog supply pins (V_{DDA} and V_{SSA}) define the limits of the analog reference voltages (V_{RH} and V_{RL}) and of the analog multiplexer inputs. **Figure 6-1** is a diagram of the analog input circuitry.

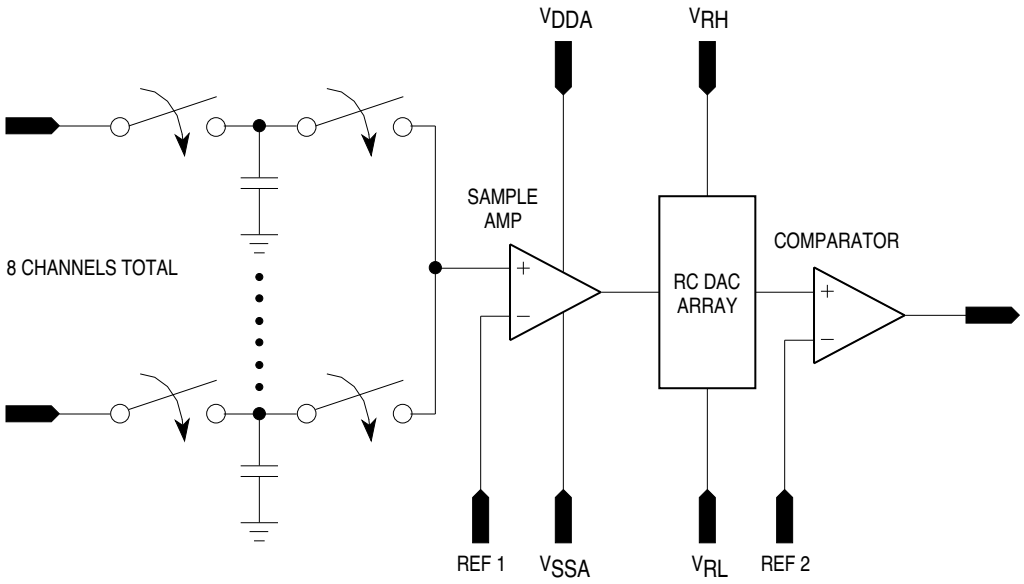


Figure 6-1 Analog Input Circuitry

Since the sample amplifier is powered by V_{DDA} and V_{SSA}, it can accurately transfer input signal levels up to but not exceeding V_{DDA} and down to but not below V_{SSA}. If the input signal is outside of this range, the output from the sample amplifier is clipped.

In addition, V_{RH} and V_{RL} must be within the range defined by V_{DDA} and V_{SSA}. As long as V_{RH} is less than or equal to V_{DDA} and V_{RL} is greater than or equal to V_{SSA} and the sample amplifier has accurately transferred the input signal, resolution is ratiometric within the limits defined by V_{RL} and V_{RH}. If V_{RH} is greater than V_{DDA}, the sample amplifier can never transfer a full-scale value. If V_{RL} is less than V_{SSA}, the sample amplifier can never transfer a zero value.

Figure 6-2 shows the results of reference voltages outside the range defined by V_{DDA} and V_{SSA}. At the top of the input signal range, V_{DDA} is 10 mV lower than V_{RH}. This results in a maximum obtainable 10-bit conversion value of 3FE. At the bottom of the signal range, V_{SSA} is 15 mV higher than V_{RL}, resulting in a minimum obtainable 10-bit conversion value of 3.

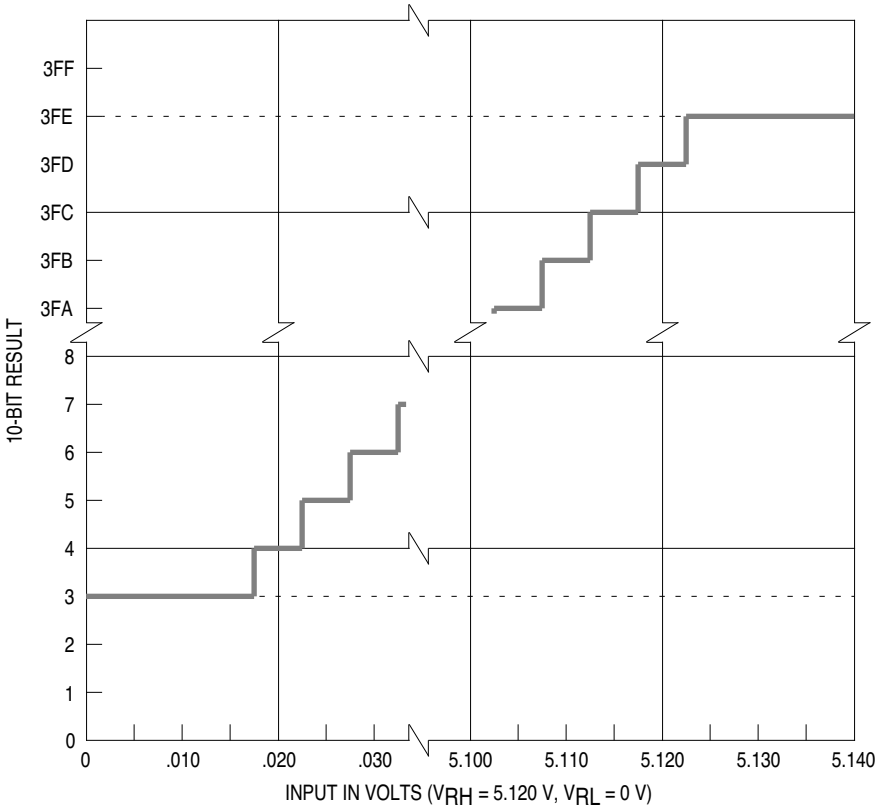


Figure 6-2 Errors Resulting from Clipping

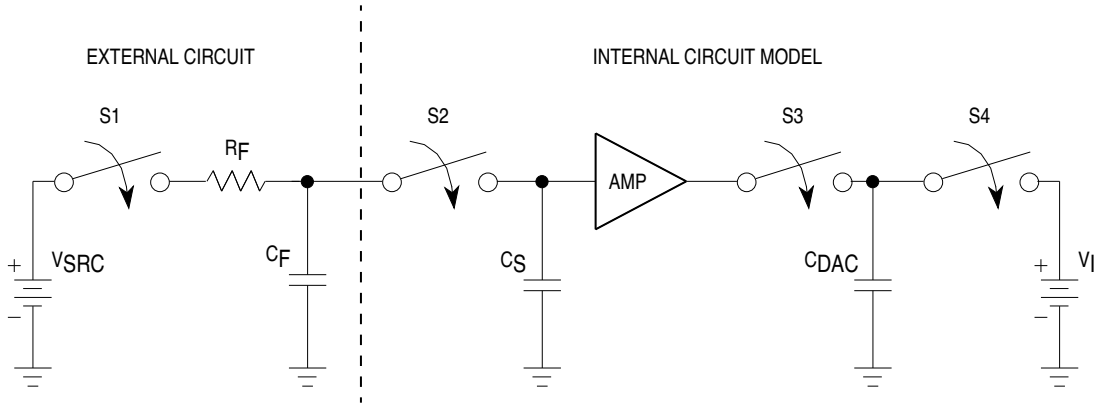
6.3 Analog Input Pins

Analog inputs should have low AC impedance at the pins. Low AC impedance can be realized by placing a capacitor with good high frequency characteristics at the input pin of the part. Ideally, that capacitor should be as large as possible (within the practi-

cal range of capacitors that still have good high frequency characteristics). This capacitor has two effects. First, it helps attenuate any noise that may exist on the input. Second, it sources charge during the sample period when the analog signal source is a high-impedance source.

Series resistance can be used with the capacitor on an input pin to implement a simple RC filter. The maximum level of filtering at the input pins is application dependent and is based on the bandpass characteristics required to accurately track the dynamic characteristics of an input. Simple RC filtering at the pin may be limited by the source impedance of the transducer or circuit supplying the analog signal to be measured. (Refer to **6.3.2 Error Resulting from Leakage**.) In some cases, the size of the capacitor at the pin may be very small.

Figure 6-3 is a simplified model of an input channel. Refer to this model in the following discussion of the interaction between the user's external circuitry and the circuitry inside the ADC.



V_{SRC} = Source voltage
R_F = Filter impedance (source impedance included)
C_F = Filter capacitor
C_S = Internal capacitance (for a bypassed channel, this is the C_{DAC} capacitance)
C_{DAC} = DAC capacitor array
V_I = Internal voltage source for precharge ($V_{DD}/2$)

Figure 6-3 Electrical Model of an A/D Input Pin

In **Figure 6-3**, R_F and C_F comprise the user's external filter circuit. C_S is the internal sample capacitor. The value for this capacitor is 2 pF. Each channel has its own capacitor. The 2-pF capacitor is never precharged: it retains the value of the last sample. V_I is an internal voltage source used to precharge the DAC capacitor array (C_{DAC}) before each sample. The value of this supply is $V_{DD}/2$, or 2.5 volts for 5-volt operation.

The following paragraphs provide a simplified description of the interaction between the ADC and the user's external circuitry. This circuitry is assumed to be a simple RC low-pass filter passing a signal from a source to the ADC input pin. The following simplifying assumptions are made:

- The source impedance is included with the series resistor of the RC filter.
- The external capacitor is perfect (no leakage, no significant dielectric absorption characteristics, etc.)
- All parasitic capacitance associated with the input pin is included in the value of the external capacitor.
- Inductance is ignored.
- The “on” resistance of the internal switches is zero ohms and the “off” resistance is infinite.

6.3.1 Settling Time for the External Circuit

The values for R_F and C_F in the user's external circuitry determine the length of time required to charge C_F to the source voltage level (V_{SRC}). At time t = 0, S1 in **Figure 6-3** closes. S2 is open, disconnecting the internal circuitry from the external circuitry. Assume that the initial voltage across C_F is 0. As C_F charges, the voltage across it is determined by the following equation, where t is the total charge time:

$$V_{CF} = V_{SRC}(1–e^{–t/R_FC_F})$$

When t = 0, the voltage across C_F = 0. As t approaches infinity, V_{CF} will equal V_{SRC}. (This assumes no internal leakage.) With 10-bit resolution, 1/2 of a count is equal to 1/2048 full-scale value. Assuming worst case (V_{SRC} = full scale), **Table 6-1** shows the required time for C_F to charge to within 1/2 of a count of the actual source voltage during 10-bit conversions. Note that these times are completely independent of the A/D converter architecture (assuming the ADC is not affecting the charging).

Table 6-1 External Circuit Settling Time (10-Bit Conversions)

Filter Capacitor	Source Resistance			
	100 Ω	**1 kΩ**	**10 kΩ**	**100 kΩ**
1 μF	760 μs	7.6 ms	76 ms	760 ms
.1 μF	76 μs	760 μs	7.6 ms	76 ms
.01 μF	7.6 μs	76 μs	760 μs	7.6 ms
.001 μF	760 ns	7.6 μs	76 μs	760 μs
100 pF	76 ns	760 ns	7.6 μs	76 μs

The external circuit described in **Table 6-1** is a low-pass filter. A user interested in measuring an AC component of the external signal must take the characteristics of this filter into account.

6.3.2 Error Resulting from Leakage

A series resistor can limit the current to a pin, but input leakage acting through a large source impedance can degrade A/D accuracy. The maximum input leakage current is specified in **APPENDIX A ELECTRICAL CHARACTERISTICS**. Input leakage is greatest at high operating temperatures and as a general rule decreased by one half for each 10° C decrease in temperature.

When $V_{RH} – V_{RL}$ = 5.12 V, 1 count (assuming 10-bit resolution) corresponds to 5 mV of input voltage. A typical input leakage of 50 nA acting through 100 kΩ of external se-

ries resistance results in an error of less than 1 count (5.0 mV). If the source impedance is 1 MΩ and a typical leakage of 50 nA is present, an error of 10 counts (50 mV) is introduced.

In addition to internal junction leakage, external leakage (e.g., if external clamping diodes are used) and charge sharing effects with internal capacitors also contribute to the total leakage current. **Table 6-2** illustrates the effect of different levels of total leakage on accuracy for different values of source impedance. The error is listed in terms of 10-bit counts. Notice that leakage from the part of 10 nA is obtainable only within a limited temperature range.

Table 6-2 Error Resulting from Input Leakage (I_{OFF})

Source Impedance	Leakage Value (10-bit Conversions)				
	10 nA	**50 nA**	**100 nA**	**1000 nA**	
1 kΩ	—	—	—	0.2 counts	
10 kΩ	—	0.1 counts	0.2 counts	2 counts	
100 kΩ	0.2 counts	1 count	2 counts	20 counts	

APPENDIX A ELECTRICAL CHARACTERISTICS

The following ratings define the conditions under which the ADC can operate without damage.

Table A-1 Maximum Ratings

Num	Parameter	Symbol	Min	Max	Unit
1	Analog Supply	V_{DDA}	– 0.3	6.5	V
2	Internal Digital Supply	V_{DDI}	– 0.3	6.5	V
3	Reference Supply	V_{RH}, V_{RL}	– 0.3	6.5	V
4	V_{SS} Differential Voltage	$V_{SSI} - V_{SSA}$	– 0.1	0.1	V
5	V_{DD} Differential Voltage	$V_{DDI} - V_{DDA}$	– 6.5	6.5	V
6	V_{REF} Differential Voltage	$V_{RH} - V_{RL}$	– 6.5	6.5	V
7	V_{REF} to V_{DDA} Differential Voltage	$V_{RH} - V_{DDA}$	– 6.5	6.5	V
8	Disruptive Input Current[1,2]	I_{NA}	– 15	15	µA

NOTES:

1. Below disruptive current conditions, the channel being stressed will have conversion values of $3FF for analog inputs greater than V_{RH} and $000 for values less than V_{RL}. This assumes that $V_{RH} \leq V_{DDA}$ and $V_{RL} \geq V_{SSA}$ due to the presence of the sample amplifier. Other channels are not affected by non-disruptive conditions
2. Input signals with large slew rates or high frequency noise components cannot be converted accurately. These signals also interfere with conversion of other channels.

Table A-2 ADC DC Electrical Characteristics (Operating)

(VSS = 0 Vdc, ADCLK = 2.1 MHz, TA within operating temperature range)

Num	Parameter	Symbol	Min	Max	Unit
1	Analog Supply[1]	V_{DDA}	4.5	5.5	V
2	Internal Digital Supply[1]	V_{DDI}	4.5	5.5	V
3	V_{SS} Differential Voltage	$V_{SSI} - V_{SSA}$	– 1.0	1.0	mV
4	V_{DD} Differential Voltage	$V_{DDI} - V_{DDA}$	– 1.0	1.0	V
5	Reference Voltage Low[2]	V_{RL}	V_{SSA}	V_{DDA} / 2	V
6	Reference Voltage High[2]	V_{RH}	V_{DDA} / 2	V_{DDA}	V
7	V_{REF} Differential Voltage	$V_{RH} - V_{RL}$	4.5	5.5	V
8	Input Voltage[2]	V_{INDC}	V_{SSA}	V_{DDA}	V
9	Input High, Digital Port	V_{IH}	0.7 (V_{DDA})	V_{DDA} + 0.3	V
10	Input Low, Digital Port	V_{IL}	V_{SSA} – 0.3	0.2 (V_{DDA})	V
11	CMOS Output High, Digital Port I_{OH} = – 10.0 µA	V_{OH}	V_{DDA}– 0.2	—	V
12	Output Low, Digital Port I_{OL} = 10.0 µA	V_{OL}	—	0.2	V
13	Output High, Digital Port I_{OH} = – 0.8 mA	V_{OH}	V_{DDA}– 0.8	—	V
14	Output Low, Digital Port I_{OL} = 1.6 mA	V_{OL}	—	0.4	V
15	Analog Supply Current[3]	I_{DDA}	—	1.0	mA
17	Reference Supply Current	I_{REF}	—	250	µA
18	Input Current, Off Channel[4]	I_{OFF}	—	100	nA
19	Total Input Capacitance, Not Sampling	C_{INN}	—	10	pF
20	Total Input Capacitance, Sampling	C_{INS}	—	15	pF

NOTES:

1. Refers to operation over full temperature and frequency range.
2. To obtain full-scale, full-range results, $V_{SSA} \le V_{RL} \le V_{INDC} \le V_{RH} \le V_{DDA}$.
3. Current measured at maximum system clock frequency with all modules active.
4. Maximum leakage occurs at maximum operating temperature. As a general rule, current decreases by half for each 10° C below maximum temperature

Table A-3 ADC AC Characteristics (Operating)

(VDD and VDDA = 5.0 Vdc ± 10%, VSS = 0 Vdc, TA within operating temperature range)

Num	Parameter	Symbol	Min	Max	Unit
1	IMB Clock Frequency	F_{ICLK}	2.0	16.78	MHz
2	ADC Clock Frequency	F_{ADCLK}	0.5	2.1	MHz
3	8-bit Conversion Time (16 ADC Clocks)[1]	T_{CONV}	7.62	—	µs
4	10-bit Conversion Time (18 ADC Clocks)[1]	T_{CONV}	8.58	—	µs
5	Stop Recovery Time	T_{SR}	—	10	µs

NOTES:

1. Assumes 2.1 MHz ADC clock and selection of minimum sample time (2 ADC clocks)

Table A-4 Analog Converter Characteristics (Operating)

(VDD and VDDA = 5.0 Vdc ± 10%, VSS = 0 Vdc, TA = TL to TH, ADCLK = 2.1 MHz)

Num	Parameter	Symbol	Min	Typ	Max	Unit
1	8-bit Resolution[1]	1 Count	—	20	—	mV
2	8-bit Differential Nonlinearity[2]	DNL	–0.5	—	0.5	Counts
3	8-bit Integral Nonlinearity[2]	INL	–1	—	1	Counts
4	8-bit Absolute Error[2,3]	AE	–1	—	1	Counts
5	10-bit Resolution[1]	1 Count	—	5	—	mV
6	10-bit Differential Nonlinearity[2]	DNL	–0.5	—	0.5	Counts
7	10-bit Integral Nonlinearity[2]	INL	–2	—	2	Counts
8	10-bit Absolute Error[2,4]	AE	–2.5	—	2.5	Counts
9	Source Impedance at Input[5]	R_S	—	20	See Note 5	kΩ

NOTES:

1. $V_{RH} – V_{RL} \geq 5.12$ V; $V_{DDA} - V_{SSA} = 5.12$ V
2. At $V_{REF} = 5.12$ V, one 10-bit count = 5 mV and one 8-bit count = 20 mV.
3. 8-bit absolute error of 1 count (20 mV) includes 1/2 count (10 mV) inherent quantization error and 1/2 count (10 mV) circuit (differential, integral, and offset) error.
4. 10-bit absolute error of 2.5 counts (12.5 mV) includes 1/2 count (2.5 mV) inherent quantization error and 2 counts (10 mV) circuit (differential, integral, and offset) error.
5. Maximum source impedance is application-dependent. Error resulting from pin leakage depends on junction leakage into the pin and on charge-sharing effects with internal capacitors. Error from junction leakage is a function of source impedance and input leakage current:

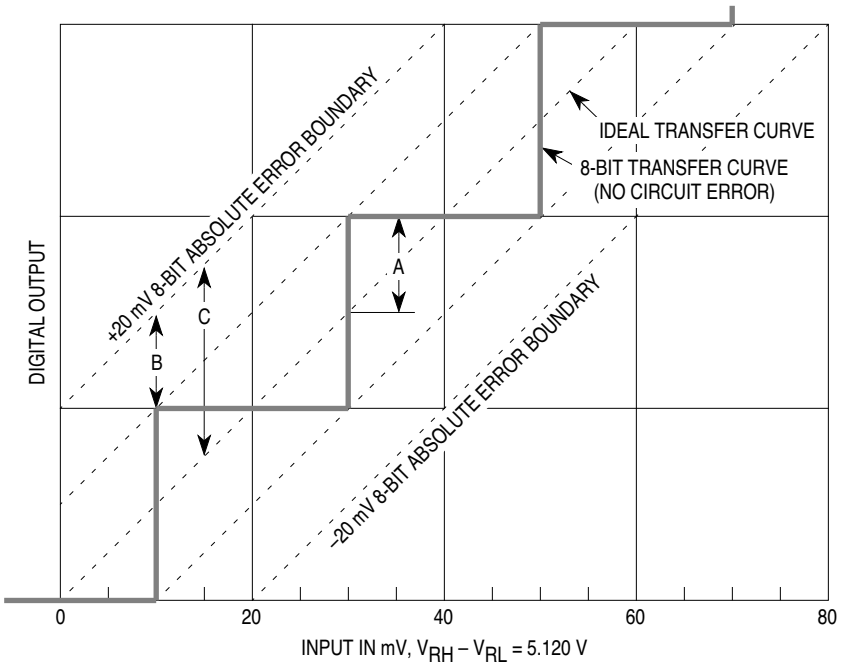
   $$V_{err} = R_S \bullet I_{OFF}$$

   where I_{OFF} is a function of operating temperature. (See note 4 in Table A–2.) Charge-sharing effects with internal capacitors are a function of ADC clock speed, the number of channels being scanned, and source impedance. For 10-bit conversions, charge pump leakage is computed as follows:

   $$V_{err10} = .25 \text{ pF} \bullet V_{DDA} \bullet R_S \bullet \text{ ADCLK}/(9 \bullet \text{number of channels})$$

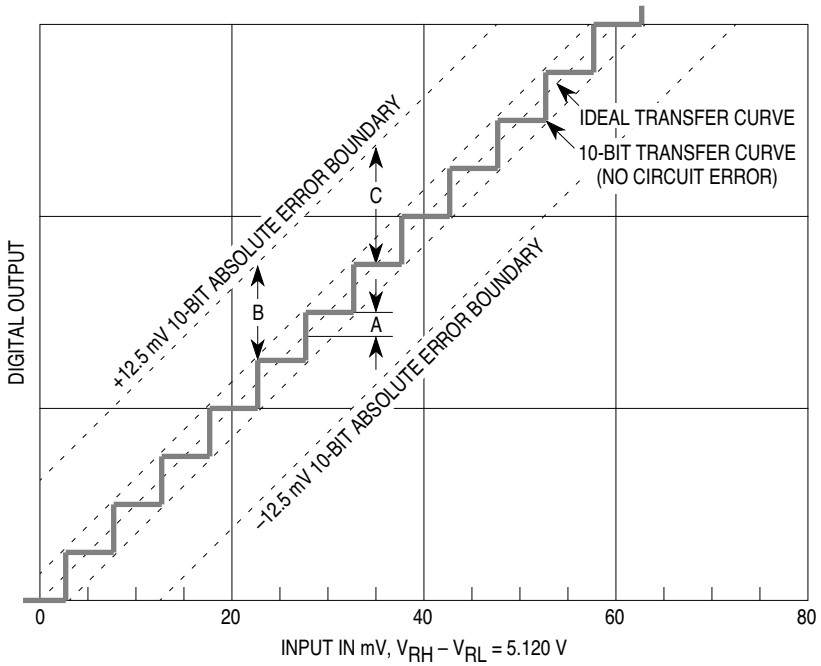
   For 8-bit conversions, charge pump leakage is computed as follows:

   $$V_{err8} = .25 \text{ pF} \bullet V_{DDA} \bullet R_S \bullet \text{ ADCLK}/(8 \bullet \text{number of channels})$$



A – +1/2-count (10 mV) inherent quantization error
B – Circuit-contributed +10 mV error
C – +20 mV absolute error (one 8-bit count)

Figure A-1 Circuit and Quantization Error in 8-Bit Conversions



A – +1/2-count (2.5 mV) inherent quantization error
B – Circuit-contributed +10 mV error
C – +12.5 mV absolute error (2-1/2 10-bit counts)

Figure A-2 Circuit and Quantization Error in 10-Bit Conversions

APPENDIX B MEMORY MAP AND REGISTERS

B.1 Memory Map

Address	Access	Control Registers
$XXXX00	S	Module Configuration Register (ADCMCR)
$XXXX02	S	ADC Test Register (ADCTEST)
$XXXX04	S	(Reserved)
$XXXX06	S/U	Port Data Register (PDR)
$XXXX08	S/U	(Reserved)
$XXXX0A	S/U	ADC Control Register 0 (ADCTL0)
$XXXX0C	S/U	ADC Control Register 1 (ADCTL1)
$XXXX0E	S/U	ADC Status Register (ADSTAT)
Address	**Access**	**Right-Justified Unsigned Result Registers**
$XXXX10	S/U	ADC Result Register 0 (RSLT0)
$XXXX12	S/U	ADC Result Register 1 (RSLT1)
$XXXX14	S/U	ADC Result Register 2 (RSLT2)
$XXXX16	S/U	ADC Result Register 3 (RSLT3)
$XXXX18	S/U	ADC Result Register 4 (RSLT4)
$XXXX1A	S/U	ADC Result Register 5 (RSLT5)
$XXXX1C	S/U	ADC Result Register 6 (RSLT6)
$XXXX1E	S/U	ADC Result Register 7 (RSLT7)
Address	**Access**	**Left-Justified Signed Result Registers**
$XXXX20	S/U	ADC Result Register 0 (RSLT0)
$XXXX22	S/U	ADC Result Register 1 (RSLT1)
$XXXX24	S/U	ADC Result Register 2 (RSLT2)
$XXXX26	S/U	ADC Result Register 3 (RSLT3)
$XXXX28	S/U	ADC Result Register 4 (RSLT4)
$XXXX2A	S/U	ADC Result Register 5 (RSLT5)
$XXXX2C	S/U	ADC Result Register 6 (RSLT6)
$XXXX2E	S/U	ADC Result Register 7 (RSLT7)
Address	**Access**	**Left-Justified Unsigned Result Registers**
$XXXX30	S/U	ADC Result Register 0 (RSLT0)
$XXXX32	S/U	ADC Result Register 1 (RSLT1)
$XXXX34	S/U	ADC Result Register 2 (RSLT2)
$XXXX36	S/U	ADC Result Register 3 (RSLT3)
$XXXX38	S/U	ADC Result Register 4 (RSLT4)
$XXXX3A	S/U	ADC Result Register 5 (RSLT5)
$XXXX3C	S/U	ADC Result Register 6 (RSLT6)
$XXXX3E	S/U	ADC Result Register 7 (RSLT7)

S = Supervisor-accessible only
S/U = Supervisor- or user-accessible depending on state of the SUPV bit in the ADCMCR

B.2 Registers

ADCMCR — ADC Module Configuration Register **$XXXX00**

15	14	13	12 … 8	7	6 … 0
STOP	FRZ		NOT USED	SUPV	NOT USED
RESET:					
1	0	0		0	

STOP — STOP Mode
- 0 = Normal operation
- 1 = Low-power operation

FRZ[1:0] — Freeze

The FRZ field determines ADC response to assertion of the FREEZE signal by the CPU.
- 00 = Ignore FREEZE
- 01 = Reserved
- 10 = Finish conversion, then freeze
- 11 = Freeze immediately

SUPV — Supervisor/Unrestricted
- 0 = Unrestricted access to registers controlled by the SUPV bit
- 1 = Supervisor access only

PDR — Port Data Register **$XXXX06**

15 … 8	7 … 0
Port ADB Output Data	Port ADA Input Data
RESET:	
0 0 0 0 0 0 0 0	State of input pins

ADCTL0 — ADC Control Register 0 **$XXXX0A**

15 … 8	7	6	5	4	3	2	1	0
NOT USED	RES10	STS		PRS				
RESET:								
0 0 0 0 0 0 0 0	0	0	0	0	0	0	1	1

RES10 — 10-Bit Resolution
- 0 = 8-bit conversion
- 1 = 10-bit conversion

STS[1:0] — Sample Time Select Field

The STS field selects the initial sample time.
- 00 = 2 A/D clock periods
- 01 = 4 A/D clock periods
- 10 = 8 A/D clock periods
- 11 = 16 A/D clock periods

Refer to **5.1 Conversion Timing** and **5.3 Final Sample Time** for additional information.

PRS[4:0] — Prescaler Rate Selection Field

%00000 = System Clock/4
%00001 = System Clock/4
%00010 = System Clock/6
%00011 = System Clock/8
. . . . . .
%11101 = System Clock/60
%11110 = System Clock/62
%11111 = System Clock/64

The system clock is divided by the PRS value plus one, then divided by two, to determine the ADC clock. (Assigning a value of zero to this field, however, has the same effect as assigning a value of one.) Refer to **5.2 Clock and Prescaler Control** for more information.

ADCTL1 — ADC Control Register 1 **$XXXX0C**

15							8	7	6	5	4	3	2	1	0
NOT USED									SCAN	MULT	S8CM	CD	CC	CB	CA
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SCAN — Scan Mode Selection Bit

0 = Single conversion sequence
1 = Continuous conversion

MULT — Multichannel Conversion Bit

0 = Conversion sequence(s) run on a channel selected by [CD:CA].
1 = Sequential conversion of four or eight channels selected by [CD:CA].

S8CM — Select Eight-Conversion Sequence Mode

0 = Four-conversion sequence
1 = Eight-conversion sequence

CD:CA — Channel Selection

The bits in this field are used to select an input or block of inputs for A/D conversion. **Table 5-5** and **Table 5-6** explain the operation of these fields.

ADSTAT — ADC Status Register **$XXXX0E**

15	14			11	10		8	7							0
SCF	NOT USED				CCTR			CCF							
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SCF — Sequence Complete Flag

This bit is set at the end of the conversion sequence when SCAN = 0 in ADCTL1 and set at the end of the first conversion sequence when SCAN = 1.

0 = Sequence not complete
1 = Sequence complete

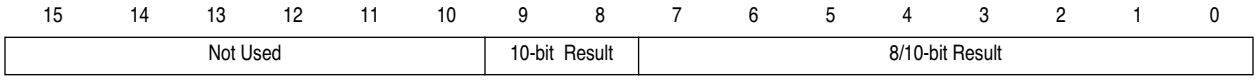
CCTR[2:0] — Conversion Counter

This field shows the content of the conversion counter pointer during a conversion sequence. The value is the number of the next result register to be written to (i.e., the channel currently being converted).

CCF[7:0] — Conversion Complete

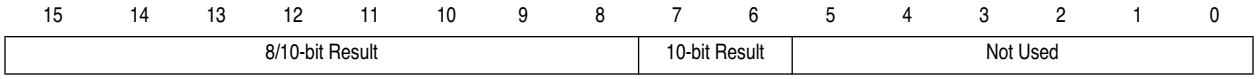
Each bit in this field corresponds to an A/D result register (CCF7 corresponds to RSLT7, etc.). A bit is set when conversion of the corresponding input is complete and is cleared when the result register containing the converted value is read.

RSLT0–RSLT7 — Result Registers (Right-Justified) **$XXXX10–$XXXX1F**



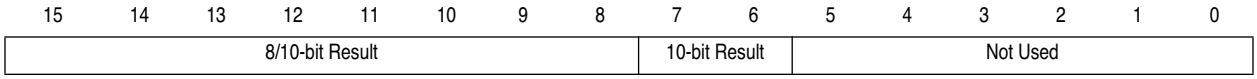
The conversion result is unsigned right-justified data. Bits [9:0] are used for 10-bit resolution, bits [7:0] are used for 8-bit conversion (bits [9:8] are zero). Bits [15:10] always return zero when read.

RSLT0–RSLT7 — Result Registers (Signed Left-Justified) **$XXXX20–$XXXX2F**



The conversion result is signed left-justified data. Bits [15:6] are used for 10-bit resolution, bits [15:8] are used for 8-bit conversion (bits [7:6] are zero). Although the ADC is a unipolar converter, this data format is provided by assuming that the zero reference point is $(V_{RH} - V_{RL}) / 2$. A read of bit 15 returns the inverse of the stored value and indicates the sign of the result. The value read from this register is thus an offset binary twos complement number. Bits [5:0] return zero when read.

RSLT0–RSLT7 — Result Registers (Unsigned Left-Justified) **$XXXX30–$XXXX3F**



The conversion result is unsigned left-justified data. Bits [15:6] are used for 10-bit resolution, bits [15:8] are used for 8-bit conversion (bits [7:6] are zero). Bits [5:0] always return zero when read.