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Motorola Semiconductor Application Note

AN1050

Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers

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Introduction

The operating speed of present high-density complementary metal oxide semiconductor (HCMOS) devices is approaching that of the fastest bipolar logic families of only a few years ago. Associated with this increase in performance ar some new design challenges for the microcontroller unit (MCU)-based system designer. This application note addresses one of these issues, the electromagnetic compatibility (EMC) of the finished product.

EMC may be considered from either an emission or a susceptibility point of view. Although the following discussion relates primarily to emission control (in particular, radiated emission), most techniques to limit emission also reduce susceptibility. Furthermore, minimizing electromagnetic interference (EMI) will reduce overall system noise, the benefits of which are higher digital noise immunity and accurate operation of local analog subsystems (for example, better design margin and a more reliable end product).

EMC can exist only when the system functions correctly within the intended electromagnetic environment and does not exceed the EMI levels specified in the appropriate standards documents. EMI, which encompasses interference in a bandwidth of dc to daylight, is a generalization of a much older term, radio frequency interference (RFI), which is now defined to encompass 10 kHz to 3 GHz. Failure to consider EMC during early phases of the design process may result in expensive modifications (possibly with many additional components), printed circuit board (PCB) re-layout, product introduction delays, and EMC consultant fees to conform to the required standards.

Legal Requirements

The Federal Communications Commission (FCC) has a set of standards to regulate EMI in electronic equipment and systems for use in the United States. Compliance with the appropriate sections of these regulations is mandatory to market or sell a product except for certain subclasses of digital devices that are temporarily exempt. Engineering models (including field-trial prototypes which are not sold) are also exempt; however, the display of a product at an electronics show is considered a marketing function subject to regulations.

FCC rules and regulations (part 15, subpart J of title 47 of *The Federal Regulations*) apply to almost all digital devices (see reference 1), defining standards and operational requirements for all devices capable of emitting radio frequency (RF) energy within the range 450 kHz to 1 GHz.

Equipment for use within West Germany must comply with a different set of standards defined and administered by the Verland Deutcher Electro-Techniker (VDE). Digital equipment is generally required to meet both VDE0871 standards. In other countries, compliance to a standard is not always mandatory; however, the European Economic Community (EEC) member states intend to introduce a mandatory RFI performance standard after January 1, 1992. The current proposal is based on Internal Special Committee on Radio Interference specification CISPR22 and is referred to as European norm EN55022. As the FCC is

a member of the CISPR, and has voted in favor of the CISPR22 standard, it is likely that the FCC will ultimately adopt the same standards. CISPR22 is somewhat more stringent than FCC part 15, subpart J, in the 88-MHz to 230-MHz frequency range, though it is less stringent than some aspects of the VDE0871.

RFI Problem Overview

The frequency spectrum of a periodic waveform has been shown, through Fourier analysis, to be composed of discrete frequency components that include the fundamental (fo) and multiple harmonics (n x fo). For a typical trapezoidal waveform, the relative amplitude of each frequency component is related to the fundamental frequency, the rise time, and mark-to-space ratio (duty cycle) of the waveform (see reference 2). Doubling the frequency, halving the rise time, or halving the mark-to-space ratio will double (+6 dB) the amplitude of a specific harmonic frequency.

It is possible to graphically predict the harmonic spectrum of a specific trapezoidal waveform by plotting the amplitude of two corner frequencies and a reference (0 dB) point. This plot is referred to as a Fourier envelope, a Bode plot, or a nomogram. An example is shown in **Figure 1** where:

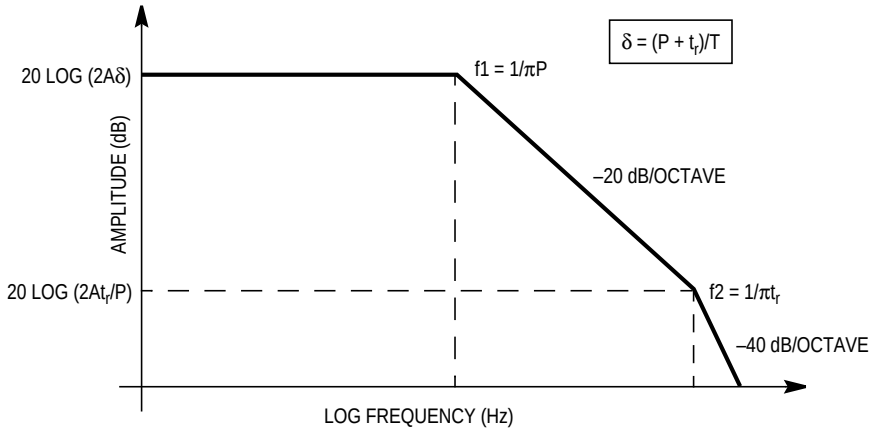
$$0\ \text{dB reference} = 20 \log(2A\delta)\ \text{dB}$$
$$f1 = 1/\pi P\ \text{Hz}$$
$$f2 = 1/\pi t_r\ \text{Hz}$$

where:

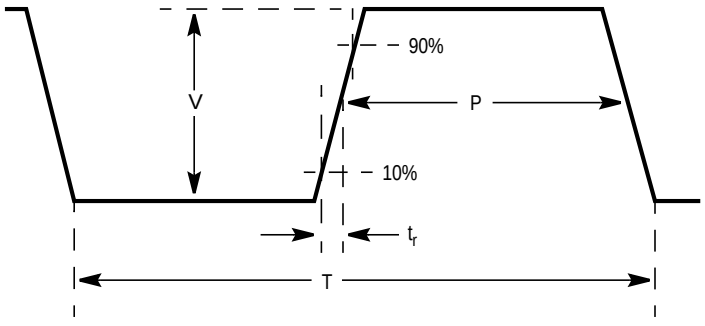
V = amplitude	V
P = pulse width	s
t_r = rise time	s
T = period	s
$\delta = (P + t_r)/T$	

At frequencies beyond f1 ($1/\pi P$), the amplitude of the harmonics falls off at –20 dB/decade. Above f2 ($1/\pi t_r$), the amplitude of the harmonics falls off at –40 dB/decade. For many applications, these latter harmonics are

considered small enough to be ignored; thus, the bandwidth of a system is generally defined to be $1/\pi t_r$. For example, an HCMOS device which can produce an external periodic signal with edge times on the order of 2 ns can generate significant harmonics (for example, have a bandwidth) of up to 160 MHz. Any printed circuit board (PCB) tracks, component leads, cables, or connectors attached directly or capacitively to signal sources, such as those previously described, can act as antennas and radiate the harmonics with varying degrees of efficiency. Radiated emission from a system may be either differential-mode or common-mode radiation; common-mode radiation is typically more difficult to reduce.



(a) Nomogram



(b) Trapezoidal Waveform

Figure 1. Nomogram of a Trapezoidal Waveform

Differential-Mode Radiation

Differential-mode radiation is caused by the flow of RF current loops around the system conductors. For a small loop area, the far-field electric term, when operating in a field above a ground plane (free space is not a typical environment), can be shown to be approximately (see reference 3):

$$E = 2.6\ (A\ I_L f^2)/R \qquad \mu V/m \qquad (1)$$

where:

A = loop area	cm^2
I_L = loop current	A
f = frequency	MHz
R = distance	m

For a constant current and loop area, the electric field at a prescribed distance is proportional to the square of the frequency (for example, it increases at 40 dB/decade). Adding this term to the Fourier envelope indicates that the differential-mode radiated emission increases at 20 dB/decade up to f2, after which it remains flat. R is fixed by both the FCC and VDE rules and regulations, and f is usually not a system variable; however, A and I_L can be reduced through thoughtful board layout and careful circuit design.

Common-Mode Radiation

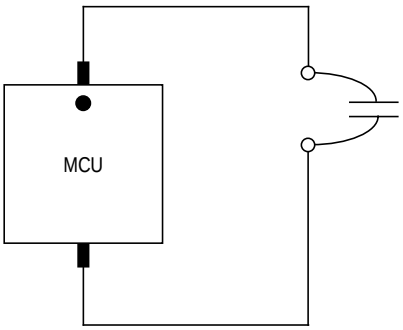
Common-mode (CM) radiation is caused by unintentional voltage drops in a circuit, which cause some grounded parts of the circuit to rise above the real ground potential (see **Figure 2**). Cables connected to the affected ground act like antennas and radiate the components of the CM potential. The far-field electric term can be shown as follows (see reference 3):

$$E \approx (f\ I_{CM}\ L)/R \qquad V/m \qquad (2)$$

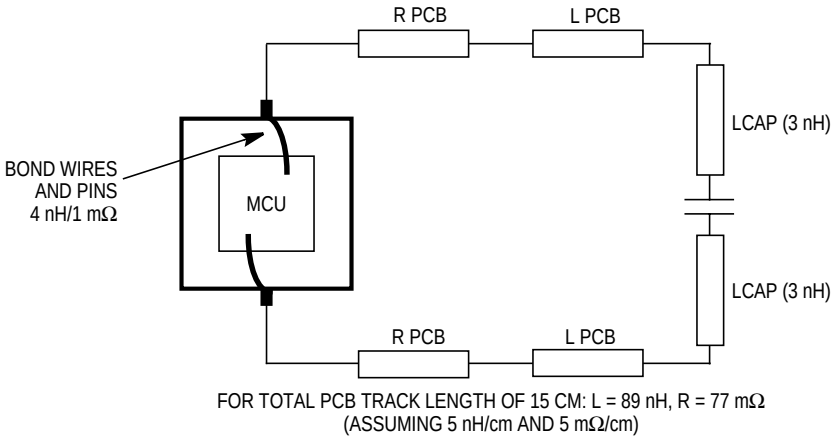
where:

L = antenna length	m
I_{CM} = common-mode current	A
f = frequency	Hz
R = distance	m

For a constant current and antenna length, the electric field at a prescribed distance is proportional to the frequency (for example, it increases at 20 dB/decade). Adding this term to the Fourier envelope indicates that the CM radiated emission remains flat up to f2, then decreases at –20 dB/decade for frequencies above f2. Unlike differential-mode radiation, which is relatively easy to reduce through careful product design, CM radiation is more difficult to control since the only variables available to the designer are typically the common path impedances and CM current. Obviously, to eliminate the radiation, the CM current must approach zero, which can be achieved through a sensible grounding scheme and the addition of inductors or capacitors to increase the cable (antenna) impedance.



(a) Poor Supply Decoupling



(b) Equivalent Circuit of (a)

Figure 2. Printed Circuit Board Layout

Supply Decoupling

Inadequate decoupling decreases system noise margins and ultimately leads to incorrect, unreliable, or unstable operation. For example, the MC68HC11A8 can generate peak supply-current transients of approximately 100 mA, which is typical of an HCMOS microcontroller. Although the average supply current is only a few milliamps, the power supply must be able to source the peak supply-current levels to guarantee correct operation. Also, for fast digital logic, the peak supply-current transients are large enough to create an EMI problem if the decoupling layout is poor.

A decoupling network is used to reduce the supply impedance at the device. To calculate the value of a decoupling capacitor, the acceptable supply ripple must first be determined. An appropriate goal is to achieve a maximum ripple of 20 percent of the minimum noise immunity voltage. For example, for the MC68HC11A8 with V_{DD} = 5 V and no loads:

$$V_{IL}–V_{OL} = (0.2 \times V_{DD}) –0.1 = 0.9 \text{ V}$$
$$V_{OH}–V_{IH} = 4.9 – (0.7 \times V_{DD}) = 1.4 \text{ V}$$

Therefore,

Minimum noise immunity = 0.9 V
Maximum ripple = 0.2 x 0.9 = 180 mV
Transient period = 10 ns

Now,

$C = I_{DD}/(dv/dt)$
$= 100 \text{ mA}/(180 \text{ mV}/10 \text{ ns})$
$= 0.006 \ \mu\text{F}$

Rounding up to the nearest preferred value gives 0.01 μF. When operating the device in expanded mode, the transient currents generated by bus switching can be significantly larger. Consequently, the recommended decoupling configuration is a 1-μF tantalum in parallel with a high frequency 0.01 μF multilayer ceramic (or similar) capacitor. The parallel 0.01-μF capacitor extends the upper frequency response of the network which might otherwise be reduced due to the internal inductance of the 1-μF capacitor. However, with the exception of VLSI devices, decoupling capacitors rarely need to exceed 0.01 μF per

device. It is also recommended to bulk decouple the board at the supply-line entry point with a 10–100 µF capacitor, depending upon the total board-supply requirements. Because it is desirable to prevent unwanted supply noise from going off-board and radiating from the connecting cables, a ferrite bead can be added between the decoupling capacitor and the connector. Care must be taken to ensure that the DC current will not saturate the ferrite, making it ineffective.

For a decoupling network to operate successfully, the impedance between the network and its load must be very low, and, to reduce EMI, its loop area must be as small as possible. Consider the PCB layout of **Figure 2(a)**; the equivalent circuit is shown in **Figure 2(b)**.

For dc current,

$$V_{Drop} = (77) \times 0.1 \text{ mV}$$
$$= 7.7 \text{ mV}$$

For ac current, assuming 100 mA peak current with a minimum rise time of 10 ns,

Total inductance = 89 nH

$V_{Drop} = L \, di/dt$

$= 89 \text{ nH } (100 \text{ mA}/10 \text{ ns})$

$= 890 \text{ mV}$

A drop of 0.9 V between the decoupling network and the MCU exceeds the maximum acceptable ripple, even if the recommended network is used. As shown in this example, for fast current transients containing many high-frequency components, the circuit inductance is by far the most critical factor when considering decoupling effectiveness.

Parasitic loop impedance can be effectively reduced through the use of thicker PCB tracks, ground/supply planes, and more direct routing. Decoupling networks should be located as close as possible to the device supply pins. Surface-mount capacitors, which have lower inductance than their leaded counterparts, may be used to the full advantage as decouplers if mounted on the non-component side of a PCB across a component, which is the closest possible location. Reducing loop impedance also tends to reduce loop area, which has been previously shown (see equation (1)) to be directly proportional to radiated field strength.

Self-Resonance

The inductance and capacitance within the decoupling loop, essentially results in a series-resonant tuned circuit where:

$$\text{resonant frequency, } \mathbf{f} = 1/2\pi\sqrt{LC} \quad \text{Hz} \qquad (3)$$

At frequencies above **f**, the impedance of the circuit becomes inductive and results in a less effective decoupler. At resonance, **f**, the impedance is purely resistive and at a minimum, which can be used to advantage in solving narrow-band RFI problems by tuning suspect decoupling networks to resonate at the problem frequency. For example, to reduce harmonics in the area of 100 MHz (the frequency modulation (FM) radio band) for a total loop inductance of 10 nH, equate equation (3) to 100 MHz and solve for C. In this example, C would equal approximately 250 pF.

Line Termination

A signal will propagate down a PCB track at approximately 0.6 the speed of light (0.6 ft/ns) until it reaches a load. If the line is unterminated (for example, a high-impedance input), then the degree of impedance mismatch between the load and the line will cause a proportional amount of the signal to be reflected back down the line toward the source. These reflections can induce ringing and overshoot, causing significant EMI problems. If the load equals the characteristic impedance of the line, Z_0, then from the viewpoint of the line, the load looks like an infinite line and nothing will be reflected.

In the case of a mismatched line, if the source-signal rise time is sufficiently slow with respect to the line propagation time, then the reflections will be absorbed by the source during the signal rise time. In all other cases, the line should be treated as a transmission line and terminated accordingly (see Reference 3). As a general guide, there should be no need to terminate a line if the one-way propagation delay of a line is less than one-fourth of the signal rise time. For example, for

HCMOS with a rise time of 10 ns, the maximum unterminated line length can be estimated as follows:

$$t_{Delay} < 0.25 \times 10 \text{ ns}$$
$$< 2.5 \text{ ns}$$
$$\text{length} < \text{velocity} \times t_{Delay}$$
$$< 0.6 \times 2.5$$
$$< 1.5 \text{ ft}$$

Therefore, for the majority of cases, termination will not be necessary when using HCMOS devices. Applying the same criteria to Schottky transistor-to-transistor logic (TTL), which has rise times on the order of 3 ns, provides a maximum length of 5.5 inches.

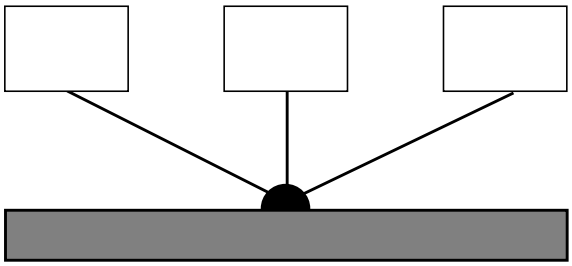
Ferrite Beads

Ferrite beads have excellent high-frequency characteristics and are especially effective in damping high-frequency switching transients or parasitic ringing due to line reflections. Their low impedance (usually below 100 Ω) makes them particularly suitable to filter out supply noise above approximately 1 MHz, preventing the noise from going off-board or into another circuit. However, care must be taken to ensure that the dc current does not saturate the ferrite if it is to be an effective filter. Ferrites having a variety of characteristics are available in many different packages, including surface mount.

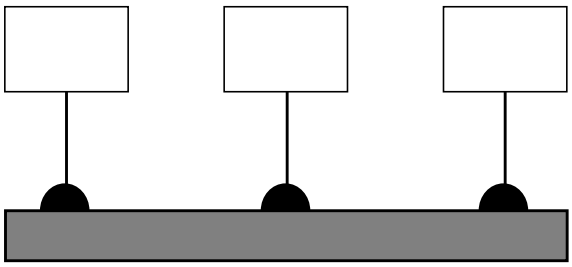
Grounding Techniques

A ground is supposed to be an equipotential point or plane used as a reference potential within a system. In reality, this is untrue due to inevitable parasitic inductance and high ground currents causing significant voltage drops, which can result in common-mode radiation problems. To design a successful grounding scheme, the designer must be aware of the paths that ground currents will take to identify possible common-mode impedance problems, reduce loop areas, and prevent noisy return currents from interfering with low-level circuits.

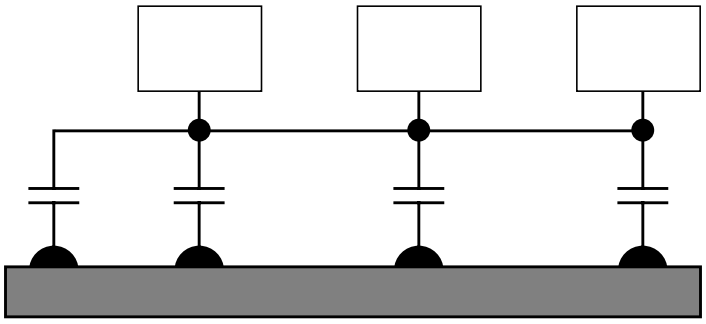
Signal grounds can be classified as single-point, multipoint, or hybrid grounds (see **Figure 3**). Single-point is acceptable for low frequencies but may have too much impedance at higher frequencies to operate correctly. The ground wire length should be kept as short as possible to reduce inductance and radiating ability. A hybrid ground looks like a single-point ground at low frequencies and a multipoint ground at high frequencies. A typical system is often a mixture of grounding techniques.



(a) Single Point



(b) Multipoint



(c) Hybrid

Figure 3. Grounding Techniques

Figure 4 shows a typical MCU application grounding scheme, categorized into low-level analog, digital, input/output (I/O) buffer, high-current switching, and hardware grounds. A single-point ground is located at the source of primary power, which is typically the power supply. The on-board digital logic has a multipoint ground, though it is grounded off-board through a single-point ground. To prevent radiation, no high-frequency components of digital return current should be allowed off-board; thus, the board power supply lines should only carry dc current, which is suitable for single-point grounding. A block diagram, such as the one shown in **Figure 4**, is a useful starting point for the design of a good grounding scheme.

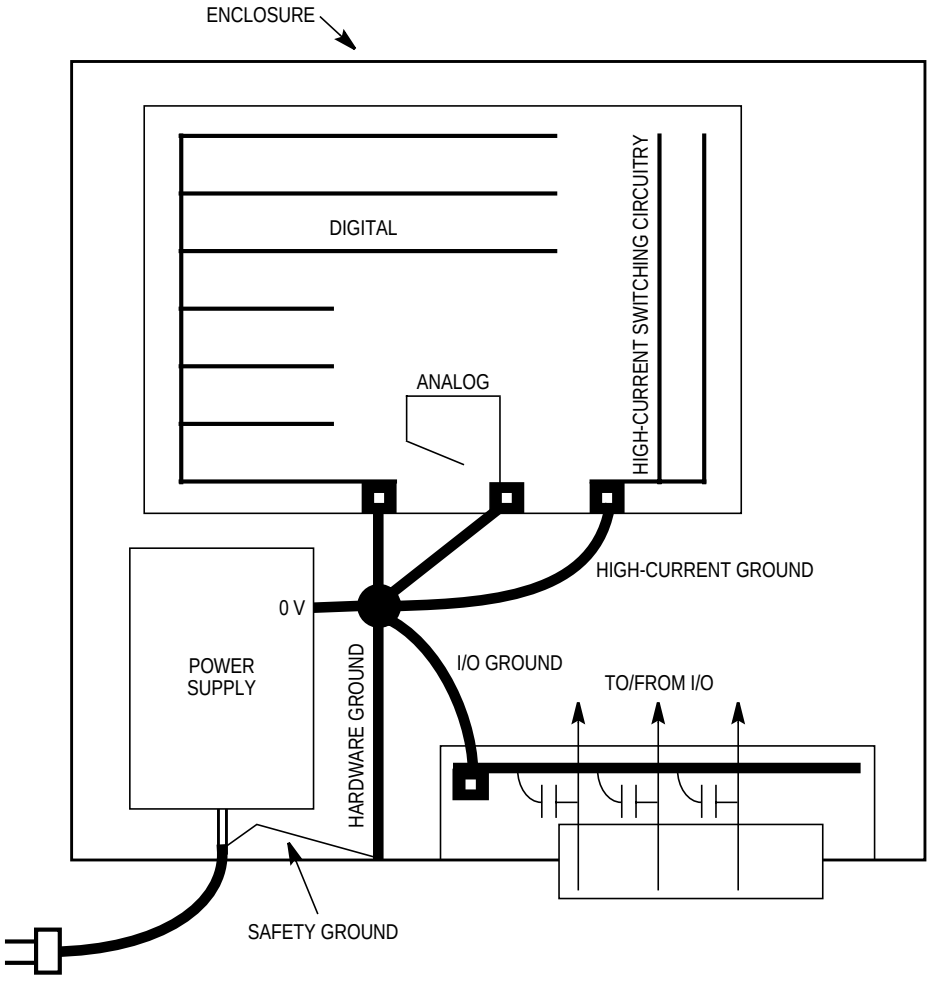
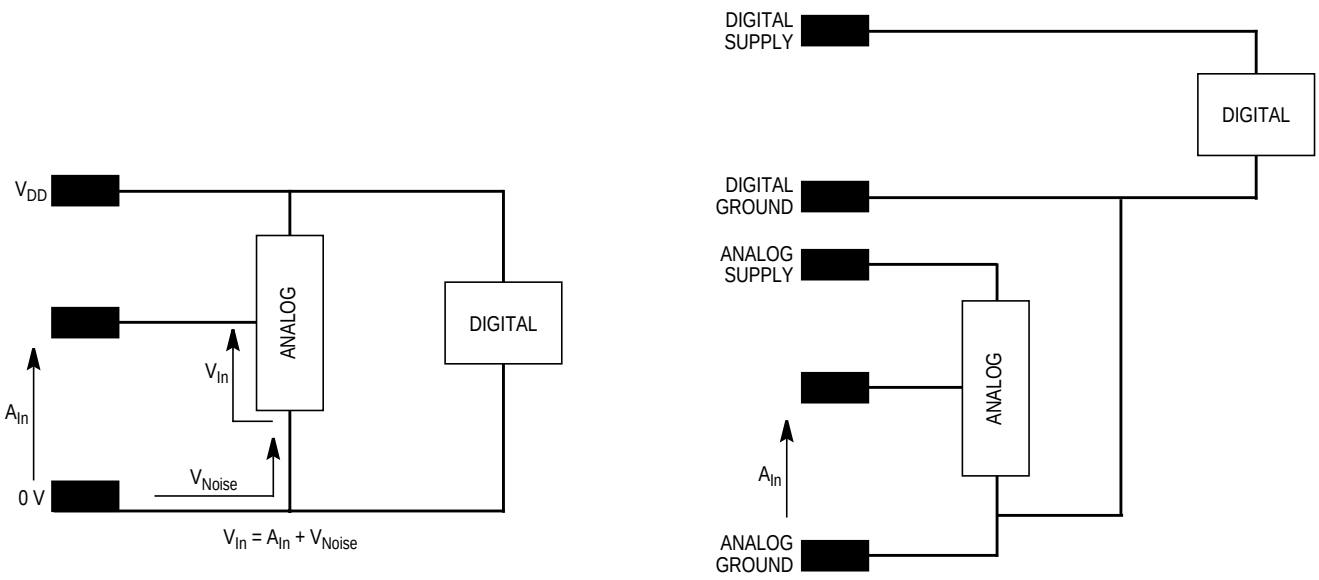


Figure 4. Typical MCU Application Grounding Example

Analog-Digital Mix

Combining analog and digital circuitry onto a single board requires special attention to PCB layout. **Figure 5 (a)** demonstrates how common-mode impedance ground coupling can superimpose noise on an analog input signal. For example, if the analog section were a 12-bit analog-to-digital (A/D) converter, the added digital noise would significantly reduce the achievable accuracy of the measurements, possibly by several bits. In **Figure 5 (a)**, the analog circuit shares its ground and supply with the noisy digital section and is therefore within the digital supply loop. The PCB tracks are also very thin, increasing the parasitic inductance and voltage drop. A better layout of the board is shown in **Figure 5 (b)** in which the digital supply and ground tracks are substantially wider and the analog circuitry is provided with its own supply and ground reference. Any voltage drop occurring on the digital ground track no longer affects the analog input signal because the digital current no longer passes through the analog input loop.

Adequate supply decoupling is also a prerequisite to minimizing noise in an analog subsystem. With regard to the MC68HC11 on-chip A/D



(a) Poor Scheme **(b) Improved Scheme**

Figure 5. Analog Circuit Grounding

converter, the recommended decoupling network for the analog reference inputs is shown in **Figure 6**.

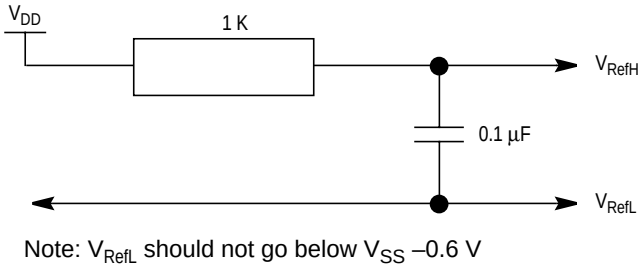


Figure 6. Recommended A/D Reference Voltage Decoupling for the MC68HC11

I/O Cables and Shielding

Providing a low-noise ground for I/O enables I/O shunt filters to be used to remove common-mode voltages from I/O cables that extend beyond the enclosure (see **Figure 4**). In addition, externally shielding I/O cables is ineffective if the termination grounds are themselves noisy. Alternatively, an inductor (choke) may also be used to increase I/O cable impedance and reduce radiation.

Generally, the shield surrounding low-frequency signals should be grounded at one end; for high-frequency signals, at both ends. For example, in **Figure 4** where the analog section is grounded, an input cable shield would be grounded only at the analog circuitry end. Shielded cables carrying digital signals (for example, MC68HC11 serial communications interface (SCI) data) should be grounded at both ends to ensure that the shield be as close as possible to ground potential throughout its length. If this configuration is not practical, the next best configuration is to ground only the signal source end of the shield.

CAUTION: *Grounding at both ends of a long cable can cause large power-frequency ground-loop currents to flow due to potential differences between the shield grounding points. This problem also can be removed through filtering or the addition of a common-mode choke or balun (see reference 3).*

PCB Layout Guidelines

A successful EMI design starts with good board design. As discussed earlier, the two criteria of most concern are signal-path inductance and loop area. The inductance of a flat conductor (for example, a PCB track) about a current-return path is:

$$L = 2\ \mathrm{In}(2\ \pi\ h/w) \qquad \text{nH/cm} \qquad (4)$$

where:

h = height above current-return path
w = track width

Evaluating equation (4) for a height above a current-return path of 1 mm and a track width of 0.5 mm, L = 5.1 nH/cm. The relationship is logarithmic, so doubling the track width will not halve the inductance; however, it will make a significant difference and is always worth doing. For example, doubling the track width to 1 mm makes L = 3.7 nH/cm. A track width of 5 mm makes L = 0.5 nH/cm, which is of the order required for effective decoupling loops and reducing common-mode radiation problems.

Use of a multilayer PCB will provide low-inductance supplies, though at an additional cost. The recommended arrangement is to place the supply and ground planes on the outside, sandwiching the signal lines between them. This arrangement will also provide some shielding. To minimize crosstalk, signals on adjacent layers should be routed perpendicular to each other wherever possible. If a multilayer board is not used, fill all unused area with ground plane; avoid creating ground loops that can cause EMI problems. For example, a ground loop is discovered and subsequently broken with a small gap. This technique is acceptable at dc, but at high frequencies the gap capacitance may effectively close the loop and create a large loop antenna. Apart from the radiation problems, large ground loops can also make a system more susceptible to malfunction when subjected to an electrostatic discharge (for example, through a membrane keypad) or other external EMI source.

Reducing loop area through decoupling and careful layout will reduce RFI. The smaller footprint of surface-mount components can be used advantageously in reducing loop area. For PCBs without a ground plane, signal lines should ideally have a ground-return path as close as possible to them to minimize loop area. In the case of address/data lines, this arrangement may be impractical; thus, routing at least one ground-return track adjacent to each of the eight lines and keeping the lines as short as possible is a good compromise. For the address lines, route the ground return next to A0 (in the case of a word-sized bus, A1), since this line is likely to be the most active. Ground and supply loops with long or thin tracks can be easily identified by tracing them on a printed copy of the PCB artwork using colored marker pens. As previously mentioned, any unused area should be filled with ground plane.

The system clock is often a primary source of radiation. The clock components should be closely grouped, and all clock lines should be as short as possible and have adjacent ground tracks or ground plane. To avoid crosstalk contamination and subsequent radiation problems, the clock circuitry should be located away or shielded from any I/O signal lines or circuitry. For example, mixing clock and I/O buffers in one package is not good practice.

Another source of RFI is an abrupt change of direction of a PCB track which effectively look like impedance discontinuities and will radiate accordingly. For HCMOS designs, it is important to ensure that 90-degree track-direction changes do not occur (see **Figure 7**).

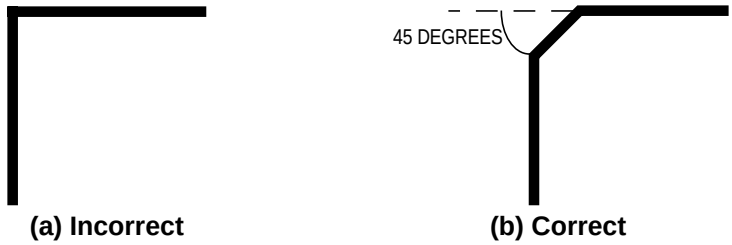


Figure 7. Incorrect (a) and Correct (b) PCB Track Layout for HCMOS Designs

Finally, all unused inputs to HCMOS devices should be terminated to prevent unintentional random switching and noise generation. Also, unterminated CMOS inputs tend to self-bias into the linear region of operation, which can significantly increase dc current drawn. They are also more susceptible to electrostatic discharge damage.

Simple RFI Diagnostic Tool

After applying the previously discussed techniques to attain EMC, if a radiated EMI problem exists, a set of RFI diagnostic tweezers may be used to speed up the identification of potential problem areas on a PCB (see reference 4).

Conclusion

EMI control has left the specialized realms of electronic design (for example, military) and is rapidly becoming an industry-wide phenomenon. Although the application of good system design will always be a prerequisite to achieving EMC, it is reasonable to suppose that similar design concepts could also be applied to the source of most of the radiation, the very large scale integration (VLSI) HCMOS device. To respond to these and other customer demands for higher performance machines, Motorola is investigating new system and circuit design, layout, and alternative packaging techniques. This research may help to reduce the likelihood of problematic RFI when using HCMOS MCU devices; however, the user's awareness and understanding of the problem will remain the most vital step toward product EMC.

Review of Key Points

Differential-mode radiation features are:

1. The system clock is often the primary source of radiation. Avoid ground loops and long tracks (always take the most direct route). Wherever possible, clock tracks (or any other signal) should have adjacent ground-return tracks. Minimize the number of devices requiring the system clock. Ensure that clock circuitry and associated lines are located well away or shielded from PCB I/O tracks or circuitry. Never mix clock and bus or I/O drivers in the same package — use separate buffer drivers for clock and buses.
2. Ensure that decoupling capacitors are as close as possible to the device supply pins to reduce the loop area through the capacitor. Always parallel decouple large-value (dc ballast) capacitors with one or more smaller high-frequency capacitors (check their equivalent series inductance (ESL) and maximum frequency rating).
3. In addition to local device decoupling, decouple the power supply where it enters the PCB. A ferrite bead (for instance, $Z > 50\ \Omega$ at 100 MHz) will also help prevent switching transients from going off-board.
4. For PCBs without a ground plane, minimize address/data line loop areas by routing a minimum of one ground-return track adjacent to each of the eight lines and by keeping the lines as short as possible. For the address lines, route the ground return next to A0 because this line is likely to be the most active. Note also that long address lines will ring, which is another potential source of RFI. These lines may need to be individually terminated (see Reference 5). Operating an MCU in single-chip mode will almost eliminate radiation from address/data lines (still exists internally, of course).
5. Avoid ground loops. Remember that breaking a loop with a small gap may be fine at dc but gap capacitance may effectively close the loop at RF frequencies, creating a large loop antenna. Apart from the radiation problems, large ground loops can make a

system more susceptible to malfunction when subjected to external EMI sources.

6. Using a printed copy of the PCB artwork and a marker pen, trace the ground and supply tracks. Long, thin, or looped tracks can then be easily identified and subsequently modified.
7. Terminate all unused inputs to prevent unintentional random switching and noise generation (in addition, unterminated CMOS inputs tend to self-bias into the linear region of operation, significantly increasing the dc current drawn).
8. The smaller footprint of surface-mount components may be used advantageously to reduce loop areas.

Common-mode radiation features are:

1. Ensure a good ground plane and choose the external ground connection to minimize the overall common-mode voltage drop (see reference 5). Increase both supply and return-supply track widths (as a general rule, cover as much as possible of the unused part of a PCB).
2. A grounding scheme that isolates digital and I/O (including any analog sections) reduces radiation from I/O cables. Shielding these cables is ineffective if the shield termination grounds are noisy. In digital systems, the shield should be connected to noise-free grounds at both ends. If this configuration is not possible, then ground only the source end.
3. A choke may be effective in reducing the radiation from an I/O cable. Also available are a variety of other passive RFI filter elements which shunt the common-mode current to ground. The effectiveness of these devices will depend upon the condition of the shunt ground.

References

1. FCC. “Understanding the FCC Regulations Concerning Computing Devices.” *OST Bulletin*, vol. 62, 1984.
2. Mardiguian, Michel. *Interference Control in Computers and MPU-Based Equipment*, Gainesville, VA: Don White Consultants Inc., 1984.
3. Ott, Henry W. *Noise Reduction in Electronic Systems*. 2nd Edition. New York: Wiley Interscience, 1988.
4. Ott, Henry W. “Digital Circuit Grounding and Interconnection,” *IEEE International Symposium on Electromagnetic Compatibility*, August 1984.
5. Moriarty, Frank. “EMI/RFI Diagnostic Tweezer Probes: A Construction Article.” *EMC Technology*, vol. 7, no. 7, November-December 1988.

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