

Motorola Semiconductor Engineering Bulletin

EB180

Differences between the MC68HC705B16 and the MC68HC705B16N

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Introduction

Motorola is introducing a new version of the MC68HC705B16. Since the old and the new versions have several differences, the new device has been named the MC68HC705B16N to avoid confusion. This bulletin summarises the differences between the two devices. Both devices are fully covered in Revision 4 of the *MC68HC05B6 Family Technical Data Book* (MC68HC05B6/D).

There are five differences between the MC68HC705B16 and the MC68HC705B16N relating to the:

1. Bootloader
2. Reset pulse width
3. Reset twice issue
4. Stop I_{DD}
5. Shrink level



Bootloader

To provide compatibility with the rest of the B Family and to enhance the diagnostic capabilities of the device, a new bootloader has been incorporated into the 705B16N.

As in the original part, the different bootloader modes are entered with the $\overline{\text{IRQ}}$ pin at 9 V, the TCAP pin at V_{DD} , and pins 1–4 on port D configured to select a particular mode.

The differences between the combinations for the 705B16 and the 705B16N are summarised in **Table 1** and **Table 2**.

The MC68HC705B16 has the bootloader options shown in **Table 1**.

Table 1. M68HC705B16 Bootloader Options

JP3	—	JP7	JP4	Configuration jumper on Motorola B programmer board
PD1	PD2	PD3	PD4	Mode
0	0	X	0	Erased EPROM verification
1	0	0	0	Erased EPROM verification; EEPROM erase and verify; EPROM/EEPROM parallel program and verify
1	0	1	0	(+) Erased EPROM verification; Erase EEPROM; EPROM/EEPROM/RAM serial bootstrap load and execute
X	X	0	1	RAM parallel bootstrap load and execute (SEC bit non-active)
X	X	1	1	(+) Serial EPROM/EEPROM/RAM bootloader (SEC bit non-active)

X = Don't Care

The MC68HC705B16N has the bootloader options shown in **Table 2**.

Table 2. M68HC705B16N Bootloader Options

JP3	—	JP7	JP4	Configuration jumper on Motorola B programmer board
PD1	PD2	PD3	PD4	Mode
0	0	0	0	Erased EPROM verification
0	0	1	0	(*) Parallel EPROM verify
1	0	0	0	Erased EPROM verification; EEPROM erase and verify; EPROM/EEPROM parallel program and verify
1	0	1	0	(*) Erased EPROM verification; EEPROM erase and verify; Parallel EPROM program and verify
1	0	0	1	(*) Jump to start of RAM (\$0051) (SEC bit non-active)
X	0	1	1	Serial RAM load and execute — similar to M68HC05B6, but can fill RAM 1 and 2

X = Don't care

As seen in **Table 2**, the RAM parallel bootstrap load and execute has been removed on the 705B16N, but three extra options have been added, denoted by (*).

The options marked (+) on **Table 1** for the 705B16 are now implemented using the serial RAM load and execute option together with the new PC software for serially programming the device. This programming software is called PRO7B16N.EXE and it provides the following options:

1. Blank EPROM check
2. Erase EEPROM
3. Blank EEPROM check
4. Read memory
5. Program EPROM
6. Program EEPROM
7. Verify S-record against MCU memory

Serial RAM load and execute on the 705B16N is now similar to that function on the rest of the B Family, except for the 705B5. For example, user programs are loaded into the MCU RAM via the SCI port and then executed. Data is loaded sequentially, starting at RAM location \$0050, until the last byte is loaded. Program control is then transferred to the RAM program starting at location \$0051. The first byte loaded is the count of the total number of bytes in the program plus the count byte.

If the customer has a Motorola B programmer board, the marking on jumper 7 (JP7), parallel and serial, does not always coincide with the bootloader mode chosen, on the 705B16N.

As can be seen from **Table 1** and **Table 2**, JP7 on the B programmer board is connected to PD3, and, on the 705B16 this port pin was high in serial mode and low in parallel mode. However, on the 705B16N, because the new device offers more bootloader options than its predecessor, PD1, PD3, and PD4 have to be manipulated more extensively, so PD3 is now not always high in serial mode and not always low in parallel mode.

To lessen confusion, on future versions of the programmer board and in documentation for the board, the words parallel and serial on JP7 will be replaced with position 1 and position 2.

Reset twice issue

On the 705B16, a bug necessitated resetting the device a second time after power-on. The easiest way to do this in software was by using the watchdog. Adding this subroutine was recommended:

```
RESET2      BSET 0,$0C      Start watchdog
             STOP          STOP causes immediate watchdog reset
```

The interrupt vector at \$3FF0 and \$3FF1 must be initialised with the RESET2 address value.

On the 705B16N, this reset twice action is now NOT required because the device does not need to be reset a second time after power-on. The interrupt service routine for the vector at address \$3FF0–\$3FF1 is no longer required, as that vector will never be fetched. However, the interrupt service routine and vector contents required for the 705B16 can be kept on the 705B16N with no detrimental effect, even though they will never be used.

Reset pulse width

The minimum reset pulse width has been changed on the 705B16N. The 705B16N requires a logic zero to be applied to the RESET input for a minimum of $3.0 t_{CYC}$, while the 705B16 requires a logic zero for a minimum of $1.5 t_{CYC}$.

Stop I_{DD}

On the 705B16N, the supply current in stop mode for automotive temperature range devices ($-40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$) has a maximum value of $100\text{ }\mu\text{A}$ at 5 V . At 3.3 V , this value is $60\text{ }\mu\text{A}$. This change affects only part numbers:

MC68HC705B16NMFN
MC68HC705B16NFU
MC68HC705B16NMB

The stop I_{DD} specification for all other temperature ranges remains the same.

Shrink level

The 705B16N is manufactured at a higher shrink level than the 705B16. While the electrical and functional specifications of the device remain unchanged, other than the differences mentioned in this document, it has been found that, in similar situations in the past, a very small percentage of customer applications can experience noise susceptibility problems with higher shrink devices.


This is because the smaller transistor size results in a faster device that can react to noise pulses that were not seen by the older technology part. Sensible application design guidelines should minimise the noise presented to the MCU.

Three application notes designed to help customers develop good EMC behaviour into their applications are available. To obtain these documents refer to **How to reach us:** at the bottom of this page. The Motorola document numbers are:

Designing for Electromagnetic Compatibility with Single-Chip MCUs (AN1263/D),

Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers (AN1050/D), and

System Design and Layout Techniques for Noise Reduction in MCU-Based Systems (AN1259/D).

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