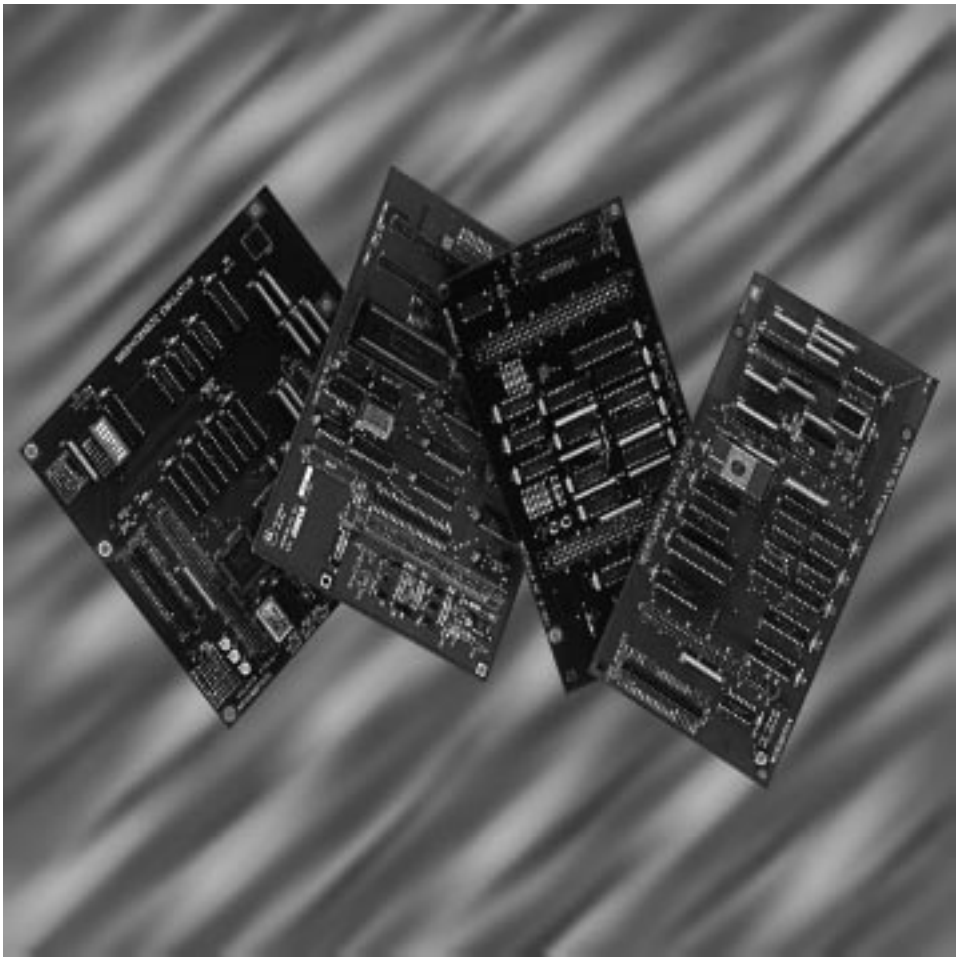
M68EM05C9A

EMULATION MODULE
USER'S MANUAL



MOTOROLA

M68EM05C9A

Emulation Module
User's Manual

Revision History

This table summarizes differences between this revision and the previous revision of this emulation module user's manual.

Previous Revision	None
Current Revision	Original release
Date	08/96

Revision History

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Introduction

Your M68EM05C9A gives your Motorola development tool the ability to emulate target systems based on MC68HC(7)05C*x*A microcontroller units (MCUs). Current members of this MCU family are the C*4*A, C*8*A, C*9*A and C*12*A. The M68EM05C9A is designed to operate at 5.0 Vdc at maximum rated frequencies per the specification.

By substituting a different emulation module (EM), you can enable your Motorola development tool to emulate other MCUs. Refer to *Motorola's Development Tool Selector Guide*, Motorola order number SG173/D, for a complete list of available EMs.

This hardware user's manual explains connection, configuration, and operation information specific to the M68EM05C9A emulation module. The module can be installed in two Motorola development systems. To configure your M68EM05C9A for either an MMDS or an MMEVS, follow the instructions given in MMDS/MMEVS Configuration and Operation on page 19.

Emulation Components

Motorola’s complete emulation system consists of the emulation module described in this manual as well as other separately purchased options described in the following paragraphs.

The following items are included with the M68EM05C9A emulation module:

- **An M68EM05C9A emulation module (EM)** — the printed circuit board that enables system functionality for MC68HC(7)05CxA MCUs. The female connectors, on the bottom of the module, mate with male connectors on a development system platform board. The EM also has a connector for the target cable assembly.
- **Configuration software** — 3 1/2-inch diskette containing personality files for this module.

Separately purchased Motorola modular development tool options include:

- **An MMEVS platform board (M68MMPFB0508)** — The MMEVS is an economical development tool that provides real-time in-circuit emulation. The unit's integrated design environment includes an editor, an assembler, a user interface, and a source-level debugging program.
- **An MMDS0508 modular development system (MMDS0508)** — The MMDS is a high-performance development tool that has all the capabilities of the MMEVS. In addition, it also has a bus state analyzer and real-time memory windows.
- **Flex cable target assembly** — Refer to Target Cable Assemblies on page 13 for more information.

User supplied components include:

- **Host computer** — see the appropriate development tool user’s manual for minimum requirements.
- **Power supply** — +5 Vdc @ 1.0 amp required for the MMEVS.

Emulation Module Layout

Figure 1 shows the layout of the M68EM05C9A. . Jumper J1 allows the selection of either Cx or CxA emulation (e.g. C4 vs C4A, C12A). Jumper headers J2 and J3 let the user select the clock source. Jumper J4 determines the logic direction of the RESET signal at the target connector. Switch array S1 determines which device is to be emulated. Switch array S2 allows the user to set the port B mask option for CxA devices.

Connector P1 connects to a logic analyzer. Target connectors P4 and P5 provide the interface to a target system. These connectors use a separately purchased target cable assembly. When you install the M68EM05C9A on the MMDS05, the target cable passes through the slit in the station module enclosure.

Variable resistor, VR1, controls MCU operating voltage between 3.0 V and 5.0 V. Test point header TP1 is the monitor point for MCU operating voltage. The MC68HC708XL36 MCU is at location XU1.

DIN connectors P2 and P3 connect the EM and a development system platform board.

Emulation Module Layout

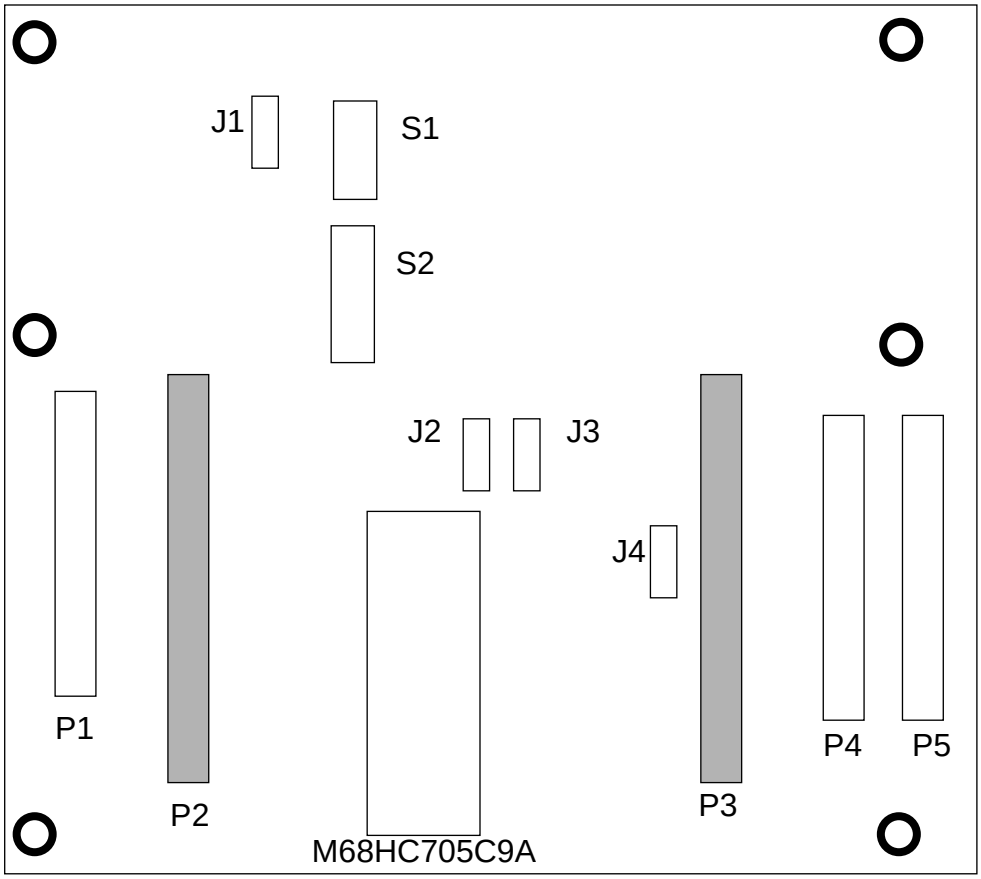


Figure 1. M68EM05C9A Emulation Module

Target Cable Assemblies

To connect your M68EM05C9A to a target system, you need a separately purchased target cable assembly. Cable assemblies are available for the 40-PIN DIP, 44-PIN PLCC, 44-pin QFP, and 42-pin SDIP MCU packages.

The target cable connects to the emulator via connector P4 and P5 on the M68EM05C9A emulation module. Pin assignments and signal descriptions for connectors P4 and P5 can be found in Target Cable Connector Pin Assignments on page 17.

Figure 2 represents a target cable assembly. An assembly for 40-pin DIP package consists of a flex cable and a DIP target head adapter. An assembly for 44-pin PLCC package consists of a flex cable and a PLCC target head adapter. An assembly for 44-pin QFP package consists of a flex cable and a QFP target head adapter. The assembly for 42-pin SDIP consists of a flex cable and a SDIP target head adapter. One end of the flex cable plugs onto M68EM05C9A connector P4 and P5 with orientation shown in **Figure 2**. The other end of the flex cable plugs into the target head adapter. The 44-pin QFP target head adapter then inserts into a TQSOCKET and then a TQPACK installed on the users target system. The 42-pin SDIP target head adapter inserts into a SDIP footprint in a target system.

The MCU package in your target system determines the target cable assembly components required:

- For a 40-pin DIP package, use flex cable M68CBL05B and target head adapter M68TB05C9P40.
- For a 44-pin PLCC package, use flex cable M68CBL05C and target head adapter M68TC05C4FN44 or M68TC05C9FN44 (C9(A) only).
- For a 44-pin QFP package, use flex cable M68CBL05C and target head adapter M68TC05C9FU64. A TQSOCKET w/guides and a TQPACK are included with the flex cable assembly.
- For a 42-pin SDIP package, use flex cable M68CBL05B and target head adapter M68TB05C9B42.

Target Cable Assemblies

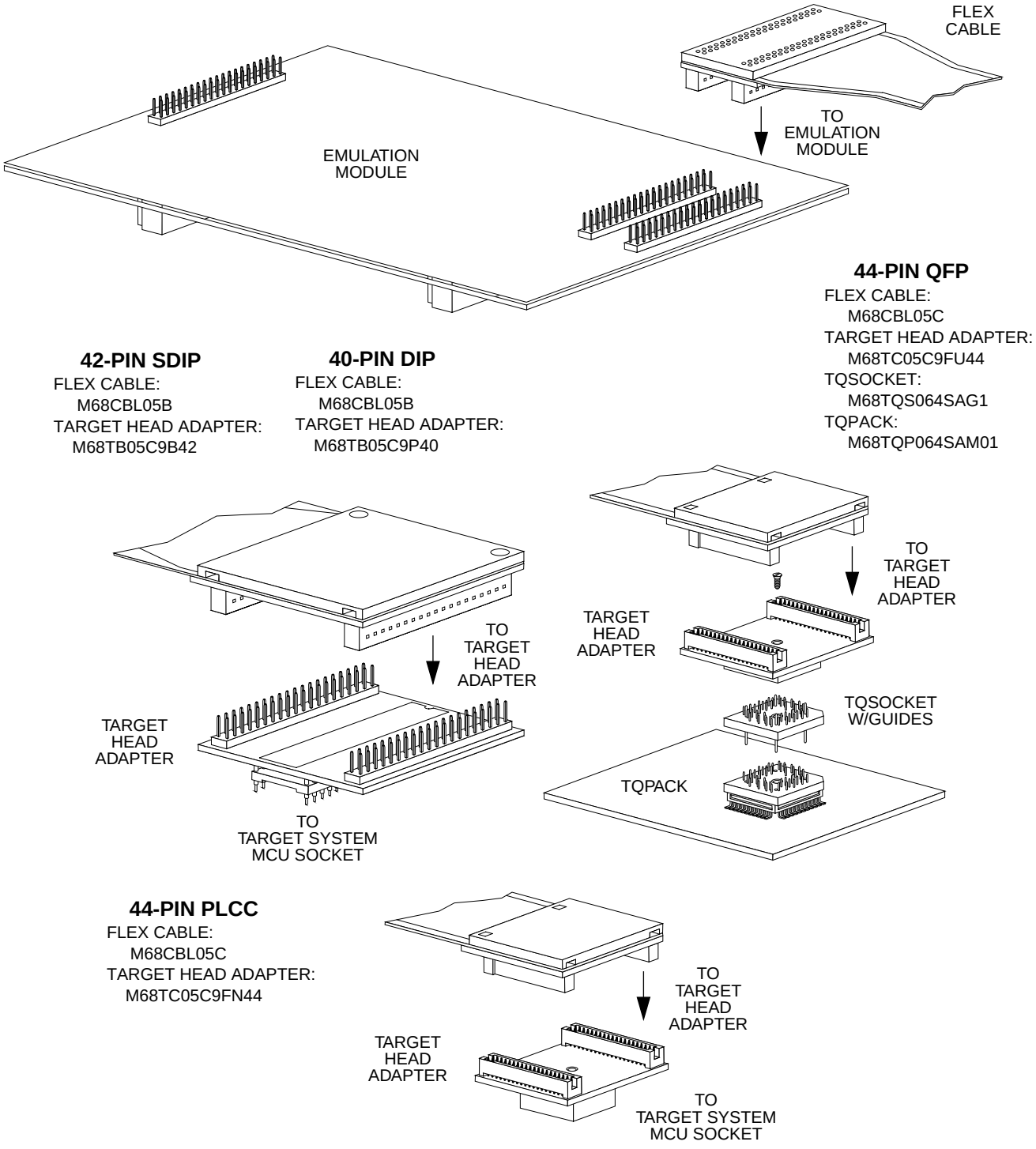


Figure 2. Target Cable Assembly

Connector Information

The connectors on the M68EM05C9A module provide access to the user mode emulation signals (P4 and P5) as well as select internal signals (P1). Connector P1 is used to connect to a logic analyzer. Connectors P4 and P5 are used for a cable interface to a user's target system.

Logic Analyzer Connector Pin Assignments

Figure 3 shows the pin assignments for logic analyzer connector P1. This connector provides the emulator easy access to many of the signals used internally. **Table 1** lists signal descriptions for this connector.

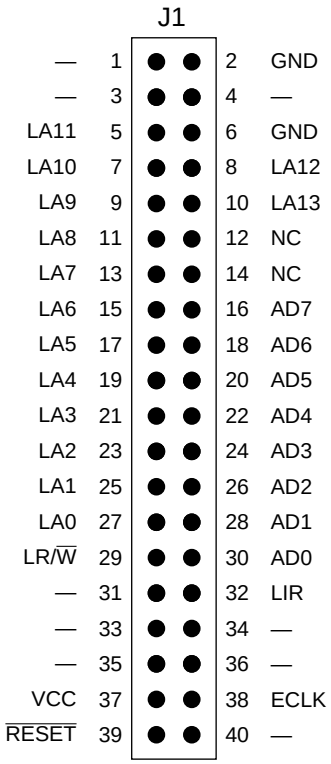


Figure 3. Connector P1 Pin Assignments

Table 1. Logic Analyzer Connector P1 Signal Descriptions

Pin	Mnemonic	Signal
1, 3, 4, 31, 33, 34,35, 36, 40	NC	NO CONNECTS.
2, 6	GND	GROUND.
8, 10	LA12–LA13	LATCHED ADDRESS (bits 12–13) — MCU latched address bus.
5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27	LA11–LA0	LATCHED ADDRESSES (bits 11–0) — MCU latched address bus.
16, 18, 20, 22, 24, 26, 28, 30	AD7–AD0	DATA BUS (bits 7–0) — MCU multiplexed I/O bus.
29	LR/$\overline{W}$	LATCHED READ/WRITE — The MCU's write signal is latched and used on the emulator to control emulator memory accesses.
32	$\overline{LIR}$	LOAD INSTRUCTION REGISTER — Active low signal indicating an opcode fetch cycle is in process.
37	V_{CC}	+5 Vdc POWER — Connection to the system voltage V_{CC}.
38	ECLK	ANALYZER CLOCK — The latched addresses are valid on the latched address bus at the falling edge of ECLK. Also, data is valid on the AD BUS at ECLK falling edge.
39	$\overline{RESET}$	RESET — Active-low signal; will be asserted during internally or externally caused resets.

Target Cable Connector Pin Assignments

Figure 4 shows the pin assignments for connector P4 and P5. **Table 2** lists signal descriptions for connector P4. **Table 3** lists signal descriptions for connector P5.

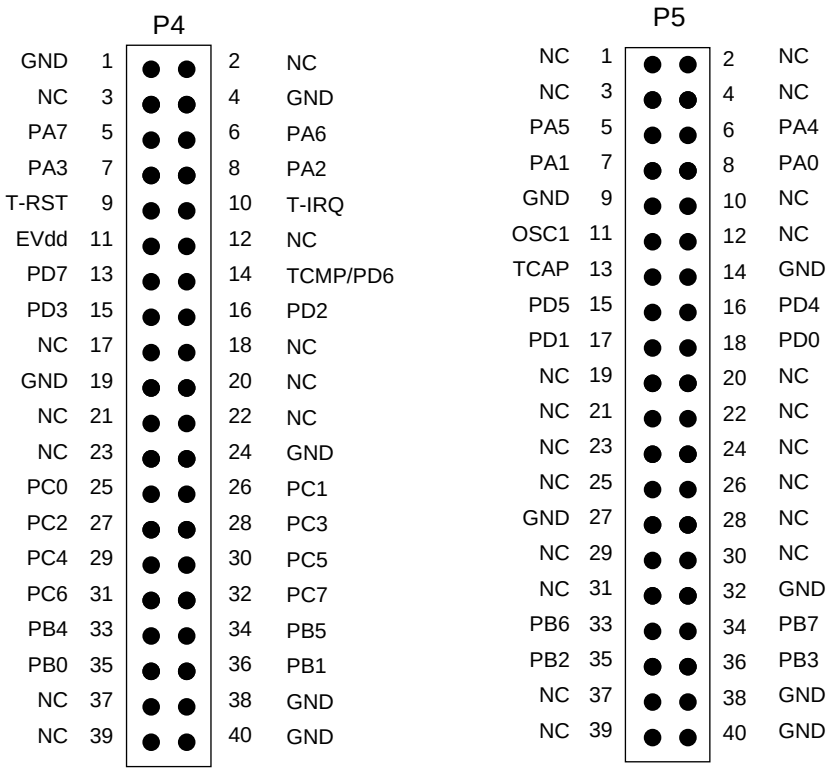


Figure 4. Target Connector Pin Assignments

Table 2. Connector P4 Signal Descriptions

Pin	Mnemonic	Signal
1, 4, 19, 24, 38, 40	GND	GROUND.
5–8	PA7, PA6, PA3, PA2	PORT A (bits 7, 6,3,2) — General-purpose I/O lines controlled by software via data direction and data registers.
9	T-RST	TARGET RESET — Active-low signal to the target system driven low to pull the MCU into reset.
10	T-IRQ	TARGET INTERRUPT REQUEST — Active-low input signal from the target that asynchronously applies an MCU interrupt.
11	EVDD	Vdd input detector — used to determine when power is applied to the MCU on the target system.
2, 3, 12, 17, 18, 20—23, 37, 39	NC	NO CONNECTS.
13—16	PD7, PD6, PD3, PD2	PORT D (bits 7, 6,3, 2) — General-purpose I/O lines controlled by software via data direction and data registers.
25—32	PC0—PC7	PORT C (bits 0—7) — General-purpose I/O lines controlled by software via data direction and data registers.
33—36	PB4, PB5, PB0, PB1	PORT B (bits 4, 5, 0, 1) — General-purpose I/O lines controlled by software via data direction and data registers.

Table 3. Connector P5 Signal Descriptions

Pin	Mnemonic	Signal
5–8	PA5, PA4, PA1, PA0	PORT A (bits 5, 4, 1, 0) — General-purpose I/O lines controlled by software via data direction and data registers.
1–4, 10,12, 19–26, 28–31, 37, 39	NC	NO CONNECTS.
9, 14, 27, 32, 38, 40	GND	GROUND.
11	OSC1	Oscillator input — Target input clock for the MCU.
13	TCAP	Timer CAPture — input pin to the MCU timer capture system
15—18	PD5, PD4, PD1, PD0	PORT D (bits 5, 4, 1, 0) — General-purpose I/O lines controlled by software via data direction and data registers.
33—36	PB6, PB7, PB2, PB3	PORT B (bits 6, 7, 2, 3) — General-purpose I/O lines controlled by software via data direction and data registers.

MMDS/MMEVS Configuration and Operation

Contents

Introduction

The following paragraphs explain how to configure and use your M68EM05C9A as part of an MMDS or MMEVS system. For other parts of system installation and configuration, see either the *MMDS0508 Operations Manual* (MMDS05OM/D) or *MMEVS05/MMEVS08 Operations Manual* (MMEVS0508OM/D).

The topics covered in this chapter are:

- Setting M68EM05C9A Jumper Headers on page 21 explains how to set the M68EM05C9A jumper headers.
- Port B Keyboard Interrupt Mask option, switch array S2 on page 25 covers the final steps to system installation.
- Personality File Usage on page 27 discusses the personality file used on the M68EM05C9A board.
- Resident MCU Substitution on page 28 explains special considerations for emulating with this module.

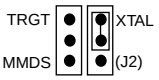
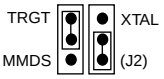
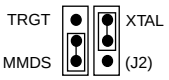
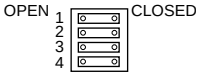
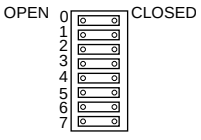
NOTE: *You can configure an M68EM05C9A already installed in the system platform board. To do so, remove system power and then follow the guidance of this chapter.*

CAUTION: *Be sure to switch off power before you reconfigure an installed EM. Reconfigure EM jumper headers with the power on can damage emulation circuits.*

Setting M68EM05C9A Jumper Headers

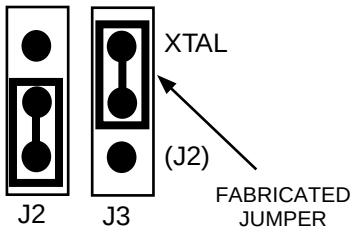
Your M68EM05C9A has four jumper headers, J1 through J4 and two switch arrays S1 and S2. The following table provides a quick reference for configuration options. Refer to the paragraphs that follow for a more detailed explanation.

Table 1. Jumper Header Positions for MMDS/MMEVS

Jumper	Position	Description	Factory Setting
CxA Enable J1		Disable the CxA MCU features	X
		Enable the CxA MCU features	
Clock Source Select, J2 and J3		Select the 4 MHz canned oscillator located on the EM board.	X
		Selects a user supplied oscillator clock as the MCU clock source.	
		Select the clock originating from the development system platform board. The frequency is controlled by the OSC command and is 4 MHz on power up.	
Reset Selection J4		Enable the MCU RESET operation.	X
S1		Selects the specific MCU device supported by the emulator	
S2		Configures port B keyboard interrupt function	

Clock Source Select Headers, J2 and J3

Jumper headers J2 and J3 determine the clock-signal source. You may choose between on-board oscillator (EM), MMDS supplied oscillator (MMDS) or clock from the target system (TRGT). To select MMDS you must place the J3 jumper at the (J2) position as well as correctly selecting the J2 setting. The diagram below shows the factory configuration: the fabricated jumper on J3 between pins 1 and 2 selects the C9EM on-board canned oscillator clock source.

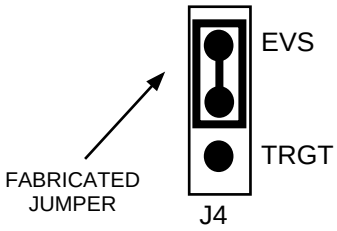


There are two other possible clock sources. To use the one originating from the development system platform, reposition the J3 jumper header to the (J2) pin. Then use the system's OSC command to select a frequency.

To use a clock source originating from the target system position the J3 jumper header to the (J2) pin, then position the J2 jumper header to the TRGT pin.

Reset Select Header , J4

Jumper header J4 controls the path of a target reset. The diagram below shows the factory configuration: the fabricated jumper at EVS enables your software to control resets. This is the only correct J4 configuration for a C9AEM that is part of an MMDS05.



CAUTION: *The J4TRGT configuration is not correct for a C9AEM that is part of an MMDS05 or MMEVS system. Such a configuration would interfere with correct operation of the RESETIN and RESETOUT commands.*

Emulation Device Selection, jumper header J1 and switch array S1

Switch array S1 and jumper header J1 together allow the user to determine the MCU which is to be emulated. S1 is used to select the size of the memory map available to the MCU and also some device specific features. J1 determines whether the keyboard interrupt function is active. **Table 2** shows the settings of S1 and J1 which are required for each MCU emulated. See **Personality File Usage** on page 27 for more information on device selection. Note that devices in italics have been or will soon be replaced and are present for historical reasons only.

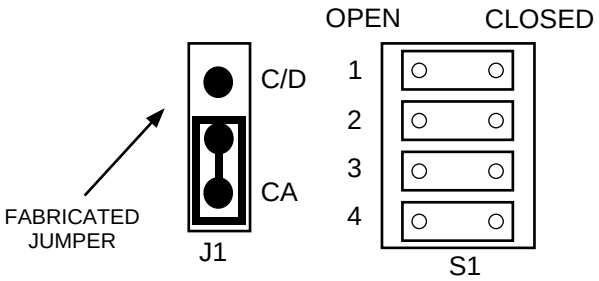
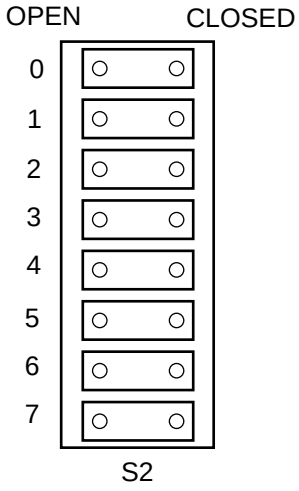


Table 2 MCUs Emulation Selection

DEVICE	S1 SWITCH	S2 SWITCH	S3 SWITCH	S4 SWITCH	J1 SETTING	
	1	2	3	4	C/D	CA
MC68HC(8)05C4	*CLOSED*	*CLOSED*	*CLOSED*	*OPEN*	*ON*	
MC68HC05C8	*CLOSED*	*CLOSED*	*CLOSED*	*OPEN*	*ON*	
MC68HC705C8	*OPEN*	*CLOSED*	*CLOSED*	*OPEN*	*ON*	
MC68HC(7)05C9	*CLOSED*	*OPEN*	*CLOSED*	*OPEN*	*ON*	
MC68HC(7)05C4A	CLOSED	CLOSED	CLOSED	OPEN		ON
MC68HC05C8A	CLOSED	CLOSED	CLOSED	OPEN		ON
MC68HC05C8A	OPEN	CLOSED	CLOSED	OPEN		ON
MC68HC(7)05C9	CLOSED	OPEN	CLOSED	OPEN		ON
MC68HC05C12A	CLOSED	OPEN	CLOSED	OPEN		ON

Port B Keyboard Interrupt Mask option, switch array S2

Switch array S2 selects which bits in port B have the keyboard interrupt function active for CxA type devices. (The switch S2 settings should match the port B mask option settings that you require for the device; in the 705C8A this is set up in register MOR1.) The bits selected are only active when programmed as inputs using the port B data direction register, in such cases a resistive pull up is activated on the bit in question. To enable the mask option for the keyboard interrupt bit, close the relevant switch in S2 and ensure that jumper J1 selects the CA option. Switch array S2 is organised as follows:



Remaining System Installation

When you have configured headers J1 through J4 and S1 and S2, M68EM05C9A configuration is complete:

- Ensure that the power to the development tool is off.
- If installing the M68EM05C9A in an MMDS station module, remove the panel from the station module top.
- Fit together EM connectors P2 and P3 (on the bottom of the board) and platform board DIN connectors. Snap the corners of the EM onto the plastic standoffs.
- Connect the target cable, if appropriate.
- If installing in an MMDS05, replace the panel.

At this point, you are ready to make remaining cable connections, as necessary, and restore power.

For instructions, consult either the *MMEVS05/MMEVS08 Operations Manual* (MMEVS0508OM/D) or the *MMDS0508 Operations Manual* (MMDS0508OM/D).

Personality File Usage

Your development system uses a specific personality file for the MCU type being emulated. For example, to emulate an MC68HC(7)05C9A MCU, the system uses the personality file 0021AVxx.MEM. Debugger software loads this personality file upon power up.

NOTE: *Personality file names follow the pattern 00ZZZVxx.MEM, where ZZZ is the EM identifier or MCU name and xx is the version of the file*

See Table 3 for a full list of the MCU devices supported by the M68EM05C9A emulator.

NOTE: *The devices shown in italics have been or will soon be replaced and are present for historical reasons only.*

Table 3 MCUs and Personality Files

EMULATED MCU	PERSONALITY FILE	COMMENTS
MC68HC(8)05C4	*00C4_V01.MEM*	
MC68HC05C8	*00218V01.MEM*	
MC68HC705C8	*00219V01.MEM*	
MC68HC(7)05C9	*0021AV01.MEM*	
MC68HC(7)05C4A	00C4_V01.MEM	See **Resident MCU Substitution** and **MC68HC(7)05C4A Emulation**
MC68HC05C8A	00218V01.MEM	See **Resident MCU Substitution** and **MC68HC05C8A Emulation**
MC68HC705C8A	00219V01.MEM	See **Resident MCU Substitution** and **MC68HC705C8A Emulation**
MC68HC(7)05C9A	0021AV01.MEM	See **MC68HC(7)05C9A Emulation**
MC68HC05C12A	00C12V01.MEM	See **Resident MCU Substitution** and **MC68HC05C12A Emulation**

Resident MCU Substitution

The socket at M68EM05C9A location U9 contains the resident MCU. The factory ships the M68EM05C9A with an MC68HC705C9A resident MCU, which is appropriate for emulating a number of MCUs with some qualifications as described in the following paragraphs.

Occasionally it may be necessary to replace the resident MCU with another to improve the level of emulation of a particular feature.

When you are ready to install the substitute MCU, turn off MMDS05 or MMEVS power and make sure that you are grounded. Then remove the MCU from M68EM05C9A location U9, insert the new resident MCU, and restore power.

Generic Emulation Considerations

Since the emulator uses common hardware to emulate several different devices there are common emulation issues that arise for the devices. These are listed below.

Pullup on $\overline{IRQ}$

In single-chip mode operation:

There is no pullup on the $\overline{IRQ}$ pin. Your application must pull the $\overline{IRQ}$ pin to V_{DD} level to prevent interrupts.

In emulation:

The $\overline{IRQ}$ pin is pulled up on the module. Be aware that an application without the $\overline{IRQ}$ pin pulled high will emulate correctly but will fail in the application because of a floating IRQ line. The $\overline{IRQ}$ pin pulled high on the module causes these results.

Configuring for C4A/C8A/C12A

If the resident MCU on the M68EM05C9A is an MC68HC705C9A, you can reprogram the internal Mask Option register of the MC68HC705C9A MCU to behave more like an MC68HC05C12A. The MC68HC05C12A is similar to the MC68HC(7)05C4A and MC68HC05C8A

NOTE: *This procedure must be carried out after every RESET and so may not be suitable for all environments.*

Follow this procedure to reconfigure the MC68HC705C9A as an MC68HC705C12A.

- Write $80 into address $001C.
- Write a value into address $FFF1 as required. This register has three relevant bits:

C12COPE — C12A COP Enable (Bit 3)

This read-only bit enables the COP function when in C12A mode. If configured in C9A mode, this bit has no effect and will be forced to zero regardless of the programmed state.

1 = When in C12A mode, this enables the C12ACOP watchdog timer.
0 = When in C12A mode, this disables the C12ACOP watchdog timer.

C12IRQ — C12A Interrupt Request (Bit 1)

This read/write bit selects between an edge-triggered only or edge- and level-triggered external interrupt pin. If configured in C9A mode, this bit has no effect and will be forced to zero regardless of the programmed state.

1 = Edge and level interrupt option selected
0 = Edge-only interrupt option selected

CXA — C12A/C9A Mode Select (Bit 0)

This read/write bit selects between C12A configuration and C9A configuration.

1 = C12A configuration
0 = C9A configuration

So bit 0 must be configured to 1 to enable the C4A/C8A/C12A features. With this bit set, configure the IRQ and COP options as required.

MC68HC(7)05C9A Emulation

The MC68HC(7)05C9A MCU is emulated on the M68EM05C9A emulation module. The resident MCU (socket U9) can be either a ROM device, a MC68HC05C9A, or an EPROM device, a MC68HC705C9A. Because emulation flexibility is optimum when using the EPROM device, the M68EM05C9A is shipped with an MC68HC705C9A as the resident MCU.

The following paragraphs detail known differences between the performance of an MC68HC(7)05C9A MCU running in single-chip mode versus the way certain features will perform during emulation mode.

Mask Option Registers

The MC68HC705C9A has two mask options registers. The first at address $3FF0 controls the bits of Port B that are part of the keyboard interrupt. Writing to this register will cause a warning to be displayed on the debugger and will have no effect on the operation of Port B. This register is implemented in hardware on the M68EM05C9A. See **Port B Keyboard Interrupt Mask option, switch array S2** on page 25 for more details.

The second mask option register is at address $3FF1. This controls various system features inclusing the ability to emulate an MC68HC05C12A. You can write to this register in emulation mode by writing $80 into address $001C. All of the bits in the register are now programmable by simply writing to them and will behave as described in the Data Book.

Computer Operating Properly (Watchdog)

You can enable to COP by following the procedure in the MCU specification. The emulator will service this watchdog as long as it is configured in C9A mode and in the monitor mode. While running your code the emulator will no longer service the watchdog.

If you change the COP mode on the MC68HC705C9A device to C12A mode then you must load the personality file for the C12A. See **Table 3** for details.

MC68HC(7)05C4A Emulation

The MC68HC(7)05C4A MCU is emulated on the M68EM05C9A emulation module. The resident MCU (socket U9) can be either a ROM device, a MC68HC05C4A, an EPROM device, a MC68HC705C4A, or the default device, a MC68HC705C9A.

You can emulate most features of the MC68HC(7)05C4A with the MC68HC705C9A. The following paragraphs detail known differences between the performance of an MC68HC(7)05C4A MCU running in single-chip mode versus the way certain features will perform during emulation mode.

SPI Emulation

The installed MC68HC705C9A MCU has a more complex SPI system than the MC68HC(7)05C4A. To use the SPI system you must first initialise the Data Direction Register for Port D on the MC68HC705C9A so that bits 2 to 5 of DDRD are configured as required.

Set the DDRD at address $0007 as follows:

DDRD2

DDR for bit 2 and MISO
1 = output, when SPI in SLAVE mode
0 = input, when SPI in MASTER mode

DDRD3

DDR for bit 3 and MOSI
1 = output, when SPI in MASTER mode
0 = input, when SPI in SLAVE mode

DDRD4

DDR for bit 4 and SCK
1 = output, when SPI in MASTER mode
0 = input, when SPI in SLAVE mode

DDRD5

DDR for bit 5 and SS
1 = output, no SPI requirement

0 = input, SPI has possible use in SLAVE mode

NOTE: *If the MC68HC705C9A device is configured as an MC68HC705C12A device as in* ***Configuring for C4A/C8A/C12A*** *the DDR registers do not need to be configured for correct SPI operation.*

OPTION Register

The MC68HC705C9 has an OPTION register at address $3FDF. This register can enable extra RAM and ROM in memory that are present on the C4A. This OPTION register also includes a bit which determines IRQ sensitivity; either edge only or level and edge. This bit (1) may be used to emulate the IRQ mask option on the C4A.

COP Watchdog

The watchdog feature on the MC68HC705C9A is different from that on the C4A. If you require to use the watchdog then either replace the resident MCU with an MC68HC705C4A or reconfigure the resident MCU by refering to **Configuring for C4A/C8A/C12A**.

MC68HC05C8A Emulation

The MC68HC05C8A MCU is emulated on the M68EM05C9A emulation module. The resident MCU (socket U9) can be either a ROM device, a MC68HC05C8A, or the default device, a MC68HC705C9A.

You can emulate most features of the MC68HC05C8A with the MC68HC705C9A. The following paragraphs detail known differences between the performance of an MC68HC05C8A MCU running in single-chip mode versus the way certain features will perform during emulation mode.

SPI Emulation

The installed MC68HC705C9A MCU has a more complex SPI system than the MC68HC05C8A. To use the SPI system you must first initialise the Data Direction Register for Port D on the MC68HC705C9A so that bits 2 to 5 of DDRD are configured as required.

Set the DDRD at address $0007 as follows:

DDRD2

DDR for bit 2 and MISO
1 = output, when SPI in SLAVE mode
0 = input, when SPI in MASTER mode

DDRD3

DDR for bit 3 and MOSI
1 = output, when SPI in MASTER mode
0 = input, when SPI in SLAVE mode

DDRD4

DDR for bit 4 and SCK
1 = output, when SPI in MASTER mode
0 = input, when SPI in SLAVE mode

DDRD5

DDR for bit 5 and SS
1 = output, no SPI requirement
0 = input, SPI has possible use in SLAVE mode

NOTE: *If the MC68HC705C9A device is configured as an MC68HC705C12A device as in* ***Configuring for C4A/C8A/C12A*** *the DDR registers do not need to be configured for correct SPI operation.*

OPTION Register

The MC68HC705C9 has an OPTION register at address $3FDF. This register can enable extra RAM and ROM in memory that are present on the C8A. This OPTION register also includes a bit which determines IRQ sensitivity; either edge only or level and edge. This bit (1) may be used to emulate the IRQ mask option on the C8A.

COP Watchdog

The watchdog feature on the MC68HC705C9A is different from that on the C8A. If you require to use the watchdog then either replace the resident MCU with an MC68HC05C8A or reconfigure the resident MCU by refering to **Configuring for C4A/C8A/C12A**.

MC68HC705C8A Emulation

The MC68HC705C8A MCU is emulated on the M68EM05C9A emulation module. The resident MCU (socket U9) can be either an EPROM device, a MC68HC705C8A, or the default device, a MC68HC705C9A.

You can emulate most features of the MC68HC705C8A with the MC68HC705C9A. The following paragraphs detail known differences between the performance of an MC68HC05C8A MCU running in single-chip mode versus the way certain features will perform during emulation mode.

SPI Emulation

The installed MC68HC705C9A MCU has a more complex SPI system than the MC68HC705C8A. To use the SPI system you must first initialise the Data Direction Register for Port D on the MC68HC705C9A so that bits 2 to 5 of DDRD are configured as required.

Set the DDRD at address $0007 as follows:

DDRD2

DDR for bit 2 and MISO
1 = output, when SPI in SLAVE mode
0 = input, when SPI in MASTER mode

DDRD3

DDR for bit 3 and MOSI
1 = output, when SPI in MASTER mode
0 = input, when SPI in SLAVE mode

DDRD4

DDR for bit 4 and SCK
1 = output, when SPI in MASTER mode
0 = input, when SPI in SLAVE mode

DDRD5

DDR for bit 5 and SS
1 = output, no SPI requirement

0 = input, SPI has possible use in SLAVE mode

NOTE: *If the MC68HC705C9A device is configured as an MC68HC705C12A device as in* ***Configuring for C4A/C8A/C12A*** *the DDR registers do not need to be configured for correct SPI operation.*

OPTION Register

To emulate the exact OPTION register RAM/ROM behaviour of an MC68HC705C8, use a MC68HC705C8A substitute for the resident MCU. By restricting the use of the RAM/ROM available to that provided on the MC68HC705C8A the MC68HC705C9 can be used as the resident MCU. When using the MC68HC05C9 to emulate the MC68HC705C8 writes to the OPTION register should be made to address $3FDF rather than $1FDF.

COP Watchdog

The watchdog feature on the MC68HC705C9A is different from that on the C8A. If you require to use the watchdog then either replace the resident MCU with an MC68HC705C8A or reconfigure the resident MCU by refering to **Configuring for C4A/C8A/C12A**.

MC68HC05C12A Emulation

The MC68HC05C12A MCU is emulated on the M68EM05C9A emulation module. The resident MCU (socket U9) can be either a ROM device, a MC68HC05C12A, or the default device, a MC68HC705C9A.

You can emulate most features of the MC68HC05C12A with the MC68HC705C9A. The following paragraphs detail known differences between the performance of an MC68HC05C12A MCU running in single-chip mode versus the MC68HC705C9A in emulation mode.

SPI Emulation

The installed MC68HC705C9A MCU has a more complex SPI system than the MC68HC05C12A. To use the SPI system you must first initialise the Data Direction Register for Port D on the MC68HC705C9A so that bits 2 to 5 of DDRD are configured as required.

Set the DDRD at address $0007 as follows:

DDRD2

DDR for bit 2 and MISO
1 = output, when SPI in SLAVE mode
0 = input, when SPI in MASTER mode

DDRD3

DDR for bit 3 and MOSI
1 = output, when SPI in MASTER mode
0 = input, when SPI in SLAVE mode

DDRD4

DDR for bit 4 and SCK
1 = output, when SPI in MASTER mode
0 = input, when SPI in SLAVE mode

DDRD5

DDR for bit 5 and SS
1 = output, no SPI requirement
0 = input, SPI has possible use in SLAVE mode

NOTE: *If the MC68HC705C9A device is configured as an MC68HC705C12A device as in* ***Configuring for C4A/C8A/C12A*** *the DDR registers do not need to be configured for correct SPI operation.*

OPTION Register

The MC68HC705C9 has an OPTION register at address $3FDF. This register can enable extra RAM and ROM in memory that are present on the C8A. This OPTION register also includes a bit which determines IRQ sensitivity; either edge only or level and edge. This bit (1) may be used to emulate the IRQ mask option on the C8A.

COP Watchdog

The watchdog feature on the MC68HC705C9A is different from that on the C12A. If you require to use the watchdog then either replace the resident MCU with an MC68HC05C12A or reconfigure the resident MCU by refering to **Configuring for C4A/C8A/C12A**.

Schematics

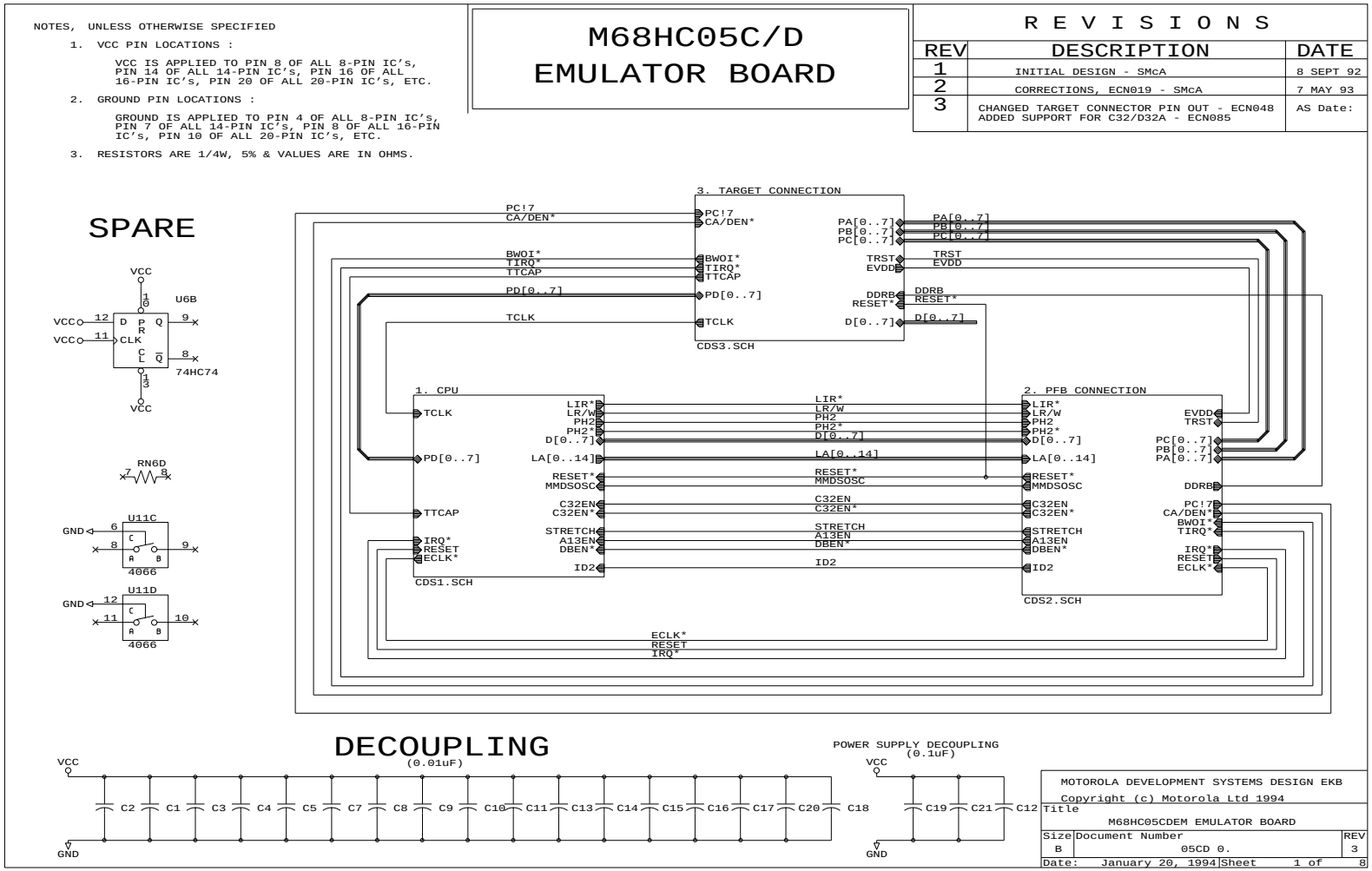
Contents

M68EM05C9A Schematics

Refer to the following pages for the eight sheets of schematics for the M68EM05C9A emulation module.

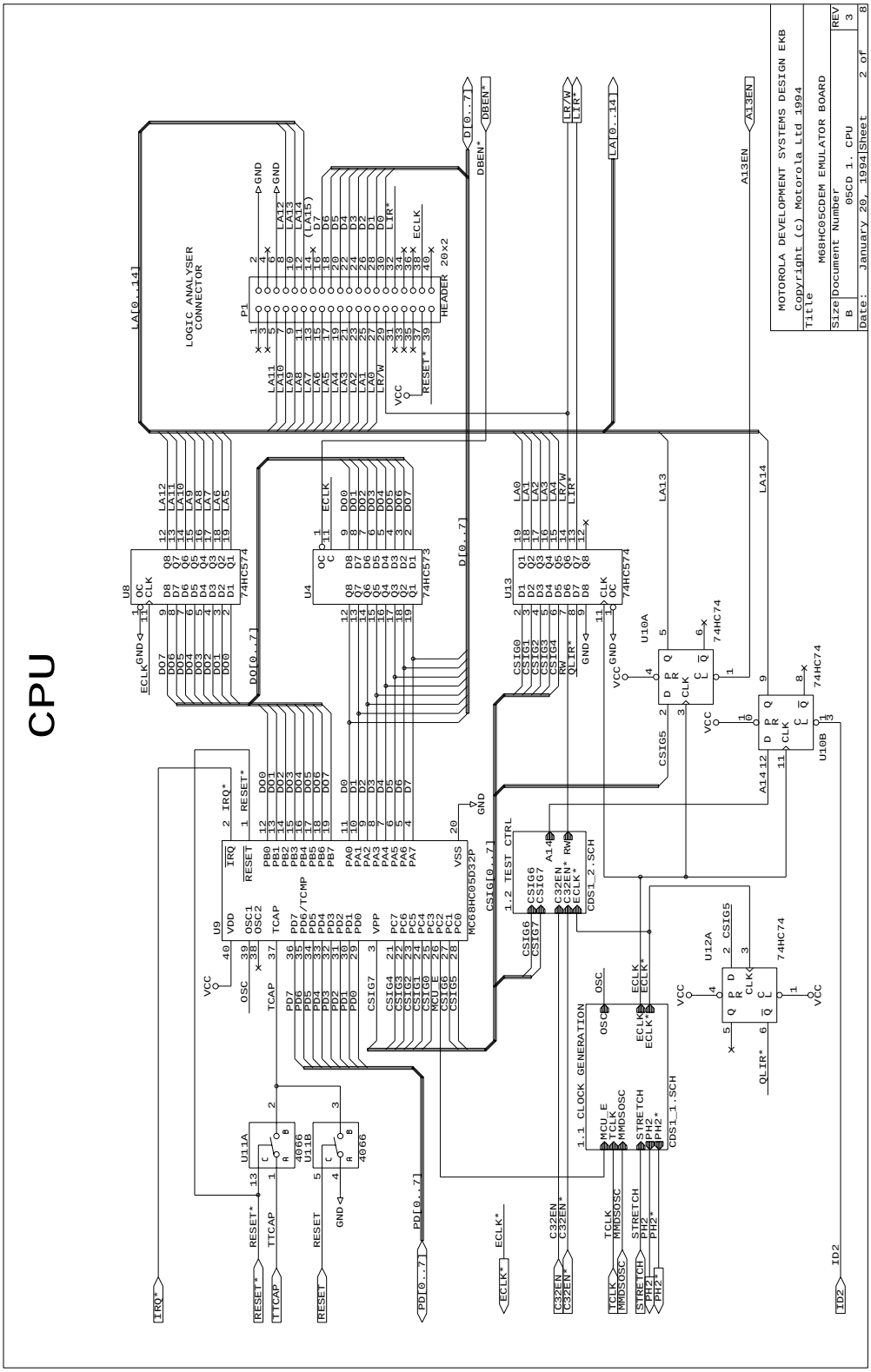
M68EM05C9A Schematics

M68EM05C9A Schematics (Sheet 1 of 8)



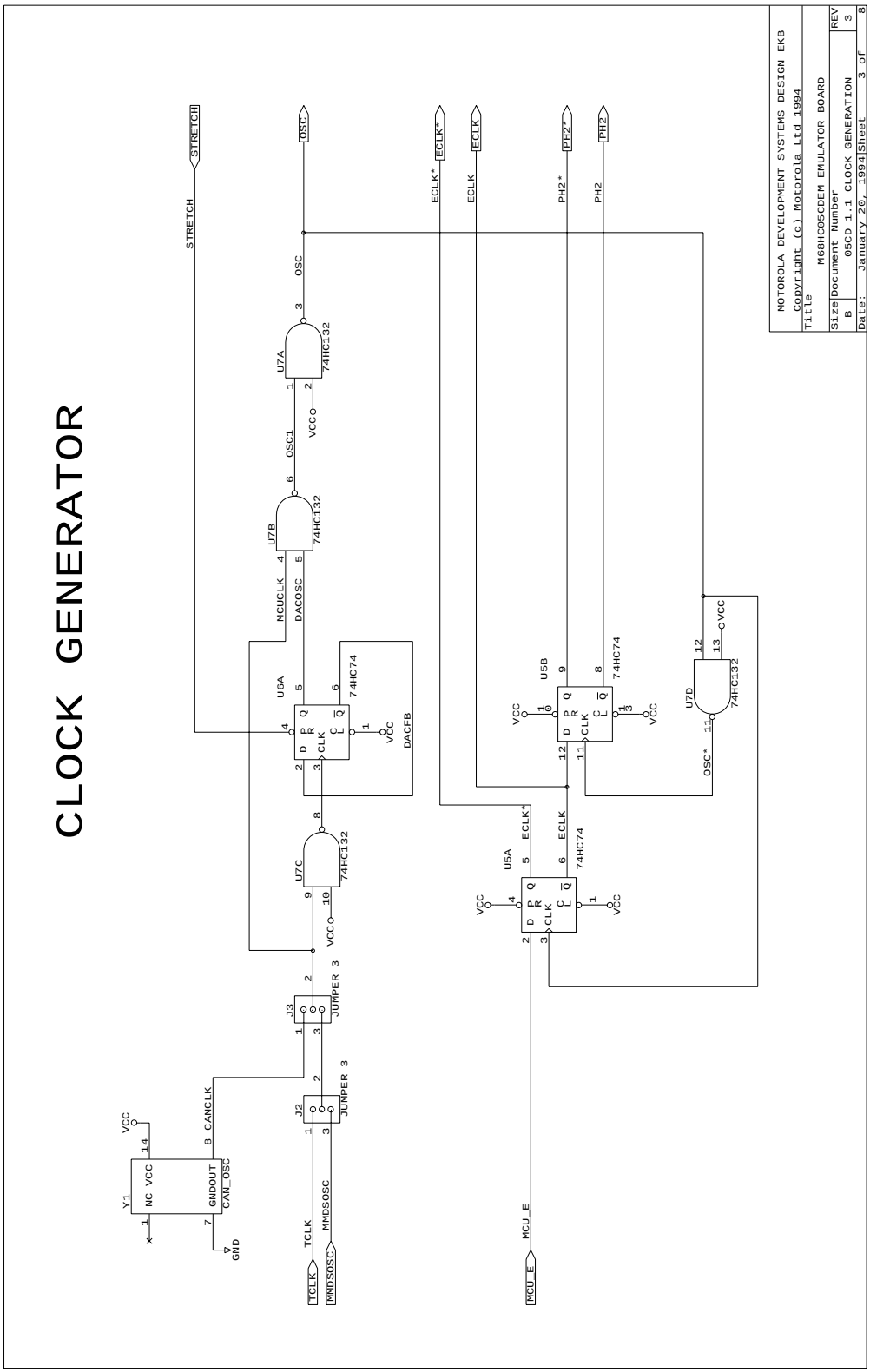
M68EM05C9A Schematics

M68EM05C9A Schematics (Sheet 2 of 8)



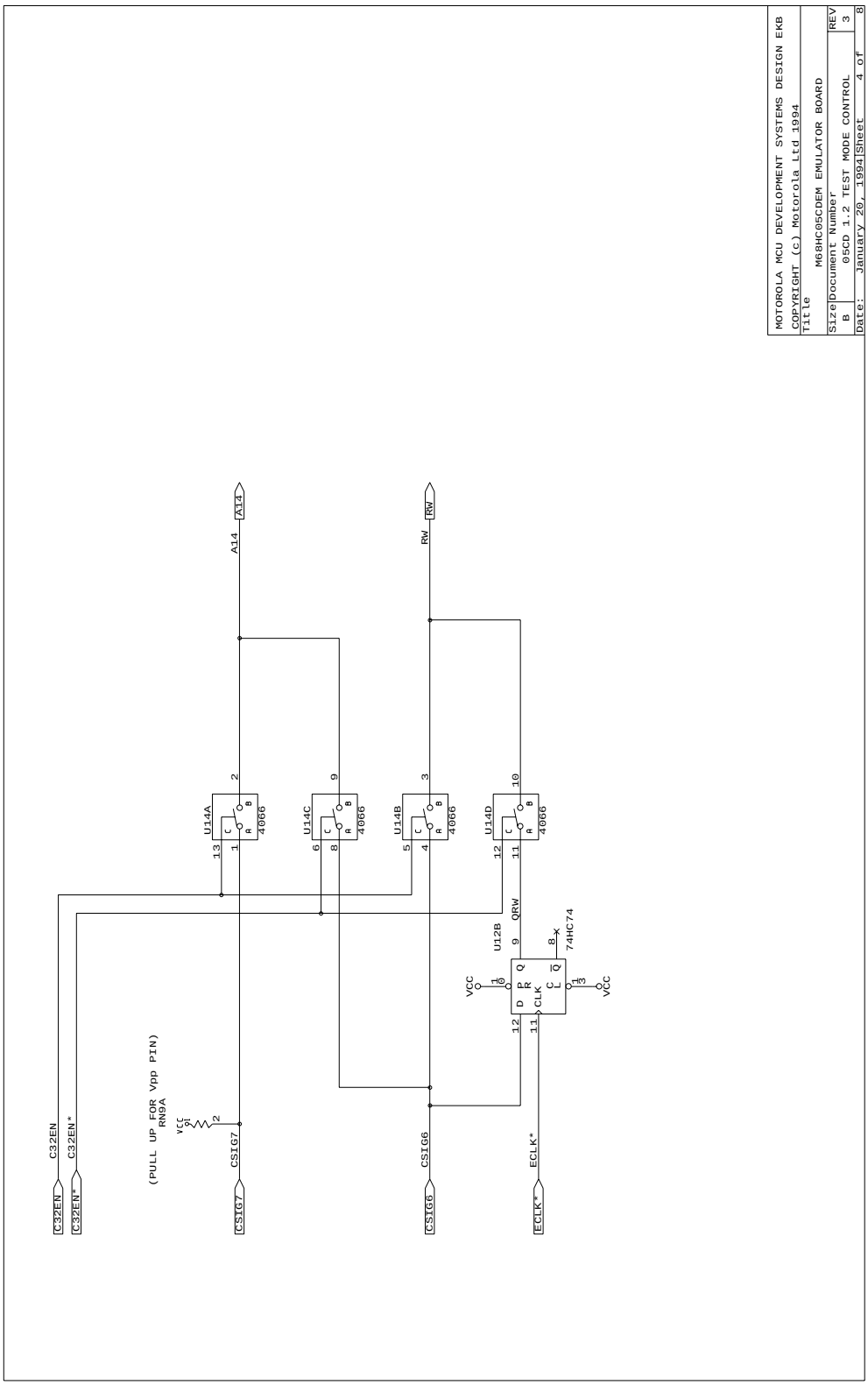
M68EM05C9A Schematics

M68EM05C9A Schematics (Sheet 3 of 8))



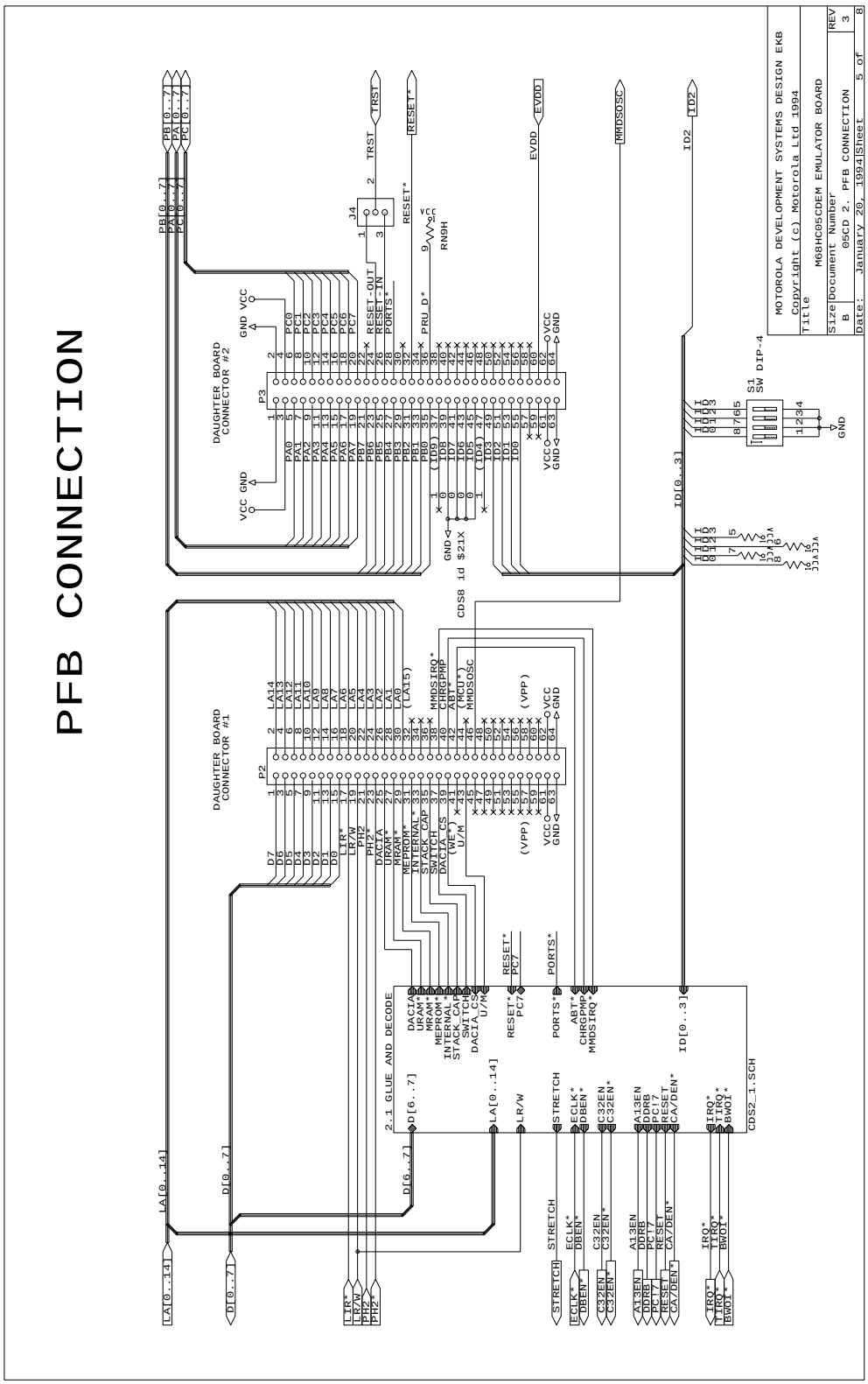
M68EM05C9A Schematics

M68EM05C9A Schematics (Sheet 4 of 8)



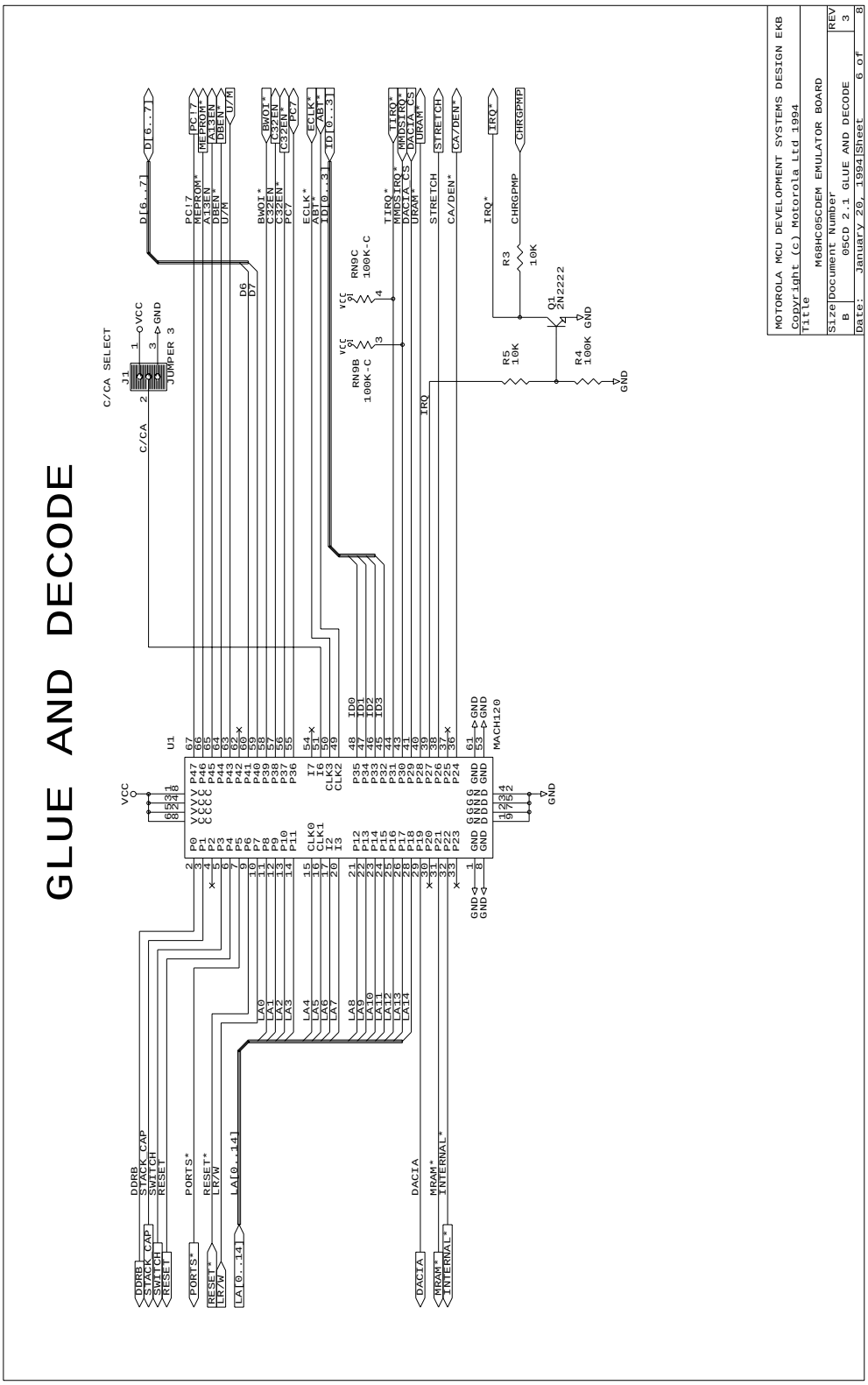
M68EM05C9A Schematics

M68EM05C9A Schematics (Sheet 5 of 8)



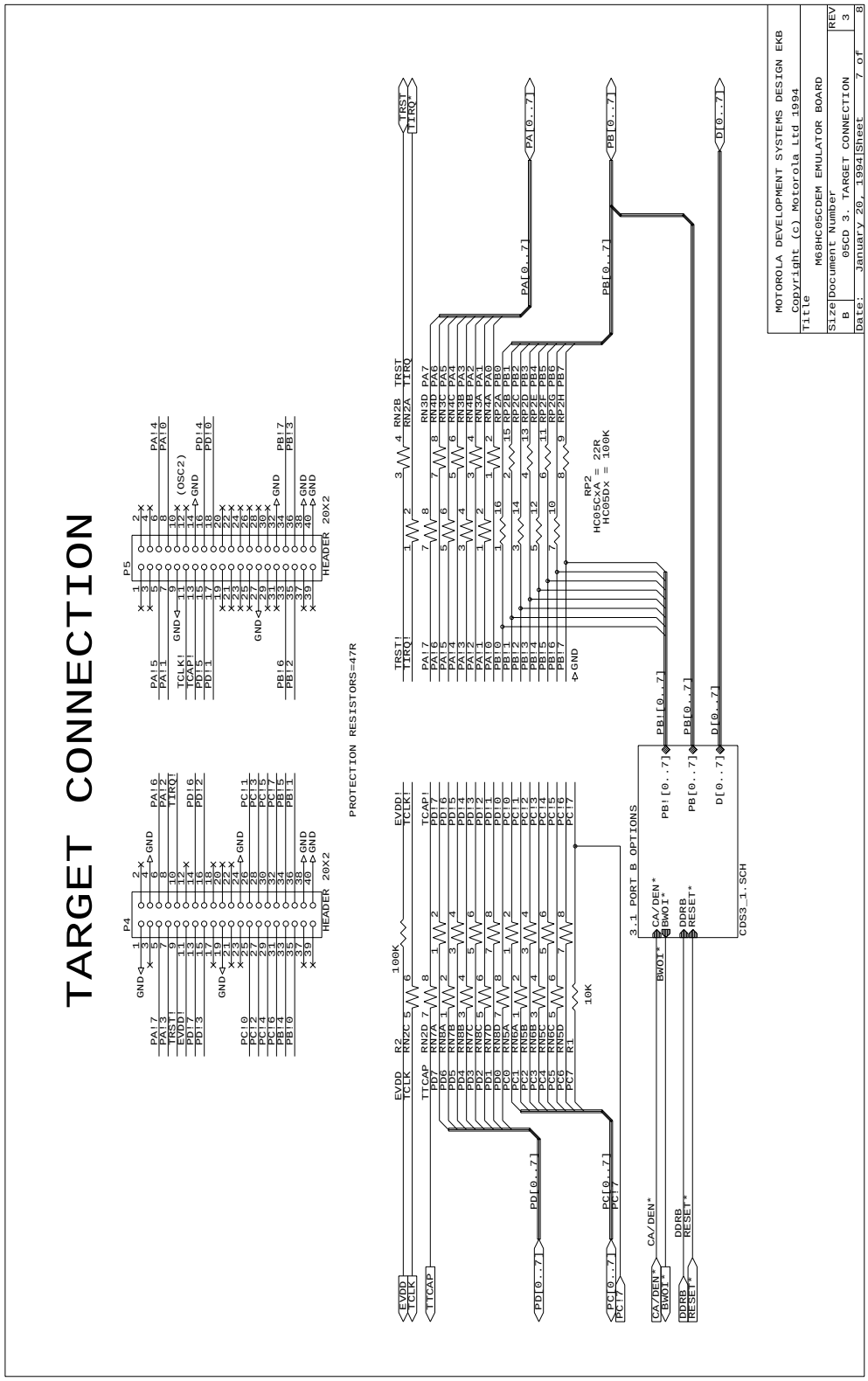
M68EM05C9A Schematics

M68EM05C9A Schematics (Sheet 6 of 8)



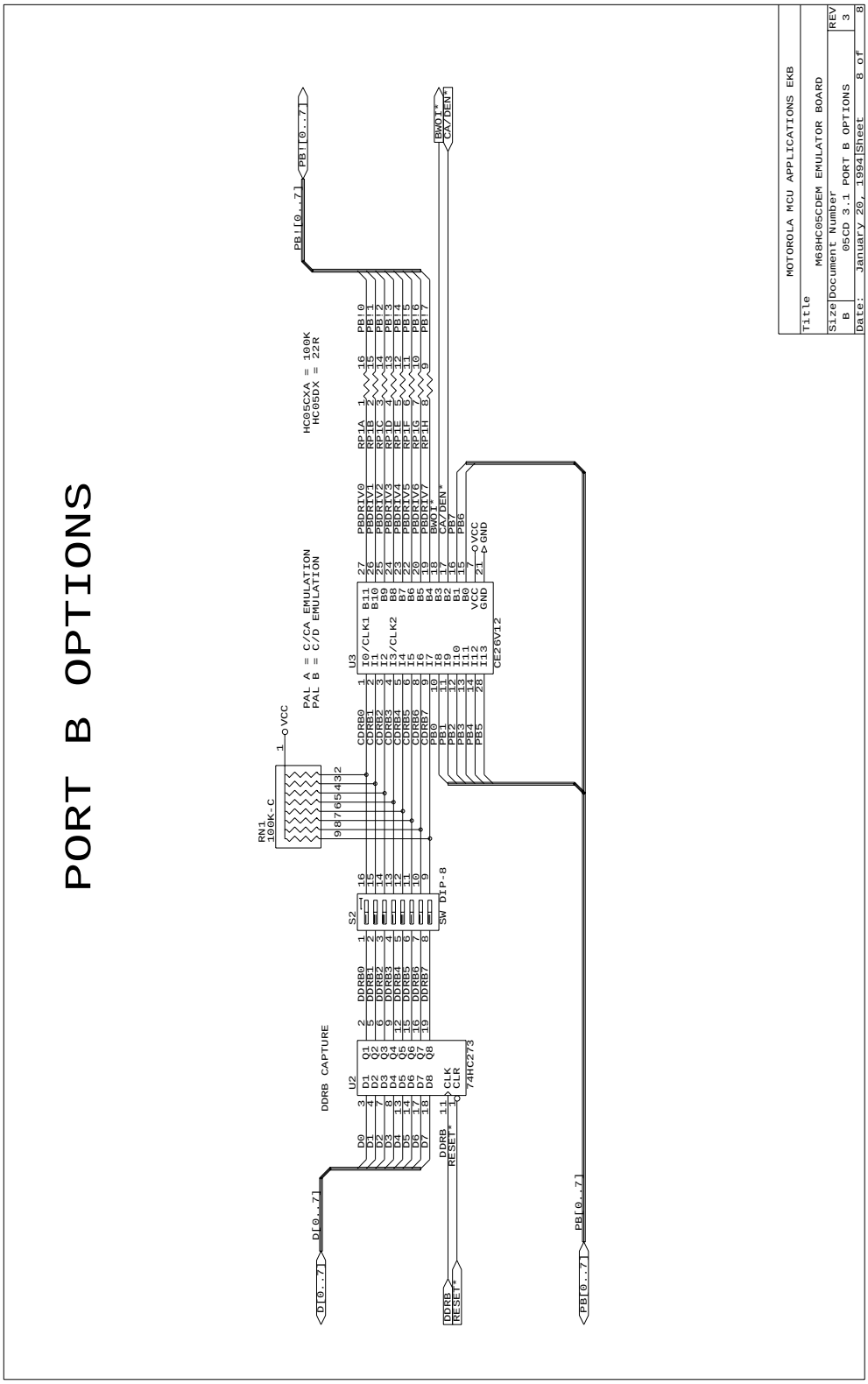
M68EM05C9A Schematics

M68EM05C9A Schematics (Sheet 7of 8)



M68EM05C9A Schematics

M68EM05C9A Schematics (Sheet 8 of 8)



M68EM05C9A Schematics

How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.1-800-441-2447 or 602-303-5454

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE 602-244-6609

INTERNET: http://Design-NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-81-3521-8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298