# M68EM05JB2

## Emulation Module
## User's Manual

January 27, 1997

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# Revision History

The following table summarizes differences between this revision and the previous revision of this emulation module user's manual.

| | |
|---|---|
| **Previous Revision** | NONE |
| **Current Revision** | 0.0 |
| **Date** | 01/97 |
| **Changes** | N/A |
| **Location** | N/A |

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# General Description

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## Introduction

The M68EM05JB2 Emulation Module (EM) enables the Motorola development tool to emulate target systems based on the MC68HC705JB2 Microcontroller Unit (MCU). The Motorola development tool can emulate other MCUs when you use an emulation module other than the M68EM05JB2. This manual provides connection, configuration, and operation information specific to the M68EM05JB2 Emulation Module. Refer to the *Motorola Development Tool Selector Guide* (order number SG173/D) for a complete list of available emulation modules.

The EM can be installed in either of two Motorola development systems: the MMDS05 or the MMEVS05/MMEVS08. Follow the procedures described in **MMDS/MMEVS Configuration and Operation** on page 17 to configure the M68EM05JB2 for either an MMDS05 or MMEVS05/MMEVS08 development system.

## Emulation Components

The M68EM05JB2 Emulation Module consists of the following items:

- **M68EM05JB2 Emulation Module** — Enables system functionality for the MC68HC705JB2 MCU. The female connectors, on the bottom of the module, mate with male connectors on a development system platform board. The EM also provides an integrated connector for the target cable assembly.
- **Configuration software** — A 3 1/2-inch diskette provides personality files for this module.

Separately–purchased Motorola modular development tool options include those listed below:

- **MMEVS (M68MMPFB0508) Platform Board** — Provides real-time in-circuit emulation. The MMEVS design environment consists of an editor, an assembler, a user interface, and a source-level debugging program.
- **MMDS05 Modular Development System (MMDS)** — Provides all the capabilities of the MMEVS including a bus state analyzer and real-time memory windowing functionality.
- **Flex Cable Target Assembly** — Connects the M68EM05JB2 to a target development system. Refer to **Target Cable Assemblies** on page 10 for detailed information.

User supplied components include:

- **Host computer** — Refer to the appropriate development tool user's manual for system requirements.
- **Power supply** — +5 Vdc required for the MMEVS.

## Emulation Module Layout

Jumper header W1 enables you to select an externally–sourced clock signal. Connector J2 connects to a target system. This connector requires the use of a separately–purchased target cable assembly. When you install the M68EM05JB2 on the MMDS05, the target cable passes through the slit in the station module enclosure. Connector J1 connects to a logic analyzer. DIN connectors P1 and P2 connect the EM and a development system platform board.

Pin assignments and signal descriptions for connector J2 can be found in **Target Cable Connector Pin Assignments** on page 12. Pin assignments and signal descriptions for connector J1 can be found in **Logic Analyzer Connector J1 Pin Assignments** on page 14.

**Figure 1** shows the connector layout of the M68EM05JB2 Emulation Module.

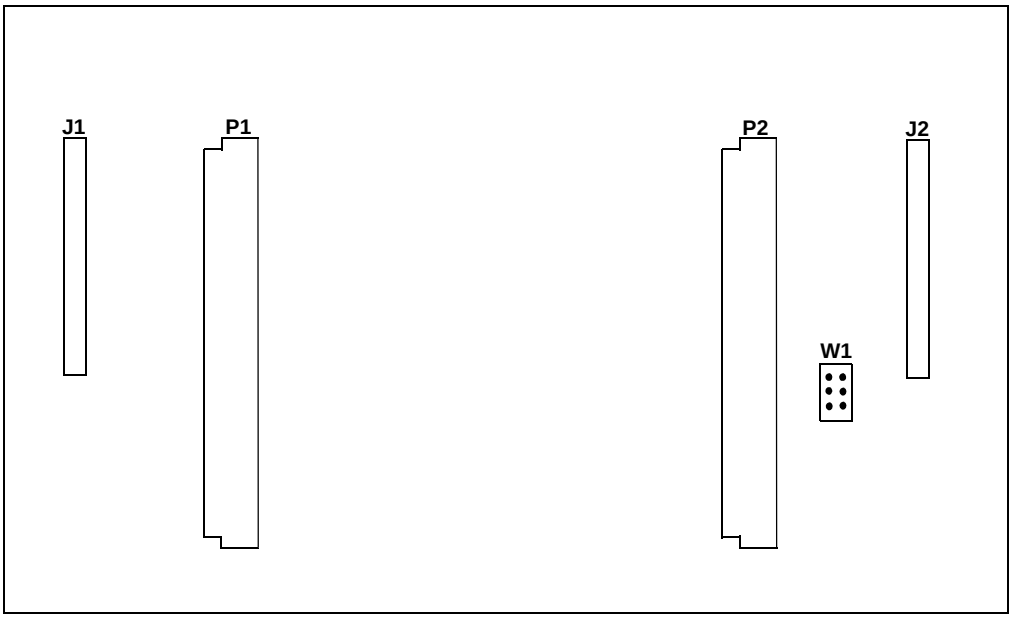


**Figure 1. M68EM05JB2 Emulation Module**

## Target Cable Assemblies

The M68EM05JB2 requires a separately–purchased target cable assembly to connect to a target system. Cable assemblies are available for two MCU packages: a 20–pin DIP package and a 20–pin SOIC package.

**Figure 2**, on the following page, shows a target cable assembly. The target cable assembly for a 20–pin DIP package consists of a flex cable and a target head adapter. The assembly connects to the EM via connector J2.

The target cable assembly for a 20–pin SOIC package consists of a flex cable, a target head adapter, and an additional SOIC adapter. One end of the flex cable plugs onto connector J2, as shown in **Figure 2**. The other end of the flex cable plugs onto the target head adapter. The target head adapter connects onto a DIP connector located in the target system, or onto the SOIC adapter.

The target system MCU package determines which target cable assembly components are required, as shown below:

- For a 20–pin DIP package, use flex cable M68CBL05A and target head adapter M68TA05JB2P20.
- For a 20–pin SOIC package, use the flex cable assembly for the 20–pin DIP in conjunction with SOIC adapter M68DIP20SOIC.

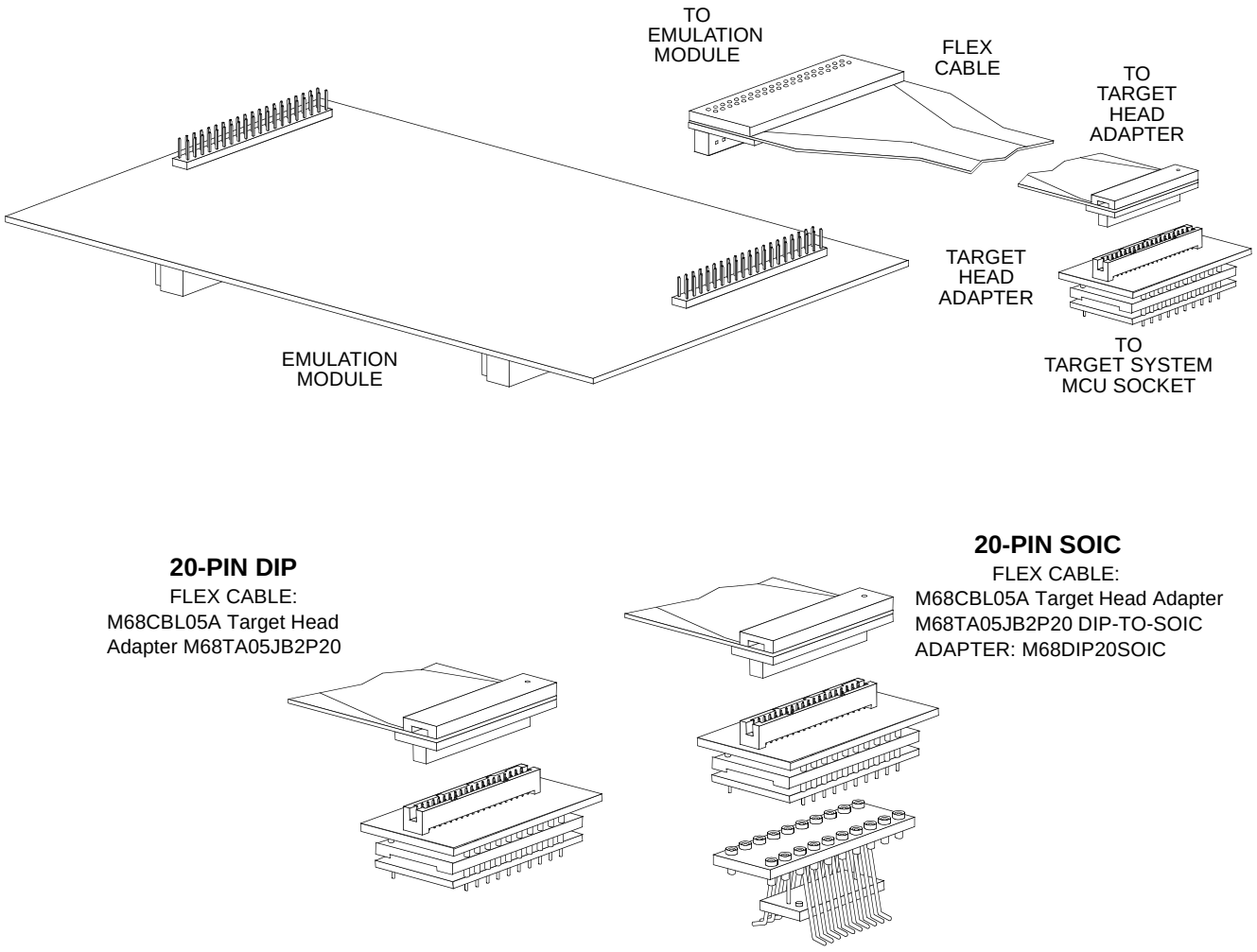


**Figure 2. Target Cable Assembly**

## Connector Information

The connectors on the M68EM05JB2 provide access to user–mode emulation signals on connector J2 as well as select internal signals on connector J1. Connector J2 interfaces the EM to a target system. Connector J1 connects the EM to a logic analyzer.

### Target Cable Connector Pin Assignments

**Figure 3** shows the pin assignments for connector J2. **Table 1**, shown on the following page, lists all signal descriptions.

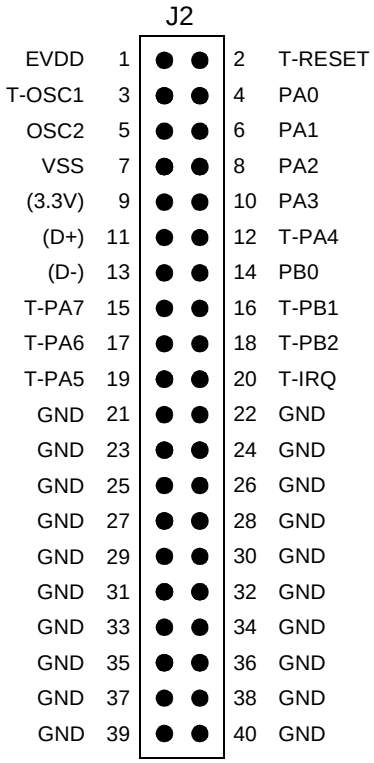


**Figure 3. Target Connector Pin Assignments**

## Table 1. Connector J2 Signal Descriptions

| Pin | Mnemonic | Signal |
|---|---|---|
| 14 | PB0 | PORT B (bit 0) — General–purpose I/O lines controlled by software using data direction and data registers. Pin 14 also functions as a TCAP pin for the TIMER 1 module. This pin implements an input pull–down capability (controlled by software) using the PDURB pull–down register and the PULLREN bit of the MOR register. |
| 16 | T-PB1 | PORT B (bit 1) — General–purpose I/O lines controlled by software using data direction and data registers. Pin 16 implements a pull–up capability (controlled by software) using the PDURB pull–up register and the PULLREN bit of the MOR register. This pin incorporates a slow output falling transition time of 170ns at a 3 MHz bus rate, controlled by software, using the SLOWE bit of the data register.<br><br>Output high current sink = 25mA at $V_{ol}$ ($0.5V_{max}$). |
| 18 | T-PB2 | PORT B (bit 2) — General–purpose I/O lines controlled by software using data direction and data registers. Pin 18 implements a pull–up capability (controlled by software) using the PDURB pull–up register and the PULLREN bit of the MOR register. This pin incorporates a sharp falling output delayed by 170ns at 3 MHz (controlled by software) using the SLOWE bit of the data register.<br><br>Output high current sink = 25mA at $V_{ol}$=$0.5V_{max}$ |
| 3 | $EV_{DD}$ | EXTERNAL VOLTAGE DETECT — Connected to target $V_{CC}$ to sense target system power that is displayed in the MMDS05 target system status window. |
| 7, 21-40 | GND, VSS | GROUND |
| 3 | T-OSC1 | TARGET OSCILLATOR 1 — External clock source input for the M68EM05JB2 Emulation Module. The system bus frequency is T-OSC1÷ 2 and is controlled by jumper header W1. |
| 5 | OSC2 | OSCILLATOR 2 — Output clock signal. Inversion of the OSC1 clock. |
| 11, 13 | (D+), (D-) | Differential data lines for the low-speed USB. |
| 9 | (3.3V) | Provides a 3.3V +/-10% DC voltage for USB pull–up resister |
| 20 | T-IRQ | TARGET INTERRUPT REQUEST — Active–low input signal from the target system that applies an asynchronous MCU interrupt. |
| 2 | T-RESET | Active–low bidirectional signal to/from the target system and driven low to place the MCU into a reset mode. |
| 4, 6, 8, 10, 12, 19, 17, 15 | PA0, PA1, PA2, PA3, T-PA4, T-PA5, T-PA6, T-PA7 | PORT A (bits 0, 1, 2, 3, 4, 5, 6, 7) — General–purpose I/O lines controlled by software using data direction and data registers. Port A incorporates an input pull–down capability on all pins. This is controlled by software using the PDURA pull–down register and the PULLREN bit of the MOR register. Port A implements an external interrupt capability on bits 0–3 (controlled by software) using the PAINTEN bit of the MOR register. |

## Logic Analyzer Connector J1 Pin Assignments

**Figure 4** shows the pin assignments for connector J1. **Table 2** lists all signal descriptions.

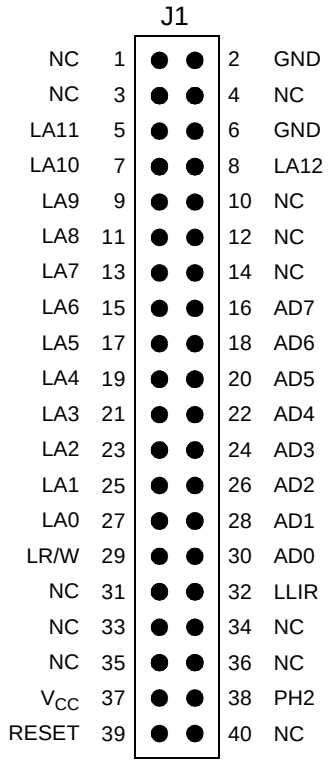


**Figure 4. Connector J1 Pin Assignments**

## Table 2. Logic Analyzer Connector J1 Signal Descriptions

| Pin | Mnemonic | Signal |
|---|---|---|
| 1, 3, 4, 10, 12, 14, 31, 33, 34, 35, 36, 40 | NC | No connection. |
| 2, 6 | GND | GROUND. |
| 8 | LA12 | LATCHED ADDRESS (bit 12) — MCU latched–output address bus. |
| 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27 | LA11–LA0 | LATCHED ADDRESSES (bits 11–0) — MCU latched output address bus. |
| 16, 18, 20, 22, 24, 26, 28, 30 | AD7–AD0 | DATA BUS (bits 7–0) — MCU multiplexed I/O bus. |
| 29 | LR/W | LATCHED READ/WRITE — The MCU's write signal is latched to and used on the emulation module to control emulation memory accesses. |
| 32 | LLIR | LOAD INSTRUCTION REGISTER — Active low signal indicating an opcode fetch cycle is in progress. |
| 37 | $V_{CC}$ | +5 Vdc POWER — Connection to the system voltage $V_{CC}$. |
| 38 | PH2 | ANALYZER CLOCK — The latched addresses are valid on the latched address bus at the falling edge of PH2. Data is valid on the AD BUS at PH2 rising edge. |
| 39 | RESET | RESET — Active–low signal that is asserted during an internally or externally caused reset. |

# MMDS/MMEVS Configuration and Operation

## Contents

## Introduction

This chapter explains how to configure and use the M68EM05JB2 with an MMDS or MMEVS development system. For other system installation and configuration information, refer to either the *MMDS05 Operations Manual* (MMDS05OM/D) or the *MMEVS05/MMEVS08 Operations Manual* (MMEVS0508OM/D).

The topics covered in this chapter are:

- **Setting M68EM05JB2 Jumper Headers** on page 19 describes how to set jumper headers.
- **Remaining System Installation** on page 21 describes the final steps to system installation.
- **Personality Files Usage** on page 22 describes how to use the personality file on the M68EM05JB2 Emulation Module.
- **MC68HC05JB2 Emulation** on page 23 explains special emulation considerations.

***NOTE:*** *To configure a pre–installed M68EM05JB2 Emulation Module, remove all system power and follow the procedures in this chapter.*

***CAUTION:*** *Be sure to switch off all power before you reconfigure a pre–installed EM. Reconfiguring jumper headers with the power on can damage emulation circuits.*

## Setting M68EM05JB2 Jumper Headers

The M68EM05JB2 has one jumper header — W1. The following describes how to configure jumper header W1.Refer to **Figure 5. Jumper Header W1**, for the following procedures.

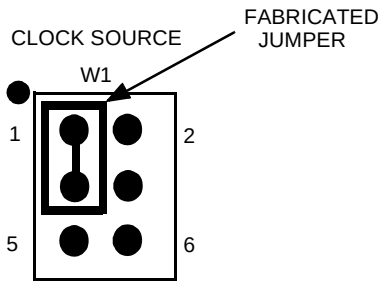


**Figure 5. Jumper Header W1**

### Clock Source Select Jumper Header W1

Jumper header W1 determines the source of the clock signal. **Figure 5** illustrates the jumper header where the unmarked pins (3 and 4) indicate common pins. The default configuration selects the 6 MHz canned oscillator clock source (at board location Y2).

There are three other possible clock sources.

*From the Platform Board:*

**1.** Reposition the W1 jumper between pins 2 and 4.

**2.** Use the system's OSC command to select a frequency.

*From a user–supplied source coming through the target cable connected to J2:*

**1.** Reposition the W1 jumper between pins 4 and 6.

***NOTE:*** *The user–supplied source must be a CMOS level square wave.*

*From a user–supplied crystal oscillator circuit:*

**1.** Reposition the W2 jumper between pins 3 and 5.

**2.** Supply the components for the Y1 crystal circuit.

The IC device at location U5 is a 74HCU04 inverter and provides signal inversion for a standard single–inverter oscillator circuit. You must supply the appropriate crystal, resistors, and capacitors for operating the clock at a user–specified frequency. See **M68EM05JB2 Schematics (Sheet 4 of 7)** on page 33 for engineering details.

***NOTE:*** *The 05JB2 MCU has a maximum source clock frequency specification of 6 MHz.*

## Remaining System Installation

You have completed configuring the M68EM05JB2 Emulation Module when jumper header W1 has been configured. Ensure that the following items are in place before completing your system installation:

**1.** Ensure the development tool power is shut down.

**2.** Remove the station module top panel if you are installing the EM in an MMDS05 station module.

**3.** Attach the P1 and P2 EM connectors (located on the bottom of the emulation module) to the platform board DIN connectors. Snap the corners of the EM onto the platform board plastic standoffs.

**4.** Connect the target cable assembly, if appropriate.

**5.** Replace the station module top panel if you are installing the EM in an MMDS05 station module.

You are now ready to connect the remaining cables and restore system power. For cable connection procedures, refer to either the *MMEVS05/MMEVS08 Operations Manual* (MMEVS0508OM/D) or *MMDS05 Operations Manual* (MMDS05OM/D).

## Personality Files Usage

The MMDS and MMEVS development systems use a specific personality file to emulate an MC68HC05JB2 MCU: the 0002DVxx.MEM file. This file is on an individual disk shipped with the M68EM05JB2. The file name format is **`00ZZZVxx.MEM`**: where **`ZZZ`** is the EM identifier or the MCU name, and **`xx`** is the personality file version.

System software loads a default personality file upon power–up. The 0002DVxx.MEM file is loaded as the default personality file when using the M68EM05JB2 on either the MMDS or MMEVS development systems.

The default personality file assigns the following address ranges to RAM and ROM:

- RAM: $80–$FF
- ROM: $1600–$1DFF

Writing to a location mapped as ROM generates a write–protect error halting user code execution. However, a writing to a location mapped as RAM does *not* halt user code execution.

Understanding how the MMDS/MMEVS development systems handle memory mapping enables you to customize the memory map according to your specific application needs.

***NOTE:*** *Use the SETMEM command to change memory settings.* Refer to the *MMDS05 Operations Manual* (MMDS05OM/D) for information on how to use the SETMEM command.

## MC68HC05JB2 Emulation

The following paragraphs describe the differences in the performance of an MC68HC05JB2 MCU run in single–chip mode versus emulation mode.

### Mask Option Register (MOR) Control

In single–chip mode operation:

The MCU mask options are determined by which options have been programmed in MOR location $1FF. This register must be programmed using a dedicated programming tool.

In emulation mode:

The mask option register must be programmed to the desired value, prior to inserting the MCU into the MC68HC705JB2 module, using a dedicated programming tool. The exceptions are the IRQTRIG, PULLREN and PAINTEN mask options described in **IRQTRIG Mask Option Bit**, **PULLREN Mask Option Bit** and **PAINTEN Mask Option Bit,** respectively.

### IRQTRIG Mask Option Bit

In single-chip mode operation:

The software–programmable high–level interrupt enable option for pins $\overline{\text{IRQ}}$, PB1, and PA0–PA7, is determined by what has been programmed in the MOR. The high–level interrupt is inhibited when this bit is set.

In emulation mode:

The mask option is controlled via software and allow–mask–option changes during a debug session. Option changes are performed by command entry (e.g., the MM command) or by executing user code (e.g., the STA instruction).

Mask options are set by writing the desired mask option register bit value to MOR location $1FF. If you use the Memory Modify (MM) command, a **'Write did not verify'** message may be displayed and should be ignored. The mask option bit returns to a default value of 1 when the MCU is reset.

**PULLREN Mask Option Bit**

In single-chip mode operation:

The software–programmable pullup/pulldown enable option for the Port A and Port B pins is determined by what has been programmed in the MOR. The pullup/pulldown option is enabled when this bit is set.

In emulation mode:

The mask option is controlled using software and allow–mask–option changes during a debug session. Option changes are performed by command entry (e.g., the MM command) or by user code execution (e.g., the STA instruction).

Mask options are set by writing the desired mask option register bit value to MOR location $1FF. If you use the Memory Modify (MM) command, a **'Write did not verify'** message may be displayed and should be ignored. The mask option bit returns to a default value of 1 when the MCU is reset.

**PAINTEN Mask Option Bit**

In single-chip mode operation:

The software programmable interrupt enable option for pins PA0 to PA3 is determined by what has been programmed in the MOR register. If this bit is set, interrupt enable option is inhibited.

In emulation:

The mask option is controlled by software and allow–mask–option changes during a debug session. Option changes are performed by command entry (e.g., the MM command) or by user code execution (e.g., the STA instruction).

Mask options are set by writing the desired mask option register bit value to MOR location $1FF. If you use the Memory Modify (MM) command, a **'Write did not verify'** message may be displayed and should be ignored. The mask option bit returns to a default value of 1 when the MCU is reset.

# Schematics

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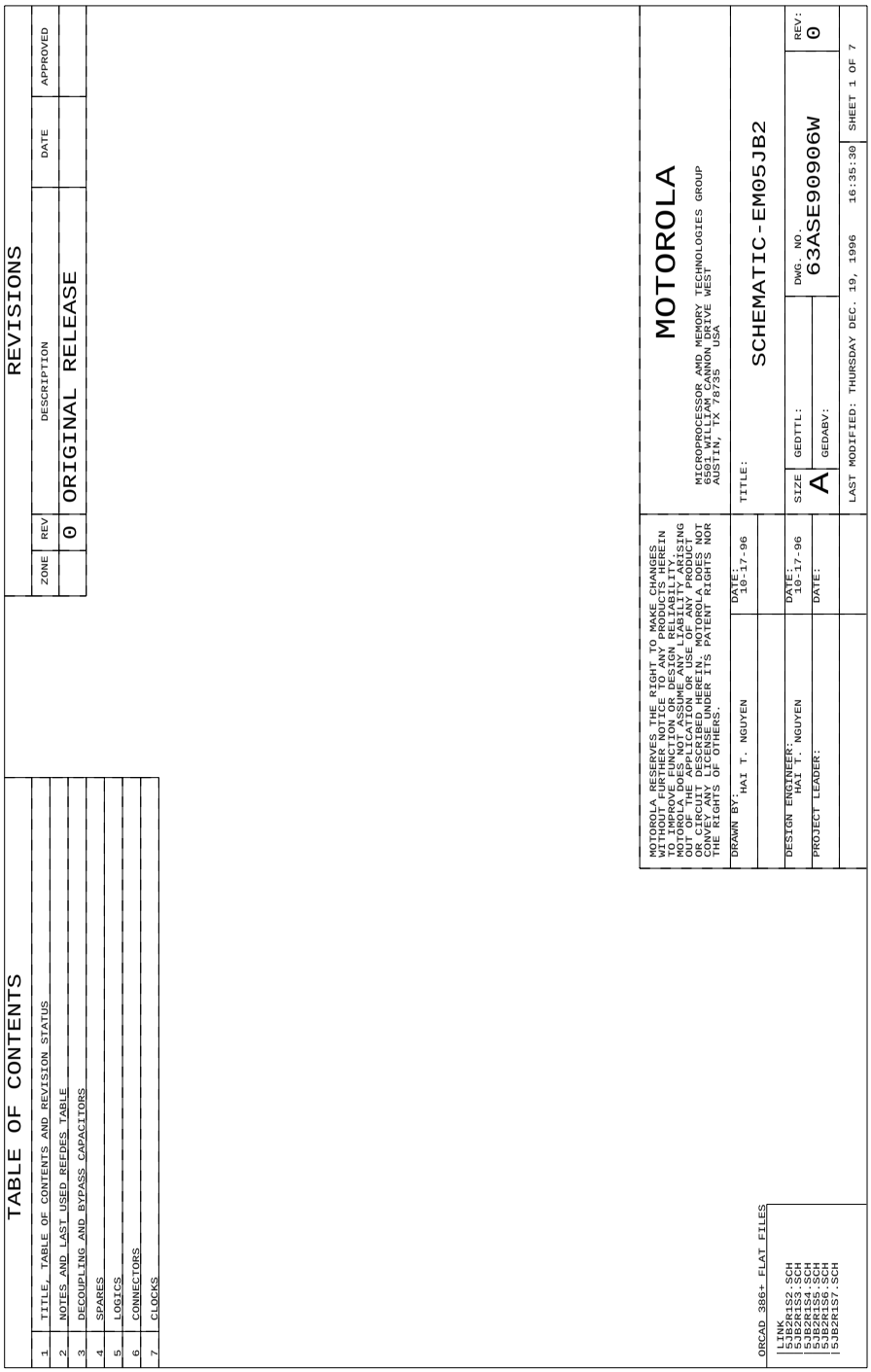
## M68EM05JB2 Schematics

This chapter provides schematics for the M68EM05JB2 Emulation Module.

## M68EM05JB2 Schematics (Sheet 1 of 7)



# M68EM05JB2 Schematics (Sheet 2 of 7)

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS, 5%, 1/4 WATT.
   ALL CAPACITORS ARE IN UF.
   ALL VOLTAGES ARE DC.

2. INTERRUPTED LINES CODED WITH THE SAME LETTER OR LETTER COMBINATIONS ARE ELECTRICALLY CONNECTED.

3. DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH THE MANUFACTURER.

4. SPECIAL SYMBOL USAGE:
   * DENOTES - ACTIVE LOW SIGNAL.
   [] DENOTES - VECTORED SIGNALS.

5. INTERPRET DIAGRAM IN ACCORDANCE WITH AMERICAN NATIONAL STANDARDS INSTITUTE SPECIFICATIONS, CURRENT REVISION, WITH THE EXCEPTION OF LOGIC BLOCK SYMBOLOGY.

6. CODE FOR SHEET TO SHEET REFERENCES IS AS FOLLOWS:
   SH # < OR > FOR INPUT OR OUTPUT

7. VCC LOCATIONS
   UNLESS OTHERWISE SPECIFIED, VCC IS APPLIED TO:
   PIN 8 OF ALL 8-PIN ICS
   PIN 14 OF ALL 14-PIN ICS
   PIN 16 OF ALL 16-PIN ICS
   PIN 20 OF ALL 20-PIN ICS
   PIN 24 OF ALL 24-PIN ICS, ETC.

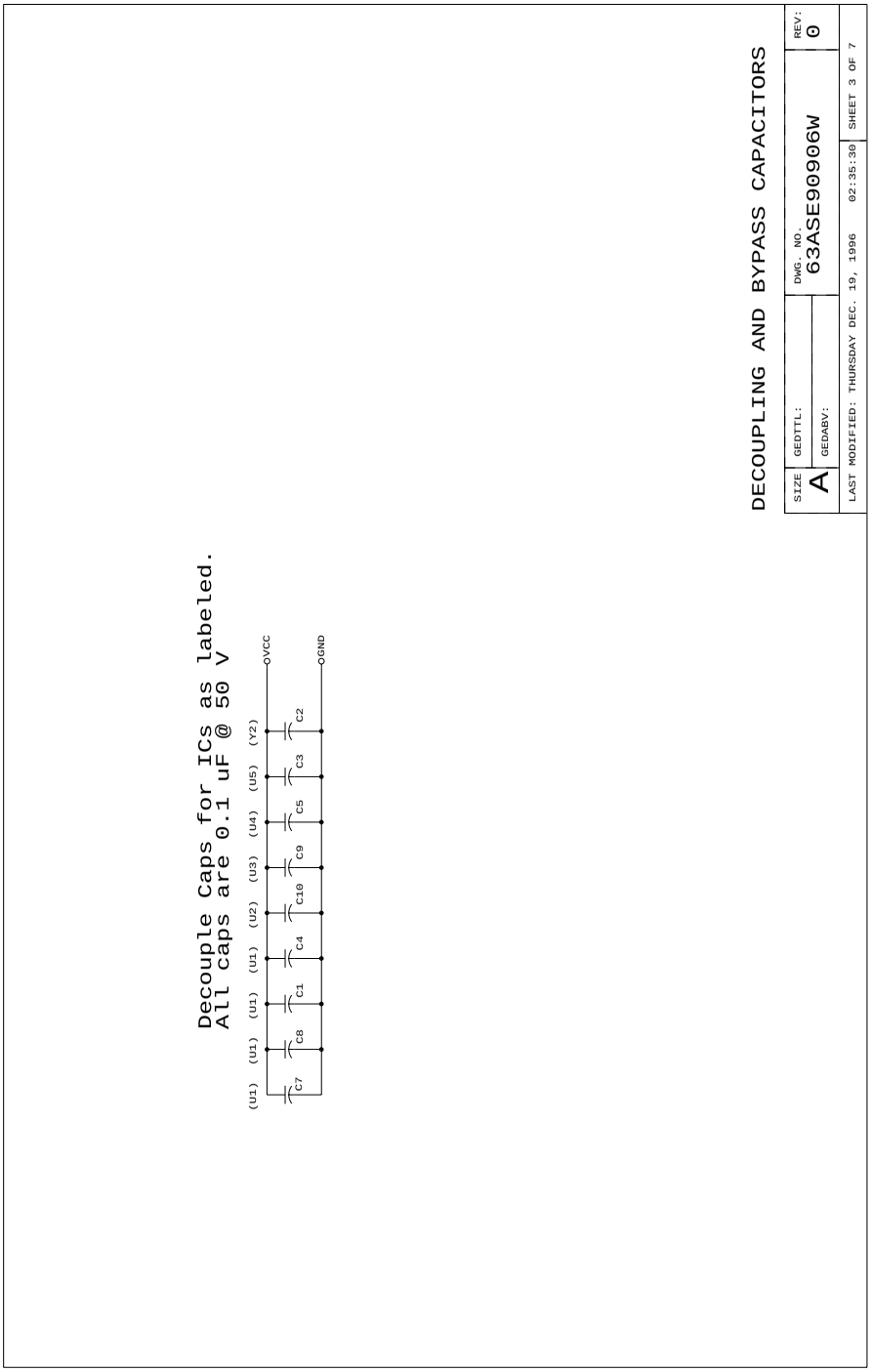
8. GROUND LOCATIONS
   UNLESS OTHERWISE SPECIFIED, GROUND IS APPLIED TO:
   PIN 4 OF ALL 8-PIN ICS
   PIN 7 OF ALL 14-PIN ICS
   PIN 8 OF ALL 16-PIN ICS
   PIN 10 OF ALL 20-PIN ICS
   PIN 12 OF ALL 24-PIN ICS, ETC.

| LAST USED | UNUSED |
|---|---|
| CR2 | |
| U5 | |
| R15 | |
| C12 | |
| Q1 | |
| Y2 | |
| W1 | |
| J2 | |
| P2 | |
| RN4 | |
| | |
| | |
| | |
| | |
| | |
| | |
| | |
| | |

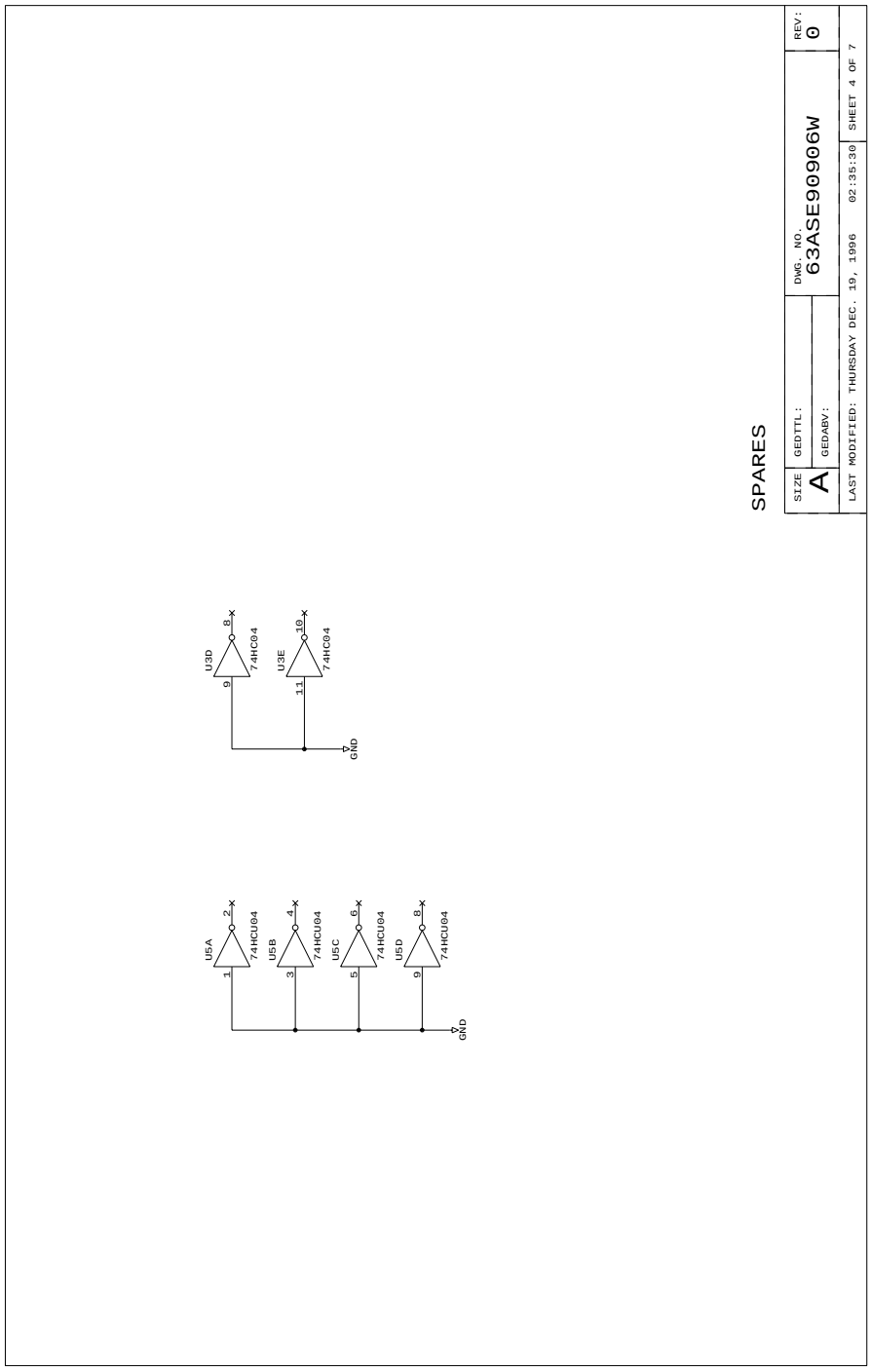
LAST USED REFDES TABLES

| SIZE | GEDTTL: | DWG. NO. | REV: |
|---|---|---|---|
| A | GEDABV: | 63ASE90906W | 0 |
| LAST MODIFIED: THURSDAY DEC. 19, 1996 02:35:30 | | SHEET 2 OF 7 | |

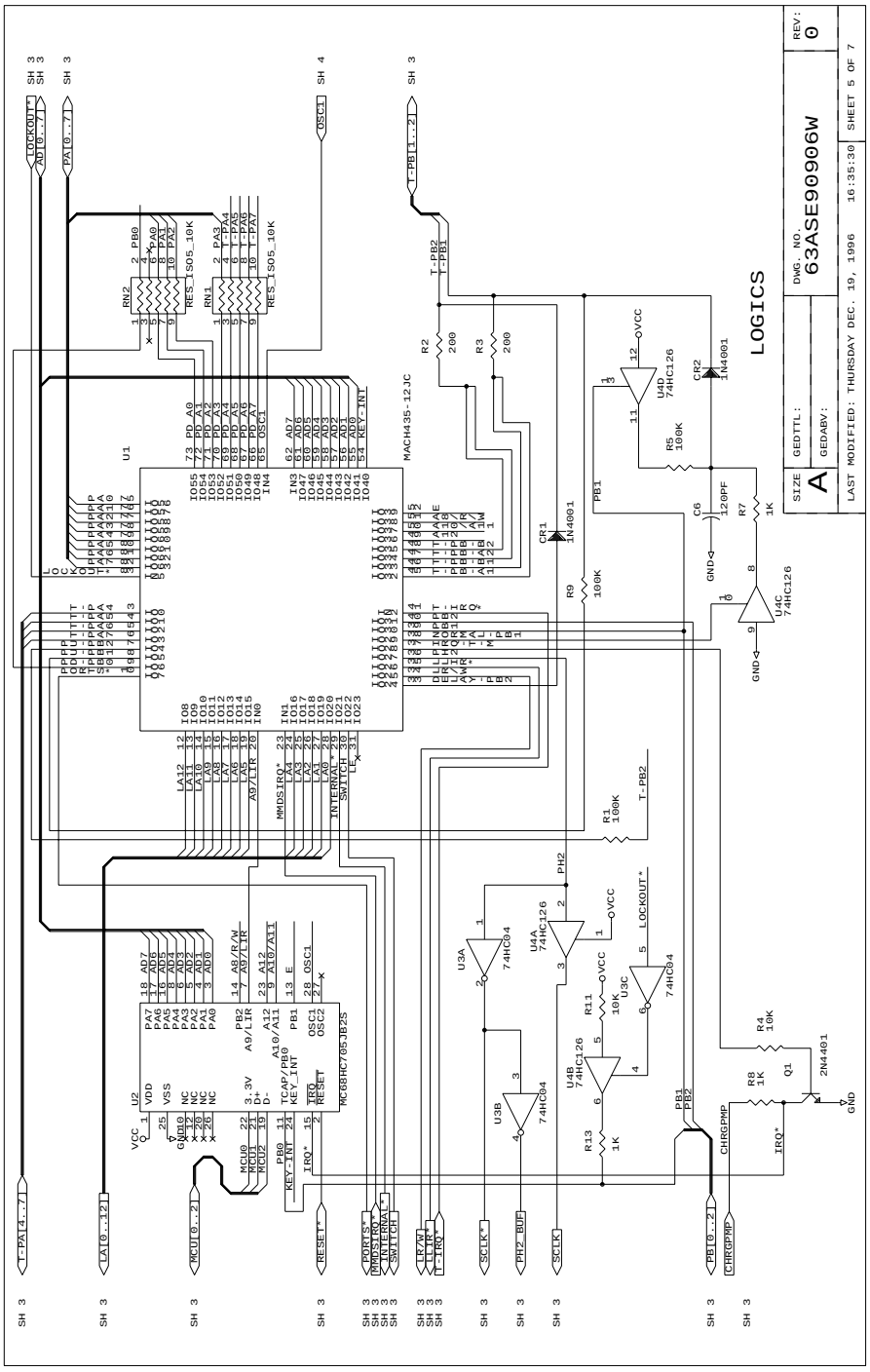
## M68EM05JB2 Schematics (Sheet 3 of 7)



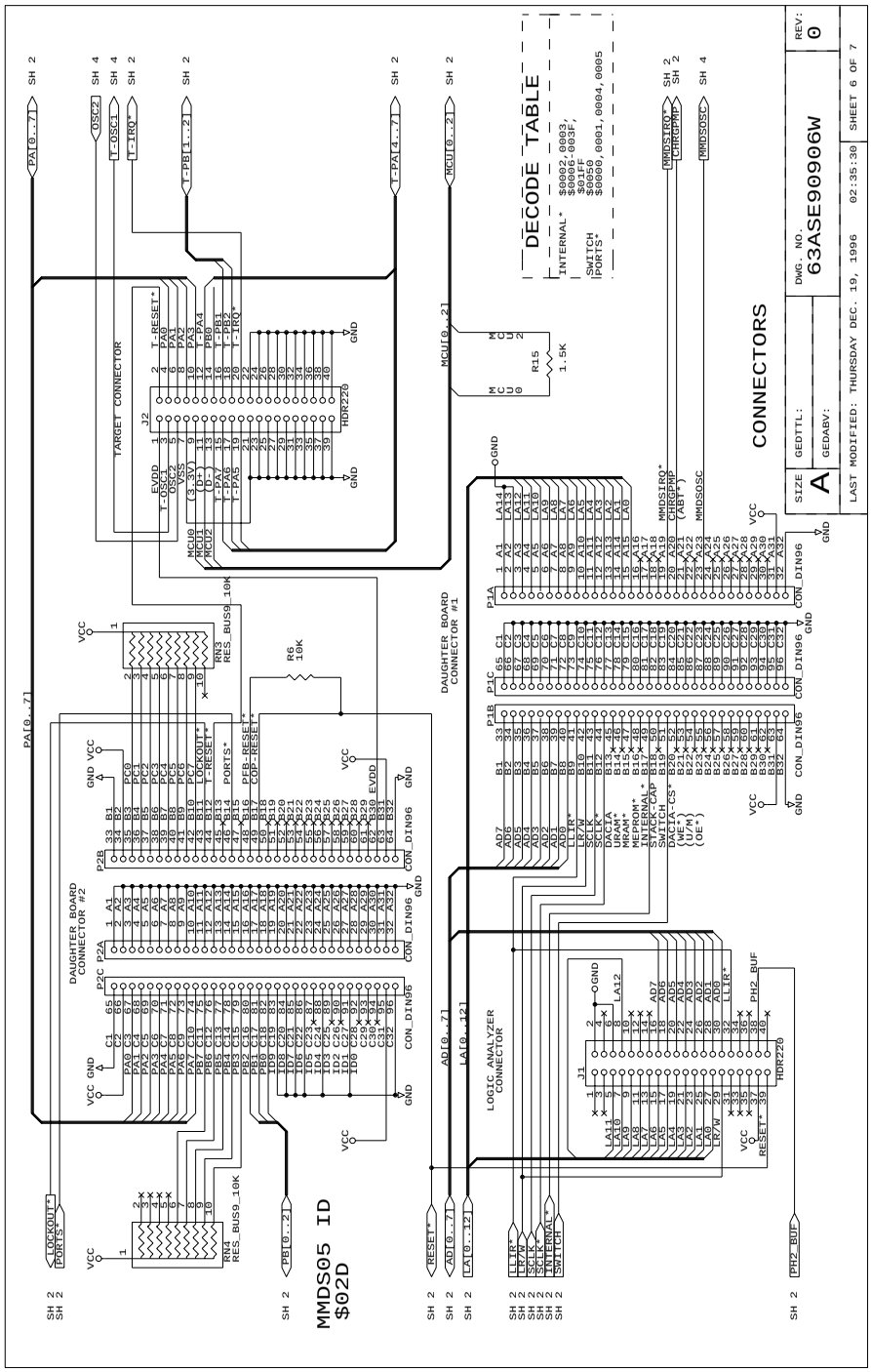
## M68EM05JB2 Schematics (Sheet 4 of 7)



**M68EM05JB2 Schematics (Sheet 5 of 7)**



## M68EM05JB2 Schematics (Sheet 6 of 7)



## M68EM05JB2 Schematics (Sheet 7 of 7)