

# *Mask Set Errata 1*

## **MC68HC705E1 8-Bit Microcontroller Unit**

### **INTRODUCTION**

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This errata provides timer overflow and real-time interrupt information applicable to the following MC68HC705E1 MCU mask set devices:

- D32N

### **MCU DEVICE MASK SET IDENTIFICATION**

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The mask set is identified by a four-character code consisting of a letter, two numerical digits, and a letter (e.g., D32N). Slight variations to the mask set identification code may result in an optional numerical digit preceding the standard four-character code (e.g., 1D32N).

### **MCU DEVICE DATE CODES**

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Device markings indicate the week of manufacture and the mask set used. The data is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. The date code "9115" would indicate the 15th week of the year 1991.

### **MCU DEVICE PART NUMBER PREFIXES**

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Some MCU samples and devices are marked with an "SC" or "XC" prefix. An "SC" prefix denotes special/custom device. An "XC" prefix denotes device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the "MC" prefix.

*Whenever contacting a Motorola representative for assistance, please have the MCU device mask set and date code information available.*

Specifications and information herein are subject to change without notice.



## TIMER OVERFLOW OR REAL-TIME INTERRUPTS

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In rare instances, clearing any of the timer control and status register (TCSR) flag or enable bits could result in vectoring to the reset vector rather than the timer interrupt vector if the correct precautions are not followed. Do not clear any of the timer flags or enable bits (i.e., TOF, TOFE, RTI, and RTIF) with bit manipulation instructions.


### CLEARING TIMER OVERFLOW FLAG (TOF) BIT

```
SEI          SEI NOT REQUIRED IF USED WITHIN TIMER INTERRUPT ROUTINE.
LDA         #$73
AND         $TCSR
OR          #$40      MASK RTIF BIT
STA         $TCSR
CLI          DO NOT USE CLI IF THIS CODE SEGMENT IS USED WITHIN
              TIMER INTERRUPT ROUTINE.
```

### CLEARING TIMER OVERFLOW FLAG ENABLE (TOFE) BIT

```
SEI          SEI NOT REQUIRED IF USED WITHIN TIMER INTERRUPT ROUTINE.
LDA         #$D3
AND         $TCSR
OR          #$C0      MASK RTIF & TOF
STA         $TCSR
CLI          DO NOT USE CLI IF THIS CODE SEGMENT IS USED WITHIN TIMER
              INTERRUPT ROUTINE.
```

Masking the real-time interrupt flag (RTIF) and timer overflow flag (TOF) bits with the OR instruction prevents these bits from being cleared if a TOF or real-time interrupt (RTI) is generated during the clearing routine. Similar sequences should be used for clearing of the RTIF and real-time interrupt enable (RTIE) bits.

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