

Mask Set Errata 1

68HRC705JP7 8-Bit Microcontroller Unit

INTRODUCTION

This mask set errata provides information regarding the analog subsystem, high-current output of port C and port B bit 4, low voltage reset, and the sample and hold capacitor leakage discharge rate of these MC68HRC705JP7 MCU mask set devices:

- 0H70H
- 1H70H

MCU DEVICE MASK SET IDENTIFICATION

The mask set is identified by a 5-character code consisting of a version number, a letter, two numerical digits, and a letter, for example 0H70H. Slight variations to the mask set identification code may result in an altered version number, for example 1H70H.

MCU DEVICE DATE CODES

Device markings indicate the week of manufacture and the mask set used. The data is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. For instance, the date code "9115" indicates the 15th week of the year 1991.

MCU DEVICE PART NUMBER PREFIXES

Some MCU samples and devices are marked with an SC or XC prefix. An SC prefix denotes special/custom device. An XC prefix denotes that the device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the MC prefix.

Whenever contacting a Motorola representative for assistance, please have the MCU device mask set and date code information available.

Specifications and information herein are subject to change without notice.



ANALOG SUBSYSTEM

These analog subsystem characteristics, which are ordinarily selectable after setting the OPT bit, are not yet available:

- Output of comparator 1 on port B bit 4
The COE1 bit is not writable. Reading it returns a logical 0.
- Ground offset voltage applied to sample capacitor
The VOFF bit is not writable. Reading it returns a logical 0.

HIGH-CURRENT OUTPUT OF PORT C AND PB4

Port C and PB4 do not yet have high-current output capabilities. Port C and port B perform to the standard V_{OL} and V_{OH} specifications mentioned for Port B. At this time, only port A has high-current output capabilities.

LOW VOLTAGE RESET (LVR) TRIP POINT AND HYSTERESIS

The LVR does not meet the minimum trip point specifications. The actual trip point may be lower than the minimum operating voltage of the CPU. Therefore, proper CPU operation down to the LVR trip point cannot be guaranteed.

The LVR also does not meet the minimum hysteresis specification.

SAMPLE CAPACITOR LEAKAGE DISCHARGE RATE

The leakage discharge rate of the internal sample and hold capacitor may not meet the specification of 0.2 V/sec at $V_{DD} = 5$ V or 0.1 V/sec at $V_{DD} = 3$ V. Actual leakage rate varies with operating method, temperature, and external grounding.

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