Mask Set Errata 1

68HC705JP7 8-Bit Microcontroller Unit

INTRODUCTION

This errata describes the various differences detected between Revision B version and Revision A silicon of the following MC68HC705JP7 MCU mask set device:

- G58T

Each of these differences has been addressed for correction or improvement in Revision C.

MCU DEVICE MASK SET IDENTIFICATION

The mask set is identified by a four-character code consisting of a letter, two numerical digits, and a letter (e.g., G58T). Slight variations to the mask set identification code may result in an optional numerical digit preceding the standard four-character code (e.g., 2G58T).

MCU DEVICE DATE CODES

Device markings indicate the week of manufacture and the mask set used. The data is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. The date code "9115" would indicate the 15th week of the year 1991.

MCU DEVICE PART NUMBER PREFIXES

Some MCU samples and devices are marked with an "SC" or "XC" prefix. An "SC" prefix denotes special/custom device. An "XC" prefix denotes device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the "MC" prefix.

Whenever contacting a Motorola representative for assistance, please have the MCU device mask set and date code information available.

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LOW POWER OSCILLATOR (LPO) IN EMULATION MODE

The HC705JP7 LPO is usually disabled in emulation mode, and the OM1 and OM2 bits choose one of two external clocks. However, the LPO is not disabled properly in emulation mode. Selecting LPO in emulation mode causes the LPO to drive the 68HC705JP7, such that the mother board loses communication with the daughter board.

OSCILLATOR SELECT BITS IN EMULATION MODE

The oscillator select bits OM1 and OM2 in the ISCR are designed to come out of reset with the OM2 bit set and the OM1 bit cleared in single-chip mode, which is the case for the LPO to be selected and the EPO to be disabled. However, when operating in emulation mode, the external oscillator will be selected to drive the chip. The OM2 bit is cleared and the OM1 bit is set to indicate the selection of the EPO and that the LPO is disabled. The chip, therefore, is not performing as the OM bits indicate following a reset on the emulator.

Revision C will have the OM bits come out of reset with the single-chip mode (OM2 set, OM1 clear, for example) in all cases, but with the external oscillator selected when in emulation mode.

ILADR IN EMULATION MODE

The illegal address reset function (ILADR) is active in emulation mode and occurs while executing code outside of RAM or EPROM.

To prevent ILADR in emulation mode, avoid developing code in the area of $0100 through $06FF.

LVR NONFUNCTIONAL

The LVR function is inverted and has been disabled in Revision B to prevent a device reset while programming the MOR. All MOR bits are functional with the exception of the LVREN bit.

SIOP DATA TRANSFERS

The state machine in the SIOP was changed to accommodate the idle state control option. The new state machine uses a larger bit counter that does not roll back to 0 at the end of an operation. So when the next operation is started (write to the data register), the count is immediately completed. The bit counter is reset only after a write to the SCR control register or by a reset.

To send and receive data to and from the SIOP, always insert an added dummy write to the SCR after writing to the SDR.

SIOP CANNOT RECEIVE DATA AT THE FASTEST RATE

Data received from another chip running at the maximum baud rate may be received in error. However, the SIOP can receive data at slower rates. The problem results from the addition of the clock phase selection to the SIOP. The clocking of a digital dual flip-flop version causes too much delay at higher clock rates, such that the SCK needs an edge detector to keep up.

CPF2 FLAG BIT ERRATIC

The CPF2 flag bit in the ASR is not set occasionally when using the A/D conversion method in mode 1. See the **Section 8. Analog Subsystem** section of the *MC68HC70JJ7/MC68HC705JP7 General Release Specification* (HC705JP7GRS/D) for more information. However, the CHG bit in the ACR does get cleared such that the software may get stuck if it is looping while testing the comparator 2 output flag. The CPF2 output flag will never get set because the charge current has been turned off.

In mode 1, do not use a test of the CPF2 in the ASR to determine the end of the charge cycle. Use a test of the CHG bit in the ACR instead.

LPO FREQUENCY INCORRECT

The LPO frequency is running at approximately 250 kHz rather than at the design specification of 60–140 kHz.

RESET PULLUP CURRENT LOW

Measurement of first silicon devices shows that the current is approximately 1–3 μA. This results in an equivalent impedance of about 700–1200 kΩ. In the presence of external noise, this value may be too low. The design specification is 10 μA minimum.

An external 620-kΩ resistor from the $\overline{\text{RESET}}$ pin to the V_{DD} pin will provide the specified pullup current for 5 volts at V_{DD}.

VOLTAGE DIVIDER SELECT

Control bits DHOLD and INV are interchanged in the AMUX register. The DHOLD function is located at the INV location, and the INV function is located at the DHOLD location.

Use an include file with all assembled code which has these bits reassigned as they appear in Revision B.

EXTERNAL PIN OSCILLATOR (EPO) RC OSCILLATOR CAPABILITY

The internal capacitor size and options for the RC option of the EPO are not functional in the Revision B silicon.

ANALOG INPUT NOISE

The unconnected input channels tend to exhibit some DC bias (approximately 200 mV) and a spike during the conversion process (ramp). Turning on the input pulldown devices helps reduce these significantly. See **Parasitic Leakage on Sample Capacitor** for more information about the leakage path for the sample and hold capacitor.

ON-CHIP TEMPERATURE SENSOR

An on-chip temperature sensor as described in the specification is not available in the Revision B silicon.

LOWER LPO FREQUENCY OPTION

The option for a lower LPO frequency as described in the specification is not available in the Revision B silicon.

PB0 DISCHARGE DEVICE LOW

The discharge current applied to the external ramping capacitor connected to PB0 is slightly below specification limits, typically at 95 μA.

PARASITIC LEAKAGE ON SAMPLE CAPACITOR

The internal sample and hold capacitor has a parasitic leakage path to V_{SS}. This leakage is aggravated by the connection of the PB4 pin to a voltage less than 1.0 volt. This behavior is less evident when operating at the lower V_{DD} levels from 2.7 to 3.3 volts. This leakage is not significant if direct connections are maintained during A/D integration. Therefore, conversions using sample and hold are not reliable on revision B silicon.

MINIMUM V_{SS} OFFSET IN A/D CONVERSIONS

The external ramping capacitor is discharged down to the level of the internal analog V_{SS} supply rail. In the Revision B silicon, this node shares the current path for the analog subsystem. Therefore, the capacitor is discharged to an offset voltage slightly above the external V_{SS} pin. An applied unknown voltage must now rise to more than this amount above the V_{SS} pin in order for the positive input to change above this offset. This offset makes measuring voltages below 50 mV above the V_{SS} pin difficult.

In Revision C silicon, the discharge device will be moved closer to the AN0 pin, and the shared current path resistance is reduced as much as possible. This will reduce the minimum offset but will not eliminate it. The specification has been revised to include a maximum offset below which A/D measurements cannot be made.

This offset does not affect the ability of either comparator to detect differences between their inputs when both are near the V_{SS} supply.

VOLTAGE SENSITIVITY ON RESISTANCE DIVIDER

The 1/2 voltage divider ratio that can be selected for comparator 2 exhibits a sensitivity to applied voltage such that the divider ratio is not constant for all levels of applied input voltage. The variation can be as much as a 7 percent drop in the divider ratio from 1.0 to 5.0 volts applied signal.

STARTUP DELAY INVERTED

The unprogrammed MOR (when DELAY=0) has a start delay of 4064 bus cycles rather than 16 cycles as defined in the specification. This excessive startup delay is driven by the LPO instead of the EPO.

Additional mask set erratas can be found on the World Wide Web at http://Design-NET.com/csic/TECHSPRT/TechSprt.htm.