

Mask Set Errata 4 **68HC705P6 8-Bit Microcontroller Unit**

INTRODUCTION

This errata provides information pertaining to the SIOP applicable to the following 68HC705P6 MCU mask set device:

- E20Y

MCU DEVICE MASK SET IDENTIFICATION

The mask set is identified by a four-character code consisting of a letter, two numerical digits, and a letter (e.g., E20Y). Slight variations to the mask set identification code may result in an optional numerical digit preceding the standard four-character code (e.g., 0E20Y).

MCU DEVICE DATE CODES

Device markings indicate the week of manufacture and the mask set used. The data is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. The date code "9115" would indicate the 15th week of the year 1991.

MCU DEVICE PART NUMBER PREFIXES

Some MCU samples and devices are marked with an "SC" or "XC" prefix. An "SC" prefix denotes special/custom device. An "XC" prefix denotes device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the "MC" prefix.

Whenever contacting a Motorola representative for assistance, please have the MCU device mask set and date code information available.

Specifications and information herein are subject to change without notice.



SIOPI

The SPIF bit in the serial status register (SSR) should be cleared by reading the SSR with SPIF set and then accessing the serial data register. When the SIOPI is configured for slave mode only, a race condition can occur between the last rising edge of SCK and an access of the SSR, such that SPIF is not cleared with the previously mentioned sequence. The race condition depends on the relationship between the rising edge of SCK and the internal CPU clock edges.

The code for waiting for a transmission in slave mode often looks like:

```
WAIT      BRCLR      SPIF, SSR, WAIT
          LDA        SDR
```

The temporary solution is to add another instruction to read the SSR before the serial data register is accessed.

```
WAIT      BRCLR      SPIF, SSR, WAIT
          LDA        SSR
          LDA        SDR
```

Change the logic for clearing the SPIF bit.

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