Mask Set Errata 3

68HC705P9 8-Bit Microcontroller Unit

INTRODUCTION

This errata provides information pertaining to the serial input-output port (SIOP) master mode initial faulty transmission applicable to the following 68HC705P9 MCU mask set devices:

- D54E

MCU DEVICE MASK SET IDENTIFICATION

The mask set is identified by a four-character code consisting of a letter, two numerical digits, and a letter (e.g., D54E). Slight variations to the mask set identification code may result in an optional numerical digit preceding the standard four-character code (e.g., 0D54E).

MCU DEVICE DATE CODES

Device markings indicate the week of manufacture and the mask set used. The data is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. The date code "9115" would indicate the 15th week of the year 1991.

MCU DEVICE PART NUMBER PREFIXES

Some MCU samples and devices are marked with an "SC" or "XC" prefix. An "SC" prefix denotes special/custom device. An "XC" prefix denotes device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the "MC" prefix.

Whenever contacting a Motorola representative for assistance, please have the MCU device mask set and date code information available.

SIOP MASTER MODE INITIAL FAULTY TRANSMISSION

A design flaw has been identified that affects only the first transmission after enabling the SIOP in the master mode. Subsequent transmissions from the SIOP are correct.

This error is caused by a delay between the serial port enable (SPE) and the master mode select (MSTR) bits in the SIOP control register. If the SPE and MSTR bits are set with the same write instruction, a race condition occurs in the SIOP logic. This race condition causes the SIOP to be enabled in the slave mode before recognizing the setting of the MSTR bit. In this short period of time, the serial clock (SCK) signal is propagated throughout the SIOP logic. When the MSTR bit is finally recognized, the SCK line is pulled high. If the state of the SCK line was initially low before enabling the SIOP, then the SIOP logic will recognize a low (zero) to high (one) transition on the SCK line and transmit one bit. When the next transmission is made, which is the first true transmission by the user, a data collision will result because a transmission has already been started by the previous SCK transition. The user may also notice that the first transmission has only 7 low to high SCK transitions.

One of two things may be done to avoid this problem. The MSTR bit can be set first, and then the SIOP enabled in a subsequent write operation. An example is shown below:

```
bset    4,$0A
bset    6,$0A
```

The SCK line may also be pulled high when the SIOP is enabled. This may be done by a pull-up device or by making PB7/SCK an output line and setting it high. The pull-up device, however, does not cover the possibility of the pin being an output line driving a low signal immediately before the SIOP is enabled in the master mode. If PB7/SCK line is held high, the SPE and MSTR bits may be set at the same time, as shown below:

```
lda     #$90
sta     $0A
```


Additional mask set erratas can be found on the World Wide Web at http://Design-NET.com/csic/TECHSPRT/TechSprt.htm.