

Mask Set Errata 1

68HC705V12 8-Bit Microcontroller Unit

INTRODUCTION

This mask set errata provides information pertaining to the byte data link controller (BDLC) applicable to the following 68HC705V12 MCU mask set devices:

- 0G96Y
- 1G96Y
- 2G96Y
- 3G96Y

MCU DEVICE MASK SET IDENTIFICATION

The mask set is identified by a 5-character code consisting of a version number, a letter, two numerical digits, and a letter, for example 0G39Y. Slight variations to the mask set identification code may result in an altered version number, for example 1G39Y.

MCU DEVICE DATE CODES

Device markings indicate the week of manufacture and the mask set used. The data is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. For instance, the date code "9115" indicates the 15th week of the year 1991.

MCU DEVICE PART NUMBER PREFIXES

Some MCU samples and devices are marked with an SC or XC prefix. An SC prefix denotes special/custom device. An XC prefix denotes that the device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the MC prefix.

Whenever contacting a Motorola representative for assistance, please have the MCU device mask set and date code information available.

Specifications and information herein are subject to change without notice.



BDLC CONTROL REGISTER 1

If the CPU executes a WAIT instruction with the WCM bit of the BDLC Control Register 1 (\$3A) set, then the BDLC will not correctly receive the byte which wakes up the 68HC705V12 MCU.

BDLC IN-FRAME RESPONSE


The BDLC cannot send an in-frame response to a message against which it lost arbitration.

BSVR POLLING

A CPU read of the BDLC State Vector Register (BSVR) allows the BSVR to display its highest priority stacked flag. Reading also clears the same BSVR flag, making the next priority flag available.

However, when polling the BSVR, any of the flags can get inadvertently cleared before the software can recognize that the flag was set.

Therefore, do not poll the BSVR for status bits I3 – I0. Instead, use CPU interrupts to process the BDLC flags.

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