Mask Set Errata 2

68HC705V12 8-Bit Microcontroller Unit

INTRODUCTION

This mask set errata provides information pertaining to the byte data link controller (BDLC) applicable to the following 68HC705V12 MCU mask set devices:

- 0G96Y
- 1G96Y
- 2G96Y
- 3G96Y
- 0H52P

MCU DEVICE MASK SET IDENTIFICATION

The mask set is identified by a 5-character code consisting of a version number, a letter, two numerical digits, and a letter, for example 0G39Y. Slight variations to the mask set identification code may result in an altered version number, for example 1G39Y.

MCU DEVICE DATE CODES

Device markings indicate the week of manufacture and the mask set used. The data is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. For instance, the date code “9115” indicates the 15th week of the year 1991.

MCU DEVICE PART NUMBER PREFIXES

Some MCU samples and devices are marked with an SC or XC prefix. An SC prefix denotes special/custom device. An XC prefix denotes that the device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the MC prefix.

Whenever contacting a Motorola representative for assistance, please have the MCU device mask set and date code information available.

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If a short-to-ground occurs on the SAE J1850 bus while a message is being transmitted, the BDLC can enter a state in which it is unable to transmit any more messages until it is reset to a known state. For this error to occur, the short-to-ground of the SAE J1850 bus must meet these strict conditions:

- The start of the J1850 bus short must occur after the bit or symbol preceding a message byte has been recognized as valid but before the rising edge of the second bit in the message byte (first active bit) has occurred. For the first byte of a message, this means that the short must occur after the start of frame (SOF) symbol has been recognized as valid and before the second bit of the byte has started. For any following message bytes, the short must start after the last bit of the previous byte has been recognized as a valid bit and before the second bit of the byte has started.
- The J1850 bus short must then short the bus long enough to prevent the second bit in the message byte from being recognized as a valid symbol. This means that if a long high symbol is being transmitted as the second bit of a byte and it is shorted to the length of a short high bit, this error will not occur. This error will manifest itself only if the second bit is shorted to a length less than that defined for a valid active symbol.

If the short-to-ground of the SAE J1850 bus does not meet the above conditions, the BDLC will not enter the state where it is unable to transmit.

If a short happens as described above, these events will occur:

- The invalid symbol flag ($1C), which is the highest priority, will be set in the BSVR.
- The loss of arbitration (LOA) flag ($14) may be set in the BSVR.
- The CRC flag ($18) will be set in the BSVR after an end of data (EOD) symbol has been recognized on the bus.
- Once the short is cleared, the BDLC may transmit an active symbol onto the SAE J1850 bus before halting transmission. Or if this active symbol is transmitted, it will be interpreted as an invalid symbol by any other node on the network.
- The BDLC will then enter a lockup state (unable to transmit) and will remain in this state until either another message is received from the SAE J1850 bus or until a WAIT instruction is executed.

To remedy a short temporarily, use either of these steps. Using both steps is not necessary.

- Receive another message. When another message is received, the rising edge of the SOF symbol will reset the BDLC to its initial state, resolving the problem. The message which resets the BDLC will be received correctly.
- Execute a WAIT instruction. This instruction will place the BDLC into its reset state. Exit from wait mode can be achieved by the reception of a message from the SAE J1850 bus or through a timer or hardware interrupt.

Additional mask set erratas can be found on the World Wide Web at http://Design-NET.com/csic/TECHSPRT/TechSprt.htm.