

## *Mask Set Errata 1*

# **XC68HC05JP6 8-Bit Microcontroller Unit**

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## **INTRODUCTION**

This mask set errata provides information pertaining to the low power oscillator (LPO) nominal frequencies, internal temperature sensing diode, low voltage inhibit (LVI) hysteresis, the sample-and-hold capacitor, and the serial input/output port (SIOP) interrupt applicable to these XC68HC05JP6 MCU mask set devices:

- 0H96J, 1H96J, 2H96J, 3H96J

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## **MCU DEVICE MASK SET IDENTIFICATION**

The mask set is identified by a 5-character code consisting of a version number, a letter, two numerical digits, and a letter, for example 3H96J. Slight variations to the mask set identification code may result in an altered version number, for example 4H96J.

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## **MCU DEVICE DATE CODES**

Device markings indicate the week of manufacture and the mask set used. The date is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. For instance, the date code "9115" indicates the 15th week of the year 1991.

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## **MCU DEVICE PART NUMBER PREFIXES**

Some MCU samples and devices are marked with an SC or XC prefix. An SC prefix denotes special/custom device. An XC prefix denotes that the device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the MC prefix.

*When contacting a Motorola representative for assistance, please have the MCU device mask set and date code information available.*

Specifications and information herein are subject to change without notice.

## LOW POWER OSCILLATOR (LPO) NOMINAL FREQUENCIES

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The LPO nominal frequencies do not meet the specified  $\pm 40\%$  of the center frequencies of 100 KHz and 500 KHz and are tested at  $+40\%$  and  $-50\%$  of the center frequencies.

## INTERNAL TEMPERATURE SENSING DIODE

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The internal temperature sensing diode does not meet the specified 0.65 V – 0.71 V rating and the temperature change in voltage of 2.0 – 2.2 mV/° C and is not currently tested.

## LOW VOLTAGE INHIBIT (LVI) HYSTERESIS

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The LVI hysteresis does not meet the 100 mV minimum and is currently tested for 30 mV minimum.

## SAMPLE-AND-HOLD CAPACITOR

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The sample-and-hold capacitor does not meet the leakage discharge rate specification of 0.2 V per second above 25° C.


## SERIAL INPUT/OUTPUT PORT (SIOP) INTERRUPT

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Refer to these two items regarding the SIOP interrupt.

- Item #1** The SIOP may fail to set the serial port interrupt flag (SPIF) when a byte of data is received. The CPU fails to assert an interrupt if the serial peripheral interrupt enable (SPIE) bit in the SIOP control register (SCR) is set.
- Item #2** If the CPU stacks because the analog subsystem asserts a CPU interrupt and if the SIOP asserts a CPU interrupt during this time, then the CPU loads its program counter (PC) with the vector address stored in memory locations \$1FF0 and \$1FF1, which do not contain interrupt vectors.

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